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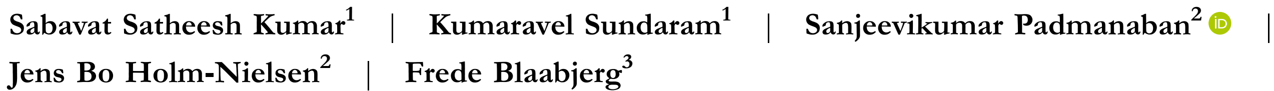
ORIGINAL RESEARCH PAPER

A low power and soft error resilience guard-gated Quartro-based flip-flop in 45 nm CMOS technology



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Abstract

Conventional flip-flops are more vulnerable to particle strikes in a radiation environment. To overcome this disadvantage, in the literature, many radiation-hardened flip-flops (FFs) based on techniques like triple modular redundancy, dual interlocked cell, Quatro and guard-gated Quatro cell, and so on, are discussed. The flip-flop realized using radiation hardened by design Quatro cell is named as the improved version of Quatro flip-flop (IVQFF). Single event upset (SEU) at inverter stages of master/slave and at output are the two drawbacks of IVQFF. This study proposes a guard-gated Quatro FF (GQFF) using guard-gated Quatro cell and Muller C-element. To overcome the SEU at inverter stages of IVQFF, in GQFF, the inverter stages are realized in a parallel fashion. A dual-input Muller C-element is connected to the GQFF output stage to mask the SEU and thus maintain the correct output. The proposed GQFF tolerates both single node upset (SNU) and double node upset (DNU). It also achieves low power. To prove the efficacy, GQFF and the existing FFs are implemented in 45 nm Complementary Metal Oxide Semiconductor (CMOS) technology. From the simulation results, it may be noted that the GQFF is 100% immune to SNUs and 50% immune to DNUs.

1 | INTRODUCTION

Scaling of technology causes higher packaging densities, reduction in node voltage and reduced device size. Hence, the critical charge quantity needed to upset the state of the memory cell is drastically reduced. Even an incident ion particle with a lesser amount of energy causes a single event upset (SEU) [1]. A conventional latch or FF is highly susceptible to particle strikes [2]. In the hold state, a single event may upset the state of the latch or FF, and these erroneous values are not corrected until a correct value is written into the latch or flip-flop. There are broad spectrums of SEU mitigation techniques proposed in recent years [3-14]. Recently proposed radiation-hardened designs include triple modular redundancy (TMR), dual interlocked cell (DICE) and Quatro cell and so on, are the most popular techniques to mitigate SEUs in memory cells such as D-FF.

TMR [15,16] is a prevalent method to correct the SEUs. Its implementation is also comparatively straightforward. TMR technique includes three identical FF stages and a majority voter circuit. These three stages perform the same operation, and the result is processed through a majority voter circuit. If the error occurs in any one of the stages, then the other two corrects the error. Nonetheless, the main drawback of TMR structure is that it consumes large area, delay and power than the conventional FF after considering the majority voter into account.

DICE cell [17,18] is a famous example of circuit-level radiation hardened by design (RHBD) category. The DICE cell structure is based on the conventional cross-coupled inverter latch structure, which consists of four (A, B, C and D) nodes. These four nodes store the data as two pairs of corresponding values (0101 or 1010). DICE cell's benefit is that any single node upset owing to the particle strike does not affect the other node of the same logic state. For instance, consider state 0, that is, data stored at A, B, C and D are 0101. An upset at node A can turn 'off ' P2, turns 'on' N4 and avoid propagating the upsets to node B and C. Thus, nodes B and C preserve their logic states.

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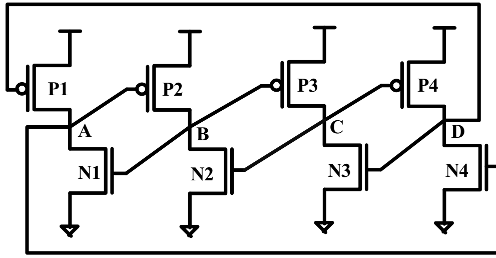


FIGURE 1 DICE cell. DICE, dual interlocked cell

Similarly, the other nodes are also immune to particle strikes. However, it remains sensitive to multiple node upsets. Figure 1 displays the schematic of DICE cell.

Beside DICE, Quatro cell [4,18] is also a notable example of circuit-level RHBD category to attain improved trade-offs among soft-error mitigation and performance penalties. The main reason for considering a Quatro cell is that it is less sensitive to charge sharing [18]. DICE and Quatro layouts in [18-20] were compactly constructed and not intended for mitigation of charge sharing. All these findings reveal that Quatro cell is suitable for achieving soft error resilience. The circuit diagram of a basic Quatro cell is presented in Figure 2(a). Similar to DICE, Quatro is also composed of four storage nodes. The Quatro cell is constructed by two pairs of cross-coupled devices, each having its load. The cross-coupled nMOS transistors have pMOS as load, and pMOS have nMOS as load. Nonetheless, Quatro remains susceptible to single node upsets (SNUs). The working of the Quatro cell will be explained in detail in Section 3.

This study proposed the soft error-resilient master-slave guard-gated Quatro FF (GQFF) based on the guard-gated Quatro cell and the Muller C-element and tested. The proposed GQFF mitigates the SNUs completely through guard-gated Quatro cell and Muller C-element. The guard gates prevent SEUs propagating in Quatro cells through feedback loops. The operation of guard-gated Quatro cell is described in detail in Section 3. The Muller C-element avoids the propagation of the upsets to the output by taking high impedance state and retains its prior state. The GQFF is also tolerant of double node upsets (DNUs). Along with the proposed design, conventional (unhardened), TMR, DICE, Quatro and IVQFFs [12-14] are implemented in 45 nm Complementary Metal Oxide Semiconductor (CMOS) technology using Cadence Spectre tool. The single and double node upset tolerances of these designs are verified, and also area, delay, power, setup time and power-delay product (PDP) are calculated through circuit simulations.

The remaining sections of this study are presented as follows: Section 2 starts with basic principles, advantages and disadvantages of TMR, DICE, Quatro and IVQFF, and introduces proposed master-slave GQFF. Section 3 describes the detailed working of proposed GQFF, its SEU resilience verification and performance comparison over the existing FFs. Section 4 describes the effects of PVT variations through Monte Carlo (MC) simulations. Section 5 concludes the study.

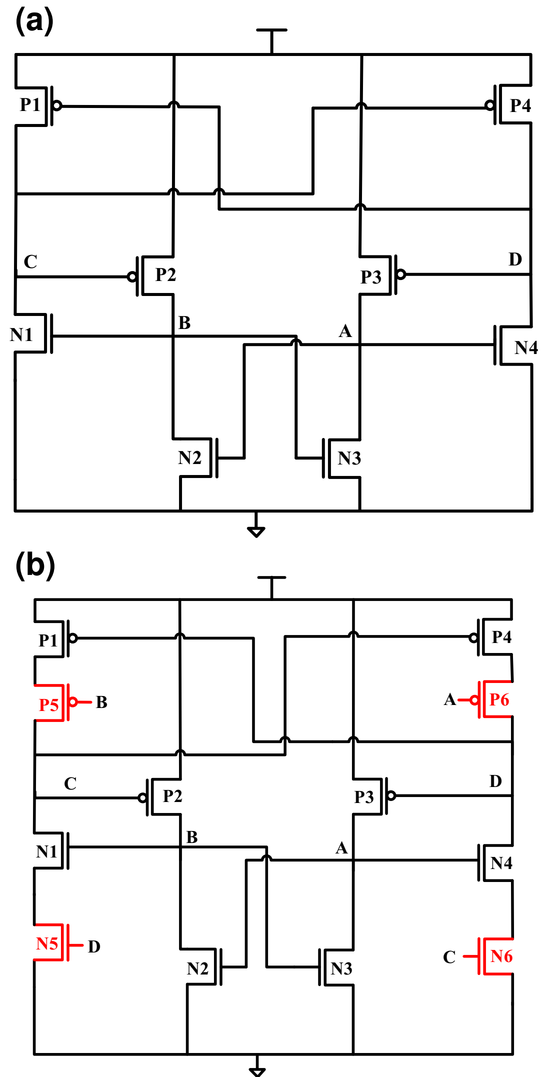


FIGURE 2 Quatro cell: (a) basic structure and (b) guard gated

2 | PREVIOUS WORK

The primary SEU mitigation methodology involves the inclusion of temporal redundancy. Figure 3 exhibits a TMR FF with the voting circuit. It uses a temporal filtering to avert SEUs [12]. From the circuit, the data input is connected to three identical edge-triggered conventional FFs simultaneously.

Similarly, the Clock (CLK) signal is also connected to three identical flip-flops with ΔT and $2\Delta T$ delays to the middle and bottom FFs [7]. The TMR FF is entirely immune for SNUs. However, the transient fault on the CLK signal results in wrong output in the circuit.

Similarly, it cannot tolerate DNUs. The consumption of area and power dissipation of TMR FF is more due to its massive structure. This disadvantage makes TMR FF less attractive.

DICE FF in [13] can 100% guarantee immunity to SNUs while maintaining a greater area and power efficiency than TMR. However, it remains sensitive to double node upsets.

This disadvantage makes DICE FF less attractive towards the realization of DNU sophisticated FF design.

The Quatro FF and IVQFF are presented in [14]. The IVQFF overcomes the disadvantages present in Quatro FF [14]. The IVQFF is realized using the RHBD cell. The circuit diagram of IVQFF is shown in Figure 4. From Figure 4, it is understood that the master and slave latches are of similar structure and are connected in series to realize the edge-triggered IVQFF. The operation of IVQFF concerning transient faults is examined with an example. Assume, the state of master as 0101(i.e. {MA, MB, MC, MD} = {0, 1, 0, 1}) for data input 1. An SEU on node MA upsets the state of MB along with node MA, while, nodes MC and MD remain unchanged (i.e. 1001). During the positive edge of the CLK, the output of the master is propagated to slave through inverter stages. Now the state of the slave latch is {SA, SB, SC, SD} = {1, 0, 1, 0}. The output of the slave latch produces an erroneous value as the output is considered across node SA. From the analysis, it can be observed that the IVQFF produces wrong output consistently if node SA produces an erroneous value even though the Quatro cell is SEU immune. Another disadvantage of IVQFF is that if the transient fault occurs on sensitive nodes of inverter stages n1 (or n2) of master and/or n3 (or n4) of the slave, it can upset multiple nodes of similar logic level on the RHBD Quatro cells and results in incorrect output. Figure 5 shows the simulation waveforms of SNU upset of the IVQFF in state 1, state 0 and nodes n3 and n4.

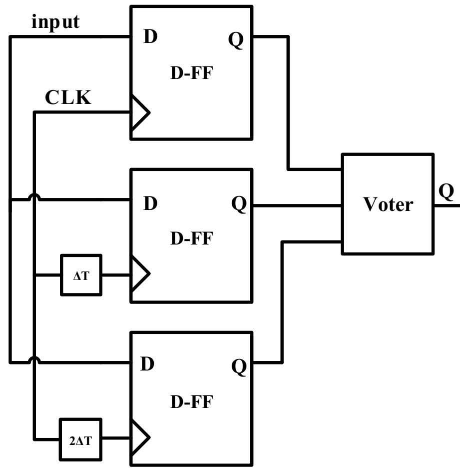


FIGURE 3 TMR FF in [12]. FF, flip-flop; TMR, triple modular redundancy

3 | PROPOSED DESIGN

The proposed master-slave GQFF shown in Figure 6 is based on guard-gated Quatro cell and Muller C-element. In GQFF, the data input and its complement are connected in a parallel fashion to the four storage nodes (MA, MB, MC and MD) of the guard-gated Quatro cell of master latch through pass

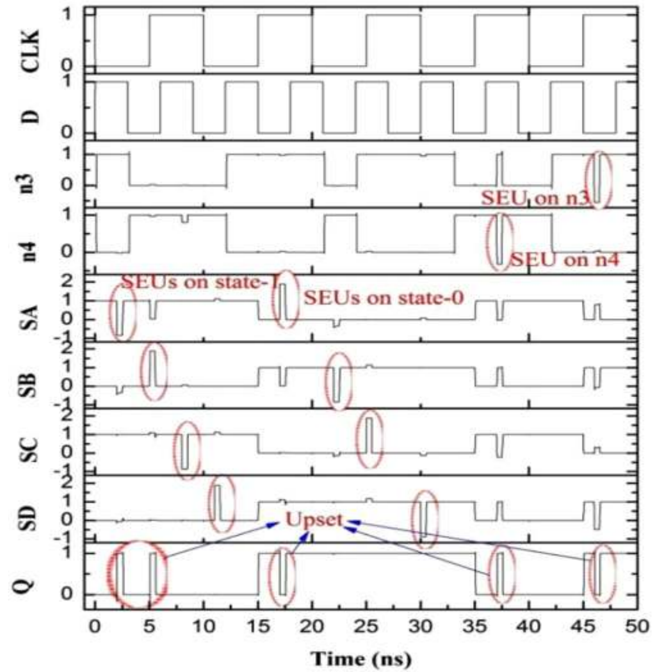


FIGURE 5 Simulation waveforms of SNU upset of the IVQFF in state 1 and state 0. IVQFF, improved version of Quatro flip-flop; SNU, single node upset

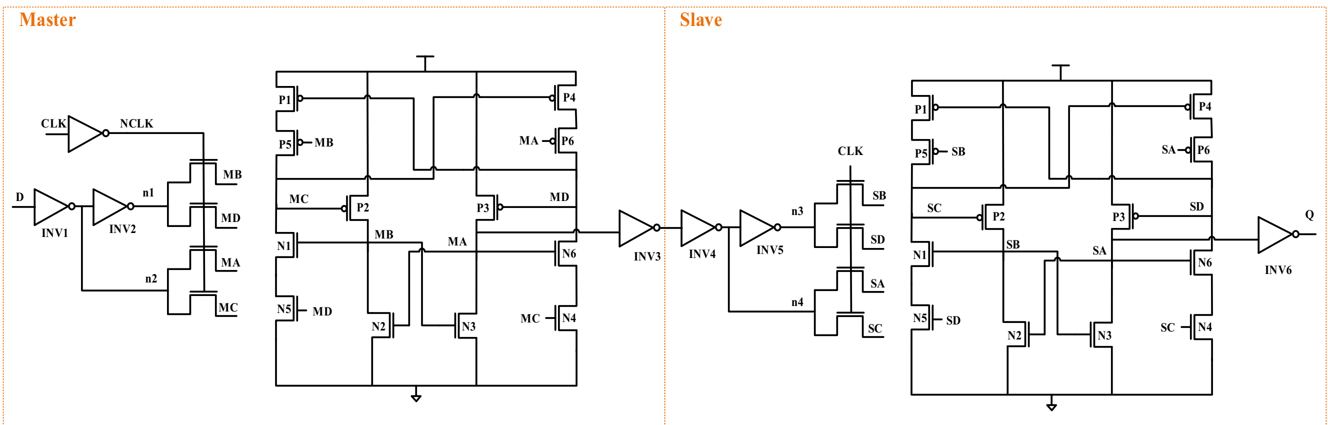


FIGURE 4 IVQFF in [14]. IVQFF, improved version of Quatro flip-flop

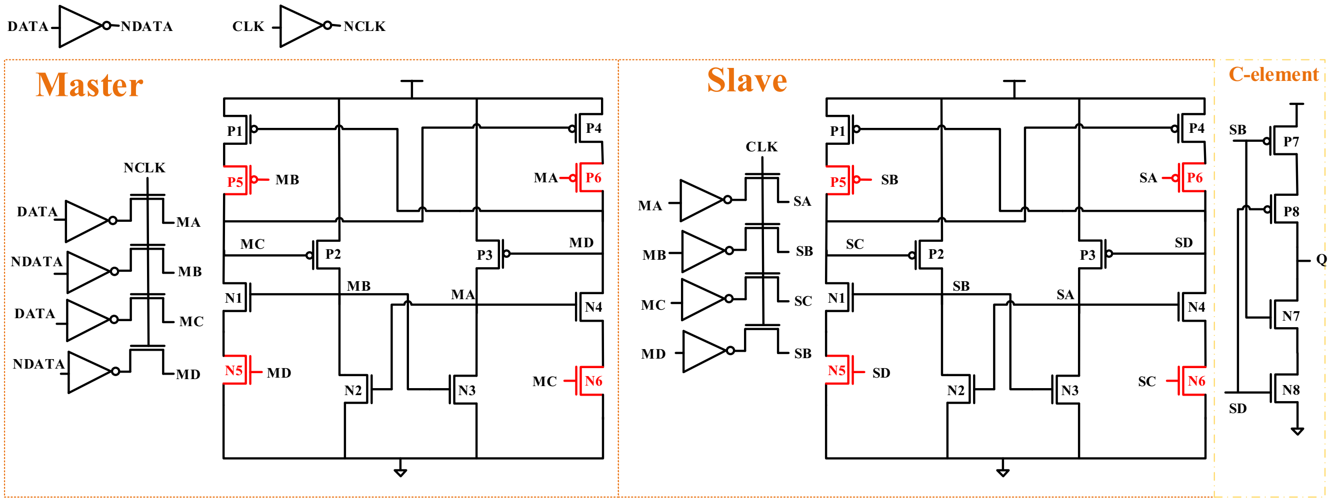


FIGURE 6 Schematic representation of proposed GQFF. GQFF, guard-gated Quatro flip-flop

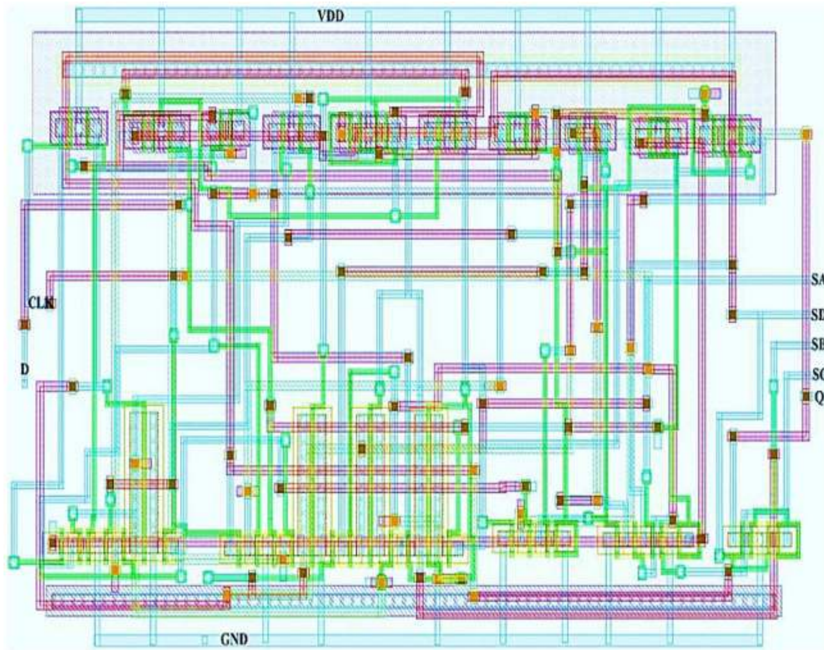


FIGURE 7 Layout of the proposed GQFF. GQFF, guard-gated Quatro flip-flop

transistors (whose gate terminals are connected to negative CLK). Subsequently, the outputs of these four nodes are provided as inputs to the other four nodes (SA, SB, SC and SD) of the slave latch. The output from SB and SD are then connected as inputs to the dual-input Muller C-element. The output of GQFF is taken across Muller C-element. Figure 7 shows the layout design of GQFF.

Since the proposed design is based on guard-gated Quatro cell shown in Figure 2(b), the operation of basic Quatro cell in Figure 2(a) and its response towards SEUs is discussed. Assume state 0 as $\{A, B, C, D\} = \{0, 1, 0, 1\}$. A positive upset pulse due to transient fault at node A can turn 'on' transistors N2 and N4. It subsequently drives nodes B and D to a logic low and drives node C to logic high. Therefore, an upset at node A can flip the whole state, that is, $\{A, B, C, D\} = \{1, 0, 1, 0\}$. Similarly, transient fault at node D can turn 'on' transistors P1 and P3. In this situation, there is a potential current competition between the 'on' state of P1-N1 and P3-N3. If the transistor sizes of P1, N1, P3 and N3 are same (or sizes of N1 and N3 are greater than P1 and P3), then the strong driving capability of N1 and N3 can preserve the logic states of nodes A and C. Hence, no upset in the state. From the analysis above, it can be observed that node A is most vulnerable to SEUs in state 0, similarly, node B in state 1.

The drawback of basic Quatro cell is overcome by a guard-gated Quatro cell. The guard-gated Quatro cell is realized by adding four extra transistors (P5, P6, N5 and N6) to the basic Quatro cell. This guard-gated Quatro cell prevents SNUs by

not propagating to the adjacent node consists of the same logic level. The working of guard-gated Quatro cell and its response towards SEUs is explained through state 0 (i.e. {A, B, C, D} = {0, 1, 0, 1}).

SEU on A: Transient fault at node A can turn 'on' transistors N2 and N4. The driving capability of N2 is increased to avoid the potential current competition between N2 and previously turned 'on' P2, which subsequently drive node B to logic low. The low level at node B turns 'off' N1 and blocks propagating to other nodes. Although the upset at node A turns 'on' N4, node D cannot alter its state because of the blocking effect of guard-gated N6. The upsets at A and B recovers after the transient fault dies down.

SEU on D: Transient fault at node D can turn 'on' P1 and P3. The driving capability of N3 is increased to avoid the potential current competition between N3 and previously turned 'on' P3, which consequently drive node A to logic low. The low level at A turns 'off' N2 and blocks which were propagating to other nodes. Even if the upset at node D turns 'on' P1, node C cannot alter its state due to the blocking effect of guard-gated P5. Finally, upset at node D recovers after the transient fault is taken off.

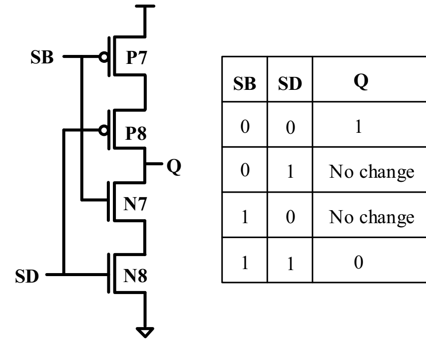
SEU on B (or C): Upset on node B (or C) blocks propagating to the other nodes thereby turning 'off' N1 and N3 (or P2 and P4). From the SNU analysis above, it is observed that any node with the particle strike has no impact on the other node with a similar logic level. The output of nodes SB and SD are connected to dual-input Muller C-element.

The output of GQFF is taken across Muller C-element. The Muller C-element prevents propagating the upsets to the output. The findings observed above are also applicable to state 1. Hence, GQFF design is realized by adopting the guard-gated Quatro cell.

SEU on <A, B>: simultaneous transient faults on nodes A and B cannot propagate inside the circuit. Hence, nodes C and D are unchanged. Due to the difference in the inputs of Muller C-element, the output is preserved. Similarly, the circuit is DNU immune in the case of <B, C> and <C, D>. The disadvantage of the system is that the nodes with similar logic levels are not immune to transient faults. Thus, faults at <A, C> and <B, D> produce the erroneous values at the output. Similarly, simultaneous fault at <A, D> also produces faulty output as it flips the whole state; as a result, the Muller C-element gets the wrong input.

Muller C-elements are essential digital blocks used in correcting the transient faults, also called as glitches. Transistor level C-element with truth table is presented in Figure 8. According to Figure 8, the output (Q) of the Muller C-element is maintained high through PMOS transistors P7 and P8 ransistors as long as the two inputs SB and SD are at a logic low level and switches to logic low only when both the inputs are at logic high (through N7 and N8 NMOS transistors). The output maintains the same state also called as no change state as the stored internal memory of C-element when the inputs are different [21].

In IVQFF if the transient fault occurs on sensitive nodes of inverter stages n1 (or n2) of master and/or n3 (or n4) of the slave, it can upset multiple nodes of similar logic level on the



SB	SD	Q
0	0	1
0	1	No change
1	0	No change
1	1	0

FIGURE 8 Muller C-element

RHBD Quatro cells and results in incorrect output. But, in the proposed GQFF due to the parallel feeding of inputs, the sensitive nodes present in the inverter stages of IVQFF (i.e. n1, n2 in the master and n3, n4 in the slave latch) is nullified. As the four nodes MA, MB, MC and MD of master and SA, SB, SC and SD of the slave are independently connected, a transient fault occurring on any individual node does not change the state of the other three nodes.

3.1 | SEU resilience verification

The analysis of the proposed GQFF for SNU and DNU tolerance is verified through transient fault injections and simulated using Cadence Spectre in 45 nm CMOS technology with 1 V supply at room temperature (27°C). For verifying SEUs for digital circuits, the transient pulse must have sufficient amplitude and width [22]. Based on the above condition, a double exponential current pulse with a minimum amplitude of 500 μA, the charge collection time constants T_α and T_β are set to be 3 ps and 1 ps correspondingly. The total collected charge Q corresponding to the double exponential current pulse used is 2fC [23].

The sizing of the proposed FF is chosen based on the difference in the mobility of PMOS and NMOS devices. The minimum width/length (W/L) of PMOS and NMOS are found to be (0.15 μm/0.045 μm) and (0.12 μm/0.045 μm), respectively, for 45 nm technology. All transistors are minimum sized except N2 and N3. The W/L of both N2 and N3 is set to be 10× faster than the minimum-sized NMOS transistor (i.e. W/L = 1.2 μm/0.045 μm).

Figure 9 exhibits the SNU resilience of the GQFF for state -1 and state - 0 at different time periods. From Figure 9, it can be observed that the circuit is 100% tolerant of particle strikes on any single circuit node. From Figure 9, statistical results for the SNUs of the GQFF are extracted and presented in Table 1. From Table 1, it can be observed that in state 1, at 5 ns fault is injected at SB, this results in an upset at SA without changing the output Q, because, Muller C-element masks the output. Similarly, the output Q is not affected by fault injections at 2 ns, 8 ns and 11 ns into SA, SC and SD, respectively. Thus, the proposed flip-flop is 100% SNU immune.

With four primary nodes (A, B, C and D), the total double node combinations are six (<A, B>, <A, C>, <A, D>, <B, C>, <B, D>and <C, D>). From Figure 10, it can be observed that in state 1, the proposed GQFF can tolerate transient faults on node pairs <A, B>, <A, D> and <C, D> but it cannot tolerate on <A, C>, <B, C> and <B, D>. Similarly, in the case of state 0, the GQFF can tolerate faults on <A, B>, <B, C> and <C, D> but it cannot tolerate on <A, C>, <A, D> and <B, D>. All these combinations are thoroughly examined and compared with the DICE and IVQFF for state 1 and state 0 and presented in Tables 2 and 3, respectively. From Tables 2 and 3, it can be observed that the IVQFF is 33% and 17%, DICE is 17% and 17% DNU immune for state 0 and state 1, respectively, while GQFF is 50% DNU immune in both state 0 and state 1, respectively. Figure 10 exhibits the DNU resilience of GQFF for state 1 at different time periods.

3.2 | Performance comparison

In this section, the proposed GQFF in Figure 6 and the existing DICE, Quatro and IVQFF are implemented in 45 nm CMOS technology for the sake of fair comparison. The comparison results of area, delay (CLK to Q), power, PDP and setup time are presented in Table 4. The power, delay, PDP and setup time are calculated from the post layout simulations under nominal conditions at 1V supply in Cadence Spectre. From the simulation results presented in Table 4, it may be

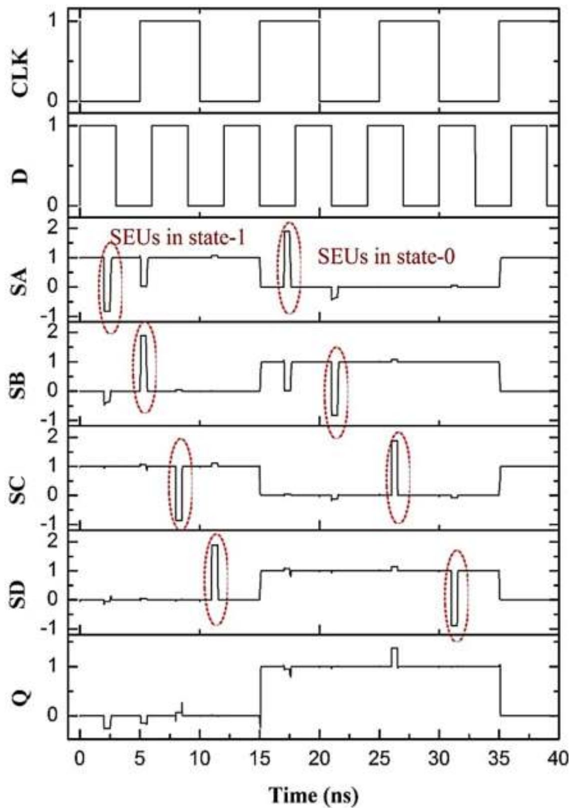


FIGURE 9 Simulation waveforms of SNU resilience of GQFF in state-1 and 0.

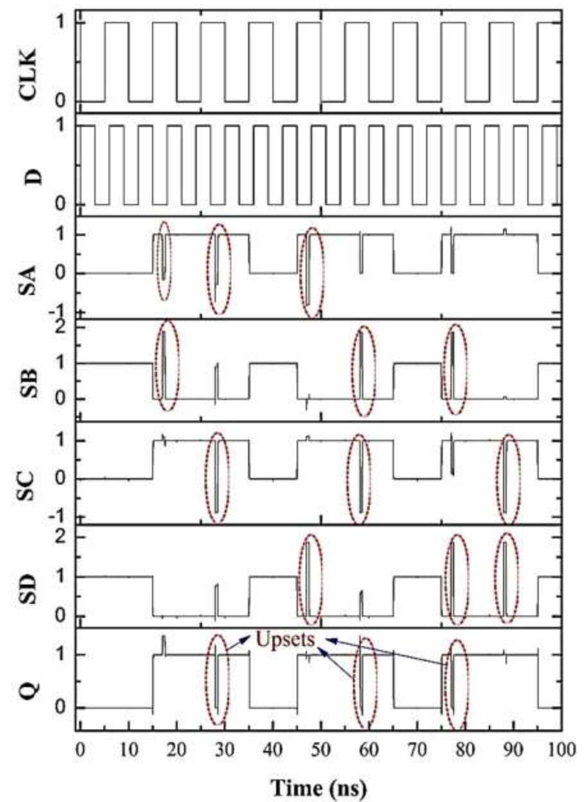


FIGURE 10 Simulation waveforms of DNU resilience of GQFF in state 1. DNU, double node upset; GQFF, guard-gated Quatro flip-flop

TABLE 1 Statistical results of SNU resilience of GQFF based on Figure 9 (for state 1 and state 0)

		Node							Node				
Time (ns)	State	SA	SB	SC	SD	Output (Q)	Time (ns)	State	SA	SB	SC	SD	Output (Q)
2	1	FI	NU	NU	NU	NU	17	0	FI	U	NU	NU	NU
5		U	FI	NU	NU	NU	21		NU	FI	NU	NU	NU
8		NU	NU	FI	NU	NU	26		NU	NU	FI	NU	NU
11		NU	NU	NU	FI	NU	36		NU	NU	NU	FI	NU

Abbreviations: FI, fault injected; GQFF, guard-gated Quatro flip-flop; NU, no upset; SNU, single node upset; U, upset.

TABLE 2 DNU sensitivities' comparison in state 1

Design	Node pairs	Node state SA	SB	SC	SD	Output Q
Proposed GQFF	<A, B>	FI	FI	NU	NU	NU
	<A, C>	FI	U	FI	U	U
	<A, D>	FI	NU	NU	FI	NU
	<B, C>	U	FI	FI	U	U
	<B, D>	U	FI	U	FI	U
	<C, D>	NU	NU	FI	FI	NU
IVQFF [14]	<A, B>	FI	FI	NU	NU	U
	<A, C>	FI	U	FI	U	U
	<A, D>	FI	NU	NU	FI	U
	<B, C>	NU	FI	FI	U	U
	<B, D>	U	FI	U	FI	U
	<C, D>	NU	NU	FI	FI	NU
DICE [13]	<A, B>	FI	FI	NU	NU	NU
	<A, C>	FI	U	FI	U	U
	<A, D>	FI	U	U	FI	U
	<B, C>	U	FI	FI	U	U
	<B, D>	U	FI	U	FI	U
	<C, D>	NU	NU	FI	FI	U

Abbreviations: DICE, dual interlocked cell; DNU, double node upset; FI, fault injected; GQFF, guard-gated Quatro flip-flop; IVQFF, improved version of Quatro flip-flop; NU, no upset; U, upset.

TABLE 3 DNU sensitivities' comparison in state 0

Design	Node pairs	Node state SA	SB	SC	SD	Output Q
Proposed GQFF	<A, B>	FI	FI	NU	NU	NU
	<A, C>	FI	U	FI	U	U
	<A, D>	FI	U	U	FI	U
	<B, C>	NU	FI	FI	NU	NU
	<B, D>	U	FI	U	FI	U
	<C, D>	NU	NU	FI	FI	NU
IVQFF [14]	<A, B>	FI	FI	NU	NU	U
	<A, C>	FI	U	FI	U	U
	<A, D>	FI	U	U	FI	U
	<B, C>	NU	FI	FI	NU	NU
	<B, D>	U	FI	U	FI	U
	<C, D>	NU	NU	FI	FI	NU
DICE [13]	<A, B>	FI	FI	U	U	U
	<A, C>	FI	U	FI	U	U
	<A, D>	FI	NU	NU	FI	U
	<B, C>	NU	FI	FI	NU	NU
	<B, D>	U	FI	U	FI	U
	<C, D>	U	U	FI	FI	U

Abbreviations: DICE, dual interlocked cell; DNU, double node upset; FI, fault injected; GQFF, guard-gated Quatro flip-flop; IVQFF, improved version of Quatro flip-flop; NU, no upset; U, upset.

noted that the power consumption of GQFF is 57.4% and 62.4% less as compared with Quatro and IVQFF, respectively. The reason for more power consumption in Quatro and IVQFF is mainly because of large-sized inverter stages and pass transistors whose gates are connected to CLK for data write operation. For the two designs, new data is entered into the storage cells by overcoming the feedback within them. This needs the driving circuits, including inverters and passes transistors, that provide sufficient driving capability to change the present state. The transistors are therefore deliberately scaled in such driving circuits to be more significant to leave more margins for reliable write operations. It is important to note that these additional transistors cause node capacitances to slow down the write operation and increase the power consumption of the Quatro and IVQFF designs. In GQFF, the inverters connected in a parallel manner for a write operation in the storage cell are of minimum sized. These minimum-sized inverters provide sufficient driving capability to change the present state. Hence, the power consumption is less in GQFF. The GQFF delay is more by 278% and 68% compared with Quatro and IVQFF, respectively. This is due to large-sized driving circuits of Quatro and IVQFF and also increased the number of transistors in GQFF. The proposed GQFF and existing FFs setup time are also calculated. From Table 4, it may be noted that the proposed GQFF, Quatro and IVQFF have comparable setup times for 1 to 0 and 0 to 1 data transition. Comparing the proposed GQFF with DICE may also make good sense. Compared to the proposed FF, the DICE has a better delay and power consumption, that is, 116% and 53% less compared to GQFF. However, in terms of DNU tolerance, the GQFF is far superior to the other existing FFs. The area (silicon area) of the FFs mentioned in Table 4 is calculated based on Equation (1). Where n1 is the number of nMOS transistors, $L_{nMOS}(i)$ and $W_{nMOS}(i)$ are sufficient length and width of each nMOS transistor. Similarly, n2 is the number of pMOS transistors, $L_{pMOS}(i)$ and $W_{pMOS}(i)$ are the effective length and the width of each pMOS transistors, respectively.

$$Area = \sum_{i=1}^{n1} (L_{nMOS}(i) \times W_{nMOS}(i)) + \sum_{i=1}^{n2} (L_{pMOS}(i) \times W_{pMOS}(i)) \quad (1)$$

4 | EFFECT OF PVT VARIATIONS ON FLIP-FLOPS

This section describes the impact of process voltage and temperature (PVT) variations on the proposed and existing FFs listed in Table 4. The process variation is different for

different technologies. However, it is more significant in lower node technologies (i.e. <65 nm). To study the impact of PVT variations, a set of MC simulations have been performed in Cadence Spectre. The results for each of the FFs are normalized with no variation to the related parameters reported in Table 4, except for supply voltage versus power/delay in Figure 11 and temperature versus power/delay in Figure 12.

Figure 11 shows the supply voltage variation impact on power/delay. The supply voltage is varied from 0.8 to 1.1 V. Figure 11(a) shows that with the increase in supply voltage, the power dissipation of all the FFs increases. However, From

TABLE 4 Performance comparisons

Design	Area (μm^2)	Delay (ps)	Power (μW)	Setup time 1→0 (ps)	Setup time 0→1(ps)	PDP (fJ)	DNU immune % in	
							State 0	State 1
DICE [13]	2.76×10^{-7}	41.3	1.1	48	49	0.045	17	17
Quatro [14]	8.8×10^{-7}	23.6	3.97	78	69	0.094	0	0
IVQFF [14]	1.12×10^{-6}	53.14	4.5	88	69	0.24	33	17
Proposed GQFF	5.32×10^{-7}	89.4	1.69	78	70	0.15	50	50

Abbreviations: DICE, dual interlocked cell; DNU, double node upset; GQFF, guard-gated Quatro flip-flop; IVQFF, improved version of Quatro flip-flop; PDP, power-delay product.

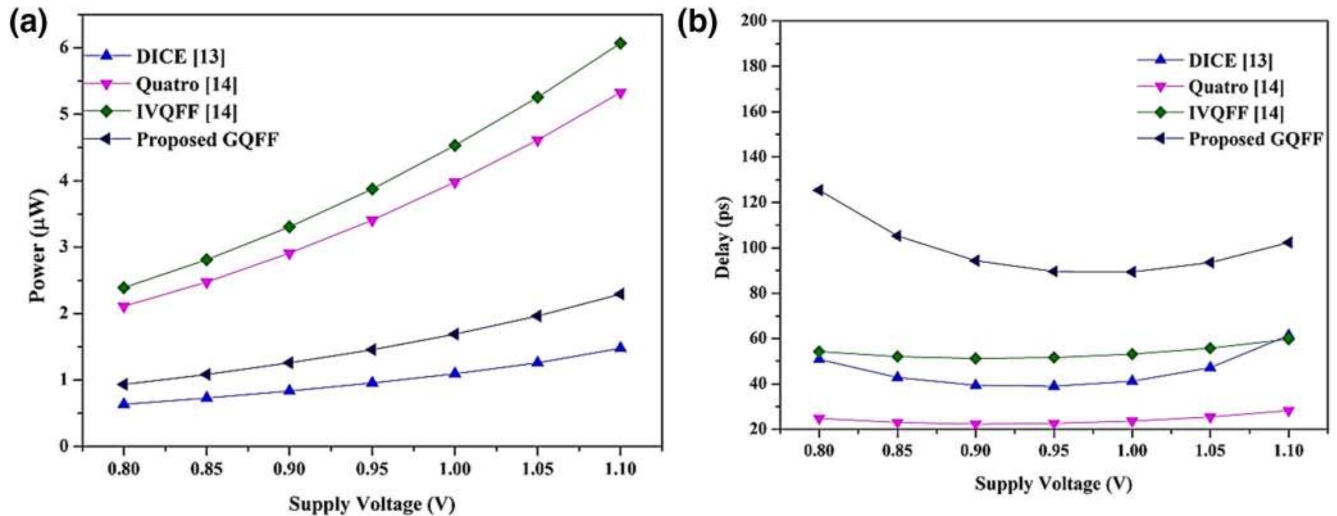


FIGURE 11 Supply voltage variation impact on (a) power dissipation and (b) Delay (CLK to Q). CLK, clock

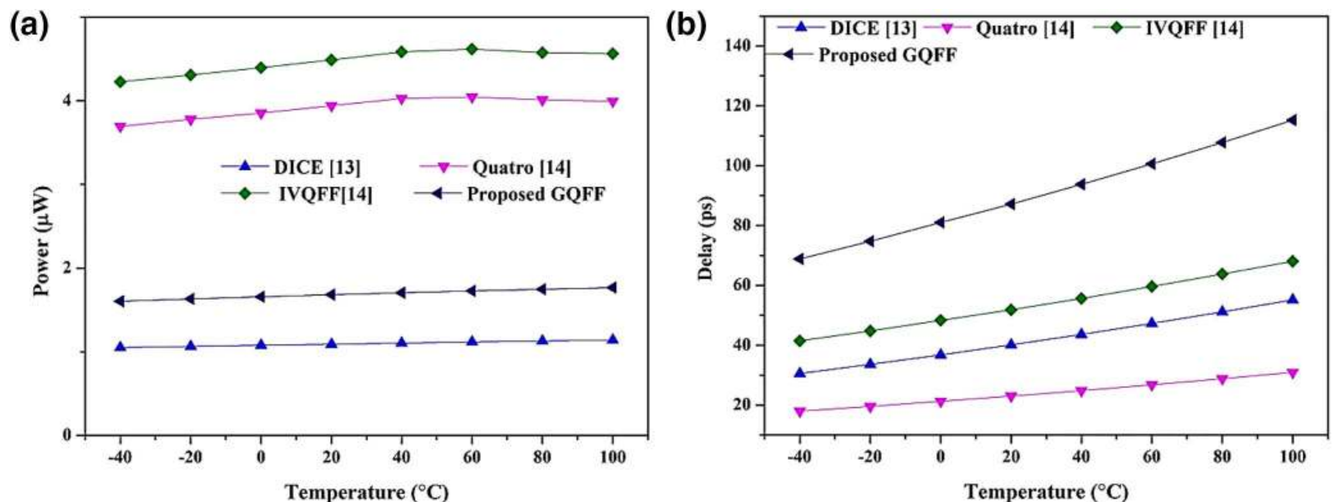


FIGURE 12 Temperature variation impact on (a) power dissipation and (b) Delay (CLK to Q). CLK, clock

Figure 11(b), it can be observed that the delay decreases as the supply voltage increases, the reason is that as the supply voltage increases the drive current in the device increases, as a consequence the delay decreases. Figure 12(a) and (b) demonstrates the impact of temperature

Quatro, IVQFF and GQFF show that the distribution of power consumption differs with a standard deviation of 53.8%, 1.76%, 1.5% and 7.2%, respectively. Therefore, the sensitivity orders for power dissipation of the proposed and existing FFs are DICE > GQFF > Quatro > IVQFF. Similarly, the distribution of delay differs with a standard deviation of 27%, 14.1%, 10.6% and 14%, respectively. The variations of the power and delay; the temperature is varied from 40°C to 100°C. It can be noted that with the increase in the temperature, the power consumption and delay increase due to reduced device carrier mobility [24-26].

For the study, the impact of process variation on the FFs and MC simulations have been carried out for 500 runs at 1 V supply and 27°C room temperature. The mean and standard deviation values for normalized power dissipation and delay of various FFs are shown in Tables 5 and 6, respectively. From Table 5, the MC simulation of DICE, sensitivity orders for delay of the FFs are DICE > Quatro ≥ GQFF > IVQFF. The proposed GQFF is a bit more sensitive to the process variations compared with Quatro and IVQFF. This is due to the feedback loops in the guard-gated Quatro cell. The feedback loops increase the circuit sensitivity to variations in parameters [27]. Another reason why the proposed GQFF is sensitive to the process variation is the use of Muller C-element. The active feedback loops in the DICE FF is more when compared to GQFF. Due to this reason, the DICE is more sensitive than all other FFs. The delay/power versus process variations is better understood with the plots shown in Figure 13. The delay is more for slow process (ss) MOSFETs and less for fast process (ff) MOSFETs. Similarly, power dissipation is less for slow process MOSFETs and more for fast process MOSFETs.

TABLE 5 Normalized mean and standard deviation values for power dissipation of FFs

	DICE [13]	Quatro [14]	IVQFF [14]	Proposed GQFF
Mean (μW)	1.1	3.94	4.5	1.7
Standard deviation (nW)	592	69.6	67.4	123

Abbreviations: DICE, dual interlocked cell; GQFF, guard-gated Quatro flip-flop; IVQFF, improved version of Quatro flip-flop; FF, flip-flop.

TABLE 6 Normalized mean and standard deviation values for delay of FFs

	DICE [13]	Quatro [14]	IVQFF [14]	Proposed GQFF
Mean (ps)	44.7	24.39	54.3	92.7
Std. dev. (ps)	12.2	3.45	5.8	13

Abbreviations: DICE, dual interlocked cell; GQFF, guard-gated Quatro flip-flop; IVQFF, improved version of Quatro flip-flop; FF, flip-flop.

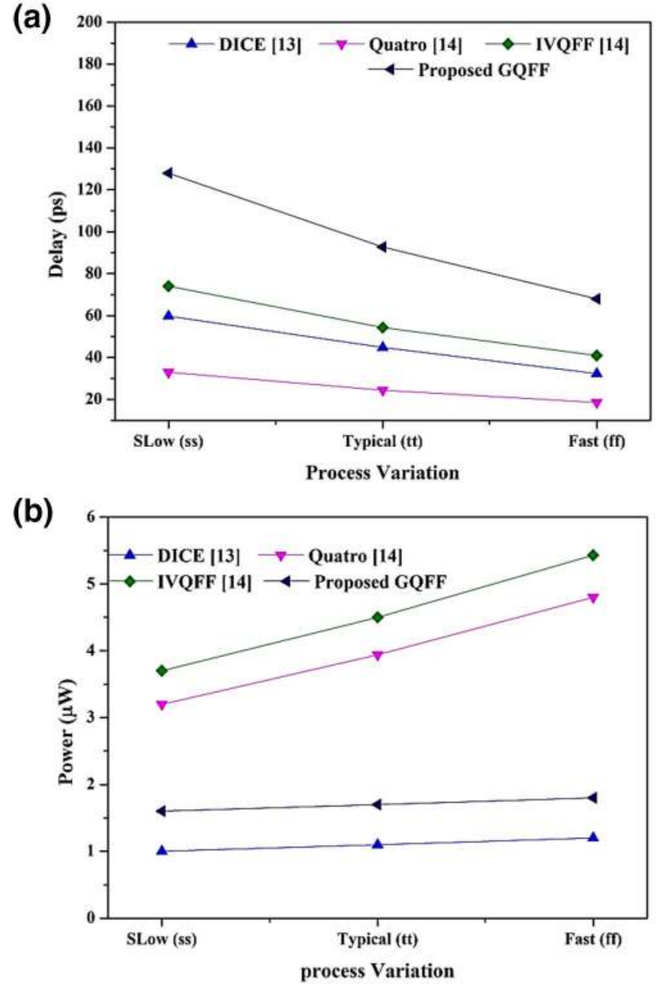


FIGURE 13 Process variation impact on (a) delay (CLK to Q) and (b) power dissipation. CLK, clock

5 | CONCLUSION

This study proposed a novel soft error resilience master-slave edge-triggered GQFF based on guard-gated Quatro cell and Muller C-element in 45 nm CMOS technology. The proposed GQFF mitigates the SNU and DNU issues of IVQFF through the parallel feeding of data inputs to the sensitive nodes of guard-gated Quatro cell. Due to the parallel feeding of inputs, the sensitive nodes present in the inverter stages of IVQFF (i.e. n1, n2 in the master and n3, n4 in the slave latch) are nullified. The Muller C-element connected as the output stage of GQFF masks the faults by taking high impedance state and preserves the correct output. The simulation result shows that the proposed GQFF has 100% SNU and 50% DNU tolerant capability than DICE, Quatro and IVQFF. The GQFF also consumes low power, that is, 62.4% less than IVQFF. However, the proposed design has a trade-off in delay and PDP. From MC simulations, it is observed that the GQFF is less inferior in terms of sensitivity towards PVT variations compared to IVQFF and performs better in terms of power consumption compared to Quatro and IVQFF.

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