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A Novel Phase Frequency Detector for a High Frequency PLL Design

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Abstract

A simple new phase frequency detector (PFD) is presented in this paper. This PFD use only 10 transistors, whereas a conventional PFD uses 54 transistors. It has been observed that the proposed PFD could operate up to frequencies about 4.6 times higher than that by conventional PFD. It has also been observed that the power dissipation is reduced by 99 %. In addition to these, area of the circuit has been reduced up to 73% when compared with conventional PFD. The phase noise of designed PFD has been reduced to - 133.4 dBc/Hz. Prototype has been designed in Cadence virtuoso environment and implemented using GPDK090 library of 180 nm technology with a supply voltage of 1.8 V. The reset process has been completely removed in this design thereby eliminating the blind zone and speeding up the acquisition process. The design has been proposed for high speed, low power and low jitter applications.

Keywords: Phase Locked Loop, Phase Frequency Detector, Dead Zone.

Nomenclature

PFD	Phase Frequency Detector
PLL	Phase Locked Loop
CP	Charge Pump
VCO	Voltage Controlled Oscillator
AM	Amplitude Modulation

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1. Introduction

Phase Locked Loop (PLL) is a class of circuit, used primarily in communication systems suitable for a wide variety of applications, such as AM radio receivers, frequency demodulators, multipliers, dividers, and as frequency synthesizers. Recent advances in integrated circuit design techniques have led to the development of high performance PLL which has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single chip.

The power consumption in the PFD contributes to a significant part of the total power consumption of a PLL. Therefore overall power consumption in a PLL can be reduced by minimizing the power consumption in PFD. The main challenge in the design of PFD is to obtain very high operating frequency with minimal power dissipation.

Different PFD designs have been proposed by many researchers for achieving high operating frequency however power consumption reported have been comparatively high [1-4]. In this paper a novel PFD architecture is proposed which is completely free from dead zone, dissipates very low power and operates at high frequency.

2. PLL Basics

Traditional block diagram of a PLL is shown in Fig.1. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals.

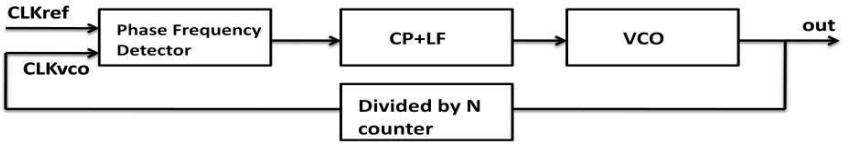

Fig.1. Basic Block Diagram of PLL

The phase frequency detector (PFD) is one of the main parts in PLL circuits. PFD produces an error output signal which is proportional to the phase difference between the phase of the feedback clock and the phase of the reference clock. The Charge Pump (CP) is another important part of PLL. CP converts the phase or frequency difference information of two input signals into a voltage which is used to tune a Voltage Controlled Oscillator (VCO) toward reference input frequency.

Thus, the Loop Filter (LF) is necessary to generate necessary control signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD, if the PFD generates an up (UP) signal, the VCO speeds up. On the contrary, if a down (DN) signal is generated, the VCO slows down. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, thereby forming the closed loop frequency control system.

3. Conventional Architecture

The traditional PFD architecture is shown in Fig. 2. The main drawbacks of this design include non zero dead zone, higher power consumption while operating at high frequency, lower maximum operating frequency and larger area due to many number of transistors.

It consists of two edge triggered resettable D flip-flops with their D inputs tied to logical ONE and one AND gate. Inputs CLK_{ref} and CLK_{vco} act as clock of flip-flops. Assuming initially UP=DN=0, when CLK_{ref} goes high, UP rises. If this event is followed by a rising transition on CLK_{vco}, DN also goes high and the AND gate resets both

flip-flops. UP and DN are simultaneously high for a short time but the difference between their average values represents the input phase or frequency difference.

Mozhgan Mansuri et al. have illustrated the non ideal behavior with the reference clock CKL_{ref} leading the output clock CLK_{vco}, causing an UP output [1]. As the input phase difference is near 2π, the next leading edge CLK_{ref} arrives before the D-flip-flops are reset due to the finite reset delay. The reset overrides the new CLK_{ref} edge and does not activate the UP signal. They have also reported that t_{reset} is determined by the delay of logic gates in the reset path and is not a function of input frequency [1]. Hence the new design has been developed based on the fact that operating frequency of the PFD or PLL could be improved if it was possible to eliminate the reset delay. Hence the proposed design concentrates on eliminating reset delay so that the dead zones are completely removed.

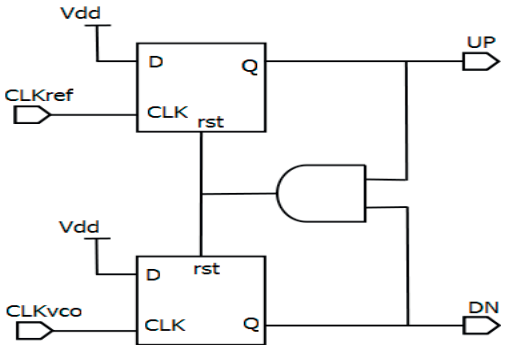

Fig.2. Implementation of Conventional PFD

4. Proposed PFD Design

In order to increase the operating frequency of the PFD, reset path is eliminated by adding pass transistor logic. The proposed PFD (PFD1) uses only 10 transistors which reduces the power consumption and area of the PLL.

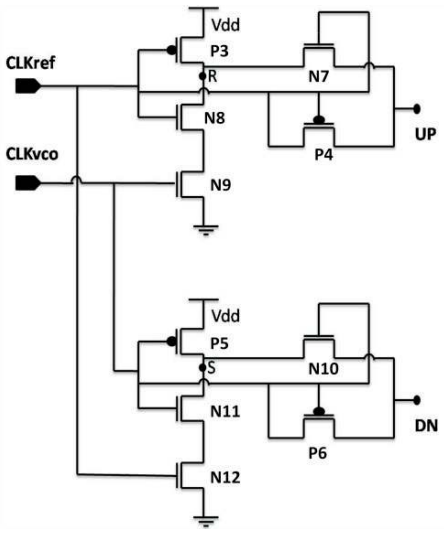

Fig.3. Schematic of Proposed PFD1

Schematic of the designed PFD is shown in Fig 3. P3 through P6 are PMOS transistors while N7 through N12 is NMOS transistors. Principle of operation is explained below. Initially the CLK_{ref} and CLK_{vco} signals are at logic zero. At the rising edge of CLK_{ref}, N7, N8 and N12 turns on and the UP signal goes to logic high. At the rising edge of CLK_{vco}, N9, N10 and N11 turn on forcing DN to go high. When both UP and DN are high, the logic levels at points R and S in Fig. 3 are pulled down to logic zero making UP and DN to go to logic zero without any delay for reset.

5. Simulation Results

5.1. Transient Response of PFD1

Timing diagrams for the proposed PFD is shown in Fig.4. It can be observed from Fig. 4 that when CLK_{vco} is lagging CLK_{ref} by 3ns, the UP signal goes high and whenever both are high immediately both UP and DN signal go down. Thus the designed PFD1 acts as a phase frequency detector like a conventional PFD.

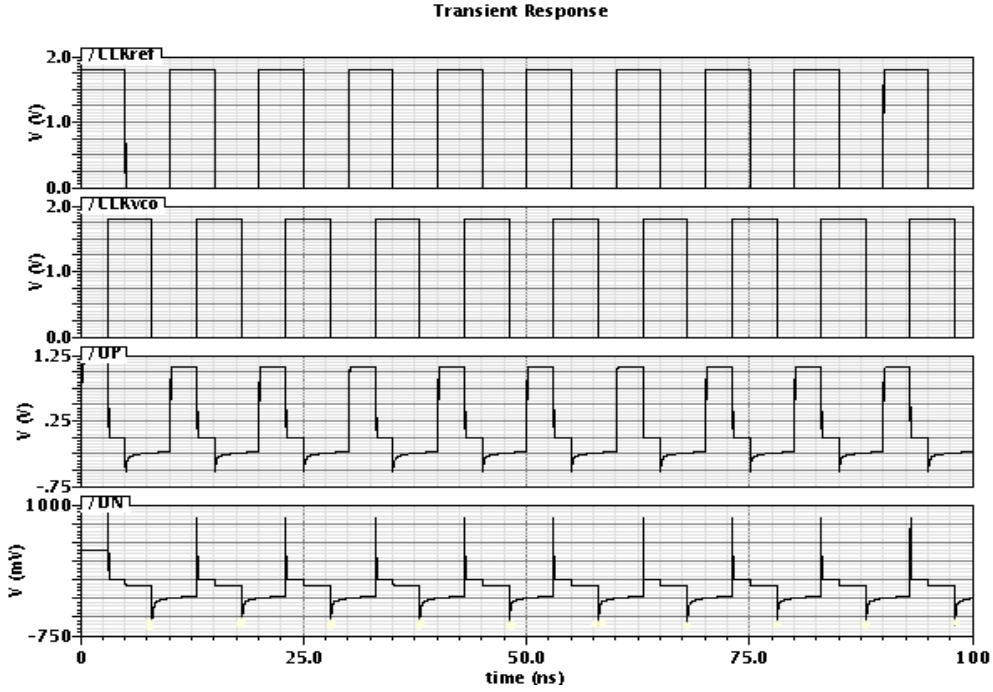

Fig.4. Timing diagram of PFD with CLKref leading CLKout by 3ns, so the pulse width of UP signal will be high for 3ns

5.2. Phase Characteristics

The average output value of the PFD1 versus the phase difference between the CLK_{ref} and CLK_{vco} signal for PFD1 is presented in Fig.5. It can be observed that dead zones are completely eliminated in this design as it does not depend on the reset signal but only on the arrival of CLK_{ref} and CLK_{vco} signals.

Now considering the linearity property, it can be observed from Fig.5 that the proposed PFD1 is almost linear throughout the period. It may also be noted that the proposed design has higher range of linearity when compared with the PFD reported in literature [2].

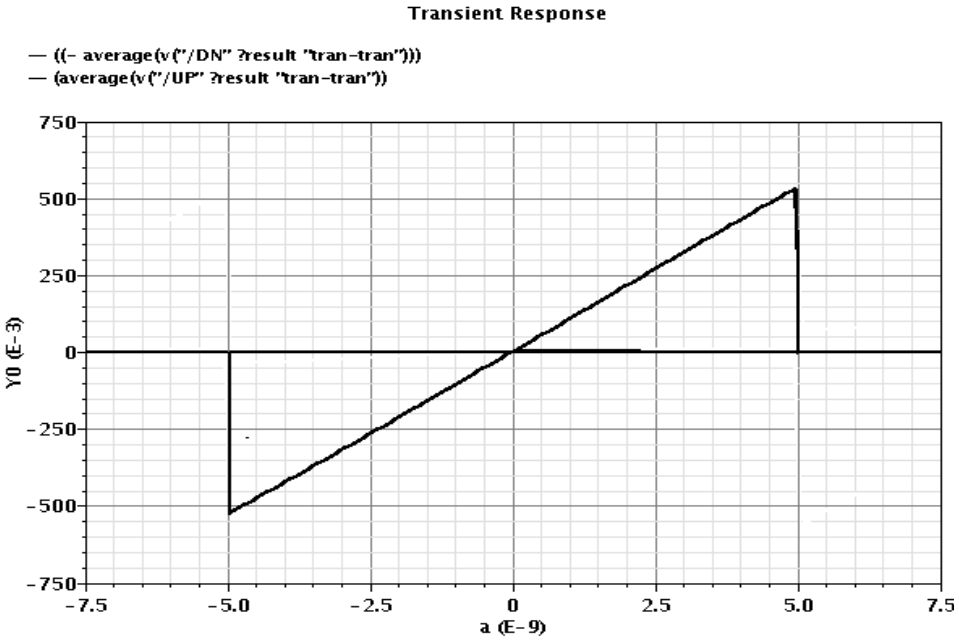

Fig.5. Phase Characteristics of PFD1

5.3. Phase Noise Analysis

Random variation in the phase of the signal is termed as phase noise. It is the frequency domain representation of rapid, short term fluctuations in the phase of the wave, caused by time domain instabilities known as jitter.

A phase noise simulation of proposed PFD1 is shown in Fig.6 with both CLK_{ref} and CLK_{out} kept as 100 MHz and both are in same phase as well. Noise is contributed to the PFDs from different sources such as dead zone, transistors, and reset time delay. It can be observed that proposed PFD1 has lower values of phase noise of -133.4 dBc/Hz at 1 MHz offset. The phase noise of conventional PFD is -122 dBc/Hz [2]. Hence it can be observed that the proposed design is suitable for low jitter applications.

5.4. Maximum Operating Frequency

Maximum operating frequency [2] as a function of supply voltage has been presented in Fig. 7 for conventional PFD and proposed PFD1. It can be observed from fig.7 that the maximum operation frequency of the traditional PFD is 800 MHz, while that for PFD1 is 3.72 GHz at a supply voltage of 1.8 V.

5.5. Area Requirement

The proposed PFD1 is implemented using GPDK090 library of 180nm technology. The chip layout of PFD1 is presented in Fig.8. Final placement area of PFD1 consists of 15.0356 μm width by 8.13 μm length (Area= 122 micron^2).

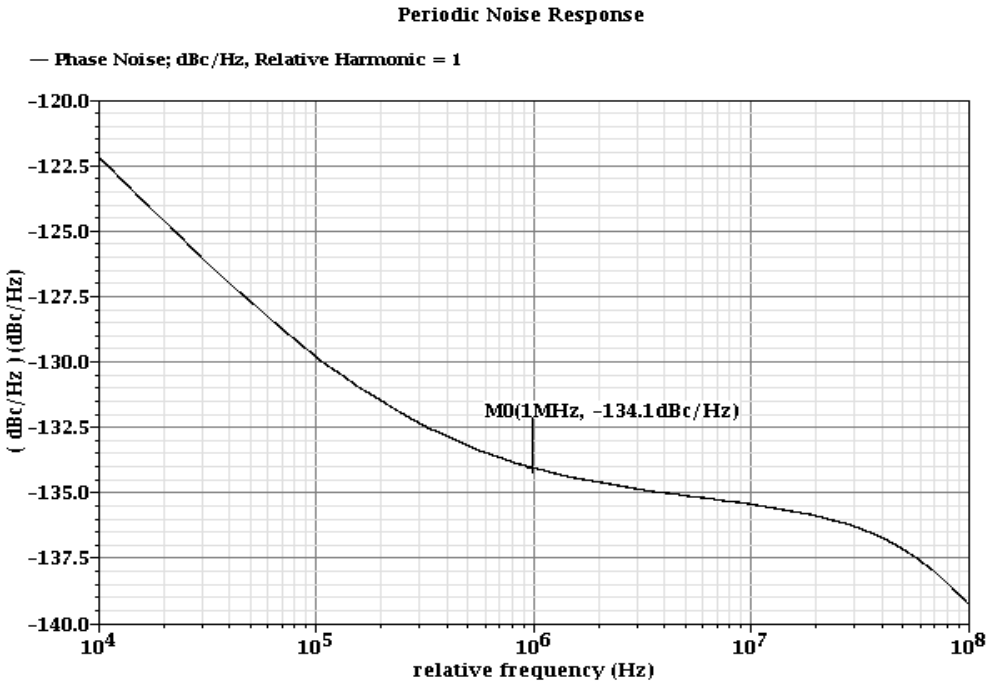

Fig.6.Phase Noise Analysis of PFD1

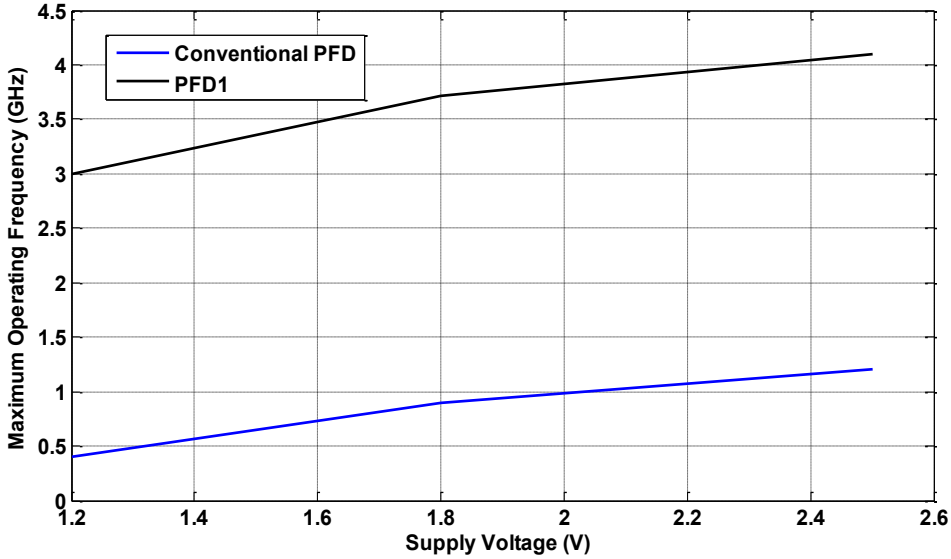

Fig.7. Maximum Operating Frequency as a function of supply voltage for conventional PFD and proposed PFD1.

5.6. PLL Analysis

The effectiveness of the proposed design has been verified by building a PLL with proposed PFD1. Charge Pump, Loop Filter, CMOS Voltage Controlled Ring Oscillator and divide by 8 counter have been implemented in Cadence virtuoso environment using GPDK090 library of 180 nm technology with a supply voltage of 1.8V.

Measured frequency acquisition characteristics of the PLL using PFD1 is presented in Fig. 9. To analyze the frequency acquisition characteristics, a reference clock of 100 MHz is supplied. In this figure it can be observed that that the acquisition range of PLL using PFD1 is 4.75 µs which is better than the PLL in reported literature [6]

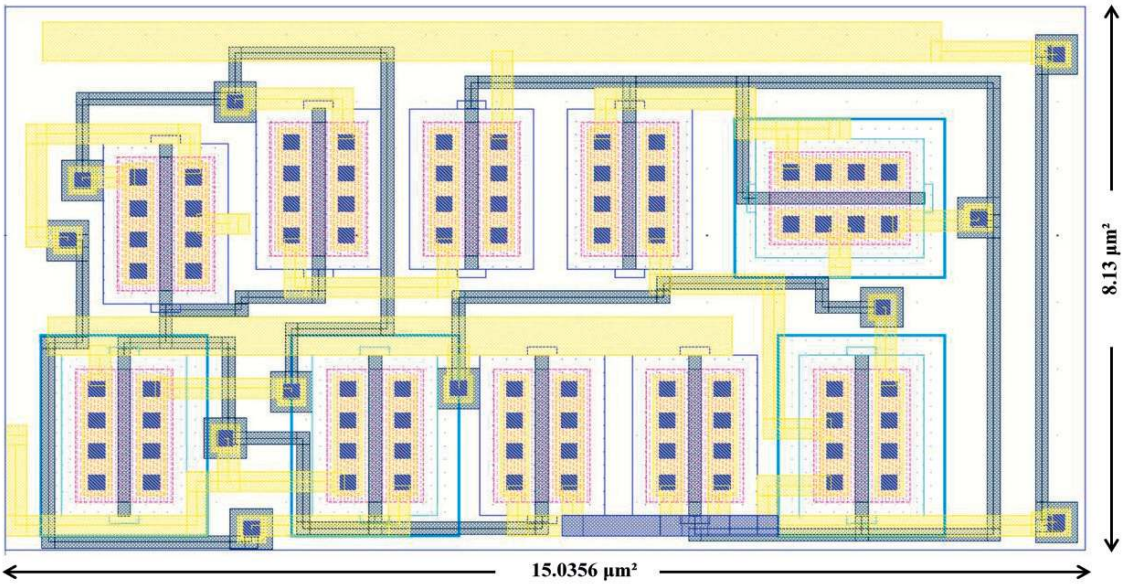

Fig.8. Layout of PFD1

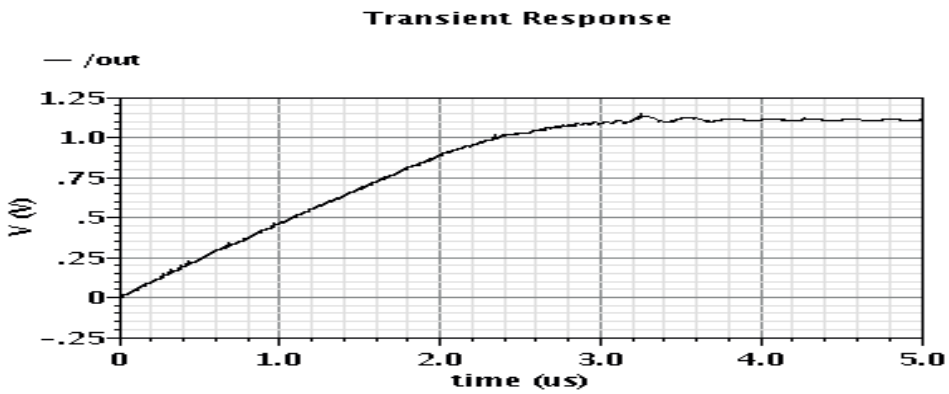

Fig.9. Response of PLL acquisition time using PFD1

6. Discussion

The performance comparison of different PFD architectures with different design parameters is presented in table I. The PFD1 is completely free from Dead Zone and the Reset time of the PFD1 is Zero.

Table 1. Simulated PFD Output Comparison.

An example of a column heading	Conventional PFD	PFD1	[3] 2010	[2] MPt-PFD	[7]	[8]
Power consumption in μW	1650	10.34	496	10	-	8
No. of Transistor	54	10	36	16	19	4
Maximum Operating Frequency in GHz	0.8	3.72	2.94	1.5	1.2	5
Reset Time in ns	0.152	0	0.156	0	0	0
Dead zone in ps	70	free	61	free	≤ 10	20
Phase noise dBc/Hz@1M Hz	-122	-133.4	--	-131.5	-	-
Area in μm^2	452	122	--	--	-	-

PFD1 uses only 10, whereas a conventional PFD uses 54 transistors. Maximum operating frequency of PFD1 is 3.72 GHz which is higher than other reported PFDs [2, 3]. It can also be seen that power dissipation is reduced by 99 % and area is saved up to 73 % in PFD1 when compared with conventional PFD. Phase noise is also reduced significantly to -133.4 dBc/Hz@ 1 MHz when compared with conventional PFD. It is also observed that acquisition range of PLL using proposed PFD1 is 4.75 μs which is better than that (22.5 μs) of the PLL reported in [6].

7. Conclusion

A simple and novel PFD designed with 10 transistors has been proposed in this paper. The significant advantage of this design is that the dead zone is completely eliminated by removing the reset path. It has been observed that these PFD1 could operate up to frequencies 4.6 times higher than that of conventional PFD. The acquisition time of a PLL implemented with this PFD1 is very less (4.6 μs) when compared with other PLL reported in literature. Hence Pit is proposed that PFD1 is suitable for low jitter, zero dead zone, high speed and low power applications.

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