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A single phase grid connected hybrid multilevel inverter for interfacing photo-voltaic system

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Abstract

This paper introduces a new single phase hybrid multilevel inverter with a minimum number of switches for a Photovoltaic application. A Perturb and observe maximum power point tracking is used for tracking maximum power from solar panel. A boost converter is used for boosting the generated voltage because proposed inverter operates at the asymmetric condition. The proposed inverter is the combination of reduced switch topology and cascaded H-Bridge topology. Two types of Phase Disposition carrier arrangement with sinusoidal reference is utilized for generating the gating pulses for proposed inverter. It generates a 15-level output voltage with 8.12% of total harmonic distortion.

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Keywords: MPPT; boost converter; hybrid multilevel inverter; pulse width modulation;single phase grid.

1. Introduction

In present days, the utilization of renewable energy is more advantageous in both economically and environmentally [1]. The Photovoltaic (PV) system provides secure, clean and reliable in renewable energy sources with the added advantageous of zero fuel cost, no moving parts, low running cost, minimum maintenance and long-life time [2]. These points of interest make the utilization of PV in many places and also in off-grid installations. Multilevel Inverter (MLI) topologies are proved as substantial global attention by the researchers and front-end industries in various medium and high power

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applications because of their ability to generate high quality of output waveforms, reducing switching stress across the switches, and reducing switching frequency [3].

In recent years, many topologies have emerged in the field of grid connected MLI in renewable energy application [5]. The basic classification of MLI is Diode-Clamped MLI (DCMLI), Flying Capacitor (FCMLI) and Cascaded H-Bridge MLI (CHBMLI) [6]. Although these types of basic MLIs are noticeable in high power applications regardless they have few demerits like components count and voltage balancing problem expect CHBMLI [7,8,9]. To overcome this problem, reduced switch MLI topologies are developed in past decades [5]. Many topologies in MLI are ended with DC source, but only a few topologies are integrated with PV applications.

In this paper, a new single phase grid connected hybrid MLI is developed and PV panel with boost converter utilized instead of DC sources in MLI. The proposed topology requires less number of switches and sources when compared to basic types MLI. Perturb and Observer (P&O) method is utilized in Maximum Power Point Tracking (MPPT) processes lead to track the maximum voltage and current from the PV panel. The hybrid topology is tested sinusoidal reference with the two different carrier arrangements such as Phase Disposition (PD) and Variable Frequency Phase Disposition (VFPD) and the results are compared with each other.

2. Proposed multilevel inverter

The proposed MLI topology is the combination of Switched DC Source (SDCS) MLI [7] and full bridge inverter which is shown in Fig. 1.a. The hybrid MLI produces an output voltage level using the appropriate arrangement of the switches and voltage sources. The output voltage levels vary depending on the DC source value. Although the proposed topology can be extended to any number of voltage levels with the addition of corresponding switches and DC sources. The generalized structure of proposed MLI is shown in Fig. 1.b. The hybrid topology requires an isolated DC source which is best suited for PV applications. The hybrid MLI operates as asymmetric conditions lead to increase the output voltage level. SDCS MLI topology can operate as both symmetric and asymmetric conditions but in this paper it operates as an asymmetric condition. The value of full bridge inverter DC source is half of the value of first DC source in reduced switch topology.

The value of DC sources in SDCS topology is followed as a natural sequence of numbering. So, proposed MLI follows the following formula for calculating number of DC source, number of switches and number of level.

Number of DC source = $\mathrm{m + n}$ (1)

Number of switches = $[\mathrm{4m + (2n + 2)}]$ (2)

Number of output voltage level = $[(\mathrm{n^2 + n + 1}) \times \mathrm{2m}] + 1$ (3)

$$\text{The value of DC source} = \begin{cases} V_{dcj} = jV_{dc}, j = 1,2,3 \dots .k \\ V_{dcx} = \frac{V_{dc1}}{2} \end{cases} \quad (4)$$

When operating the SDCS MLI in asymmetric condition, the placement of asymmetric value DC source at the appropriate place is very much important to produce the desired output voltage level. The placement of DC source at the exact position is considered by the following equation

For Odd number of DC source

$$V_{dcj} = \begin{cases} (2j-1)V_{dc}, & 1 \le j \le ((k+1)/2) \\ 2(k+1-j)V_{dc}, & [(k+3)/2] \le j \le k \end{cases} \quad (5)$$

For Even number of DC source

$$V_{dcj} = \begin{cases} (2j-1)V_{dc}, & 1 \le j \le (k/2) \\ 2(k+1-j)V_{dc}, & [(k+2)/2] \le j \le k \end{cases} \quad (6)$$

Here ‘n’ and ‘m’ represents the number of DC sources in SDCS MLI topology and number of DC sources in full bridge inverter respectively. The value of ‘m’ should be always 1.

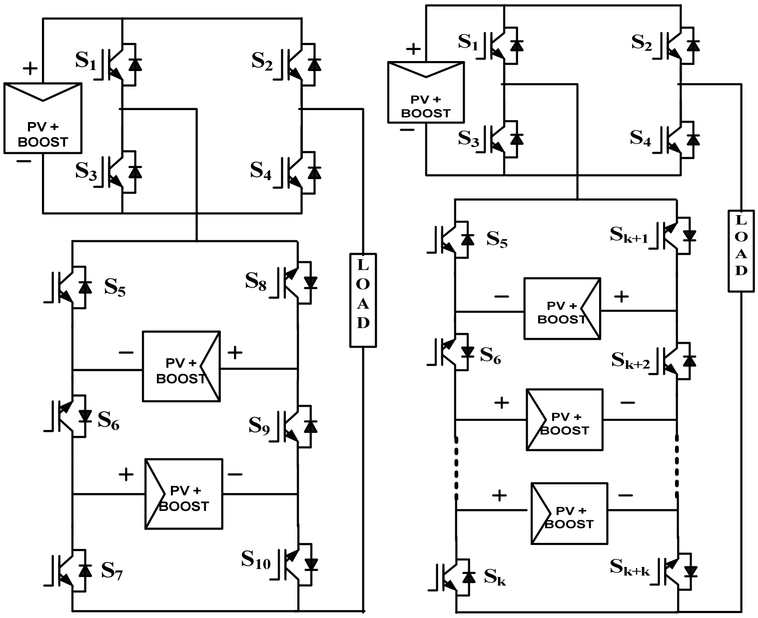


Fig. 1. (a) Proposed hybrid MLI; (b) Generalized topology for proposed hybrid MLI

The value of ‘n’ should vary from 0 to ∞. The hybrid topology modes of operation for generating positive levels are explained in table 1. From that table 1, it is clearly justified when the presence of full bridge inverter odd voltage levels can generate in both polarities whereas the even voltage levels in both polarity can generate in the absence of full bridge inverter. The count of conducting switches per voltage level is less when compared to conventional CHBMLI. Separate PV models are associated with each DC source of proposed MLI through the individual DC-DC Boost Converter. The boost converter is utilized for boosting the output voltage of PV panel to the required level.

Table 1. Switching table of proposed MLI

Modes	On state Switches	Voltage level
1	S_2, S_3, S_8, S_9,S_{10}	$0V_{dc}$
2	S_2, S_3, S_8, S_9, S_{10}	$1V_{dc}$
3	S_1, S_2, S_6, S_7, S_8	$2V_{dc}$
4	S_2, S_3, S_6, S_7, S_8	$3V_{dc}$
5	S_1, S_2, S_5, S_6, S_{10}	$4V_{dc}$
6	S_2, S_3, S_5, S_6, S_{10}	$5V_{dc}$
7	S_3, S_4, S_6, S_8,S_{10}	$6V_{dc}$
8	S_3, S_2, S_6, S_8, S_{10}	$7V_{dc}$

3. Design Specifications

The PV panel output voltage is connected MLI through boost converter. The PV panel rating is 80 W. Four PV panel is utilized for generating the 15-level output voltage. So, the inverter is operated at 320 W.

The PV panel is designed at standard test condition (STC) and the equation is followed as

Output current $I_A = N_p I_{sc} - N_p I_o \left[exp\left(\frac{V_A + I_A R_s}{n N_s V_t}\right) - 1\right]$ (7)

The detail explanation of PV modeling and P&O MPPT technique is described in [1] and [10] respectively. The boost converter is designed based on the following formulas

Duty cycle $(D) = 1 - \left(\frac{V_{in}}{V_{out}}\right)$ (8)

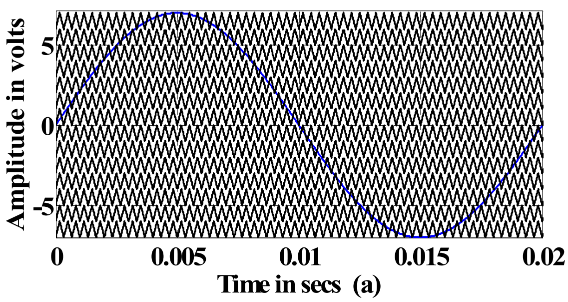
Inductor $(L) = \frac{V_{in} \times D}{\Delta_{iL} \times f}$ (9)

Capacitor $(C) = \frac{I_o \times D}{\Delta_{vo} \times f}$ (10)

The parameters $\Delta_{iL}, and\ \Delta_{Vo}$ represent the ripple inductor current and ripple output voltage. The parameters $V_{in} and\ V_o$ represent input voltage and output voltage.

4. Switching Scheme

Different types of pulse width modulation techniques are explained in [11]. Sinusoidal Multicarrier Pulse Width Modulation is utilized for generating the switching pulse to proposed topology. The proposed topology is tested with two different carrier arrangements such as PD and VFPD. For 15 level output voltage, 14 carriers are needed. In that, 7 carriers are above zero references and remaining 7 carriers are placed in below zero references. The PD carriers are each in phase with the same amplitude and same frequency as shown in Fig. 2.a. The VFPD carriers are each in phase with the same amplitude but the alternative carriers are in different frequency as shown in Fig.2.b. The odd carriers are operated at 3000 Hz whereas the even carriers are operated at 1500 Hz. The positive carriers are placed above the zero reference axis and negative carriers are placed below the zero reference axis. The switching pulses are generated by continuously comparing the reference signal with triangular carriers. In that comparison, the carriers above zero reference provide a positive signal if the reference signal is greater than the carrier signal and zero otherwise. Also, the carriers below zero reference provide zero if the reference single is greater than the carrier signal and negative signal otherwise. Then the switching pulses for the switches are generated by the combination of logic gates based on the switching table 1.



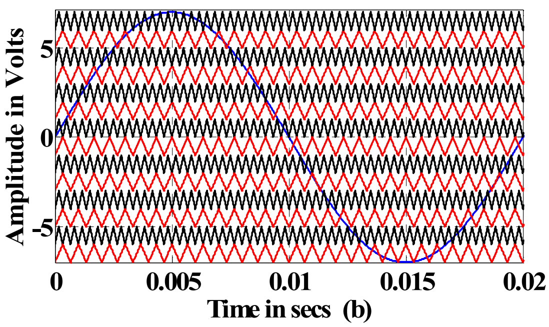


Fig. 2. Carrier arrangements (a) PD technique; (b) VFPD technique

5. Simulation Results

The proposed single phase hybrid MLI integrated with PV panel is simulated for 15-level output waveform suing MATLAB/Simulink. The hybrid MLI has isolated DC sources. In this simulation, for each DC source the separate PV panel with boost converter is considered. So, the P&O MPPT technique is used for tracking the maximum voltage and current. Each PV panel rating is 80 W with the maximum voltage of 18.33 V. The topology requires different voltage rating because it acts as an asymmetric condition. Here, four panels with three different ratings of boost converter are utilized. So, the overall inverter is operated at 320 W. The total DC bus voltage should be always greater than $\sqrt{2}$ to injected current into the grid; otherwise, the current will be injected from the grid into the inverter [8]. So, the full bridge inverter DC voltage is set to 65 V. The remaining DC voltage is set to 130 V and 260 V. Based on these voltage ratings, boost converters are designed because the PV panel produces maximum 18.33 V. The Boost converter switching frequency is 24 KHz. The modulation index is main parameter to maintain a 15-level output voltage. In this inverter the required output voltage will maintain in the range of modulation index 0.86 to 1. Boost converter output voltage of each source is shown in Fig. 3. Fig. 4.a and 4.b. shows the simulated 15-level output voltage and their FFT plot for PD technique. Fig. 5.a and 5.b. shows the simulated 15-level output voltage and their FFT plot for VFPD technique.

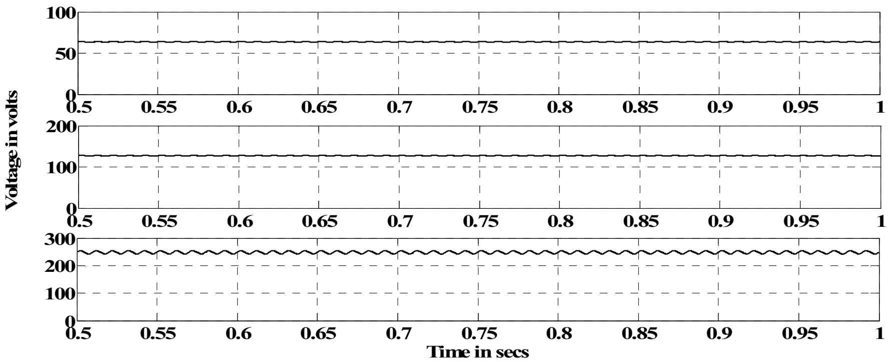


Fig. 3. Boost Converter output voltage waveform

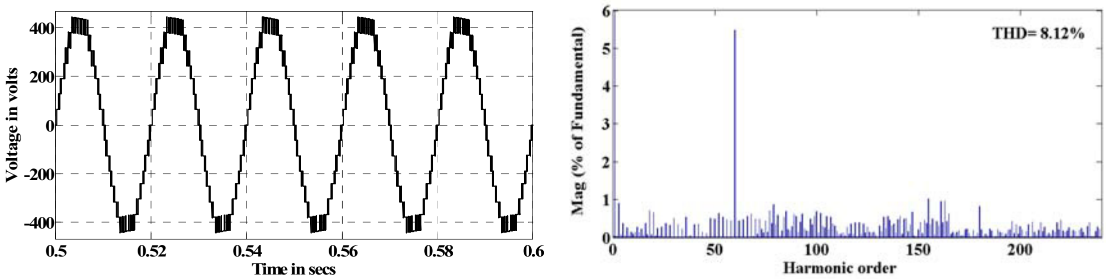


Fig. 4. PD technique (a) output voltage; (b) FFT plot

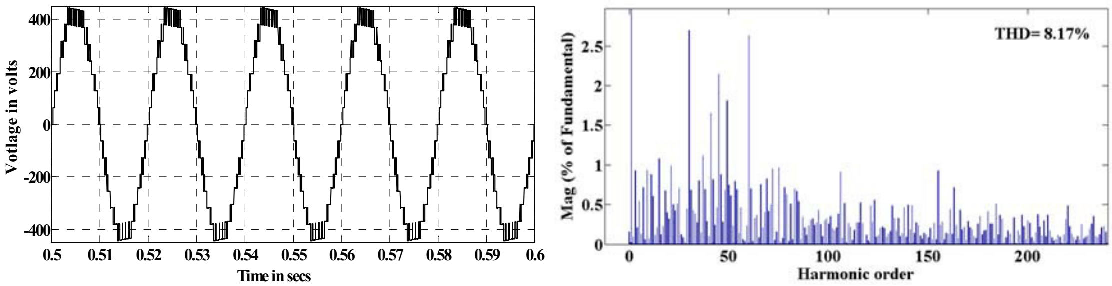


Fig. 5. VFPD technique (a) output voltage; (b) FFT plot

Fig. 6 shows the grid voltage and inverter current waveform with filter inductance. The filter inductance is calculated using the following formula

Filter Inductance $L_f = \frac{V_{f_{sw}}}{I_{f_{sw}}}\left(\frac{1}{2\pi f_{sw}}\right)$ (11)

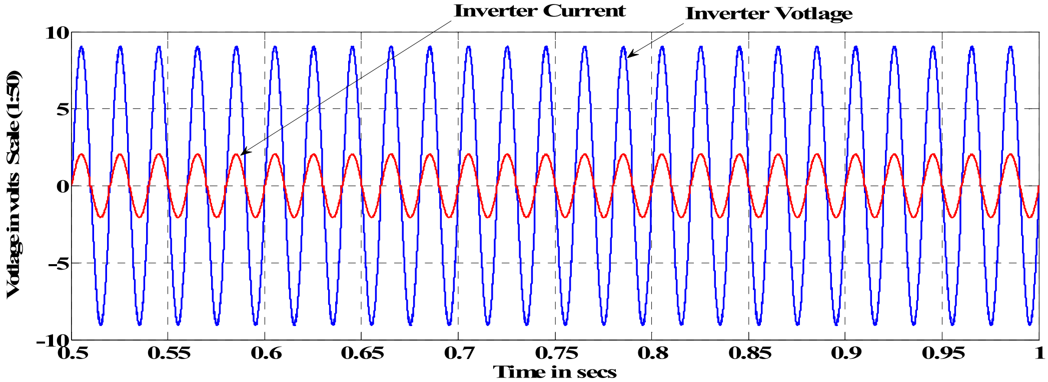


Fig. 6. MLI output voltage with filter inductance waveform

6. Conclusion

This paper has presented a single phase grid connected MLI with a reduced number of switch count and DC sources integrated with PV panel. Perturb and Observer method MPPT method is utilized. The isolated DC source is replaced by 80 W PV panel with boost converter and it boosting voltage based on the asymmetric conditions values. Sinusoidal pulse width modulation technique is used for generating the switching pulses. Two different Phase Disposition techniques are simulated using MATLAB/Simulink. The overall system is operated at 320 W. From the results it is concluded that proposed hybrid MLI is well suited for PV based grid application.

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