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A Single Phase Reduced Device Count Multilevel Inverter Topology Using MCPWM for Renewable Energy Systems

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Abstract

In this paper, a new hexagonal switch cell multi level inverter (HSCMLI) is proposed for the PV system which offers reduced number of devices as compared with conventional multi level inverter (MLI) topologies. Thereby, reduces the size and complexity of the overall PV system. For performance analysis of HSCMLI in PV system various constant frequency multi-carrier pulse width modulation (MCPWM) generating methods are proposed to enhance the fundamental root mean square (RMS) voltage, Peak voltage and reduce total harmonic distortion (THD). The proposed strategy can be applied to PV system to effectively reduce the odd harmonics with reduced size and complexity for grid application.

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Keywords: Solar panels; Maximum power point trackers; DC-DC power converters; DC-AC power Converters; Power conversion; harmonics.

1. Introduction

Inverter plays a crucial role in generating alternating signals and improves power quality for alternating sources [1]. This DC-AC control change is the key innovation in the present day setup of generation, transmission, distribution, and usage of electric power. Inverters assume a significant part in VF drives, cooling, continuous power supplies, enlistment warming, high voltage dc control transmission, electric vehicle drives, static VAR compensators, dynamic channels, adaptable AC transmission frameworks and dc source use. Capacitors, batteries and renewable vitality voltage sources can be utilized as the numerous input dc levels.

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Control switches are controlled in order to sum up these different dc levels [2] to accomplish high voltage at the output, while the evaluated voltage of the power semiconductor switches relies upon the rating of the dc voltage sources to which they are associated. Consequently, as a rule, the voltage stress on a power switch [3] is much lower than the specified voltage. In this paper, the proposed PV configuration it uses constant switching frequency multi-carrier PWM method with phase disposition (PD), Inverse phase disposition (IPD), Phase opposition disposition (POD), Alternative phase opposition disposition (APOD), carrier overlap (CO) MCPWM for generating gate pulses to trigger inverter switches to examine the fundamental RMS voltage and THD of the inverter.

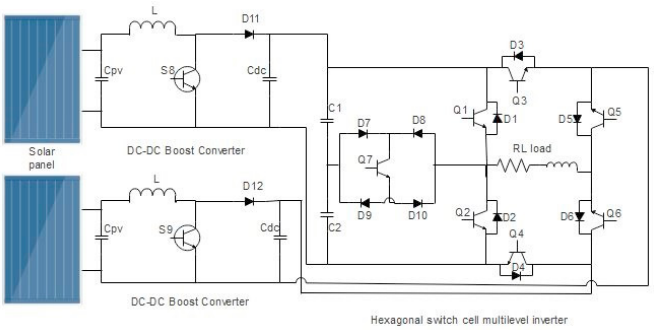

Fig.1. Proposed Inverter Topology for PV

2. Single phase Hexagonal Switch cell Multi level Inverter

The single phase HSCMLI is represented in Fig. 2. The circuit is intended for generating 7, 9 and 11 level output consisting of only 7 switches [4]. It consists of two DC sources, two capacitors, the auxiliary switch for controlling and four diodes for connecting the auxiliary switch to hexagonal switch cell form Q1-Q6. It can function both in symmetrical and asymmetrical configuration. The switching states of 7,9 and 11 level HSCMLI is as shown in Table. 1, Table. 2 and Table. 3 respectively. For generating 7 level during conduction state 1 for generating positive voltage level of $+1V_{dc}$ switches Q4 and Q7 conduct along with diodes D6, D7, D10. During conduction state 2 for generating positive voltage level of $+2V_{dc}$ switches Q1 and Q4 conduct along with diode D6. During conduction state 3 for generating the positive level voltage of $+3V_{dc}$ switches Q1, Q4, Q5 conducts. During conduction state 4 for generating the negative level voltage of $-1V_{dc}$ switches Q3 and Q7 conduct along with diodes D5, D8, and D9. During conduction state 5 for generating the negative level voltage of $-2V_{dc}$ switches Q2 and Q6 along with diode D5 conducts. At last during conduction state 6 for generating the negative level voltage of $-3V_{dc}$ switches Q2, Q3 and Q6 conducts. Thus, for a two source MLI, V_0 can be any of the 7 levels $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$.

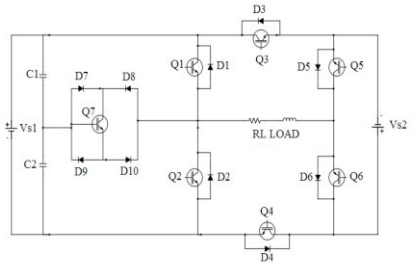

Fig. 2. Hexagonal switch cell multi level inverter [4].

Table 1.Seven level HSCMLI switching states [4]

levels	Switches "ON"	Diodes "ON"
1	Q4, Q7	D6, D7, D10
2	Q1, Q4	D6
3	Q1, Q4, Q5	-
0	-	-
-1	Q3, Q7	D5, D8,D9
-2	Q2, Q6	D5
-3	Q2, Q3, Q6	-

Table 2.Nine level HSCMLI switching states [4]

levels	Switches "ON"	Diodes "ON"
1	Q4, Q7	D6, D7, D10
2	Q4, Q5	D2
3	Q4, Q5, Q7	D7, D10
4	Q1, Q4, Q5	-
0	-	-
-1	Q3, Q7	D5, D8,D9
-2	Q3, Q6	D1
-3	Q3, Q6, Q7	D8, D9
-4	Q2, Q3, Q6	-

Table 3.Eleven level HSCMLI switching states [4]

levels	Switches "ON"	Diodes "ON"
1	Q4, Q7	D6, D7, D10
2	Q1, Q4	D6
3	Q4, Q5	D2
4	Q4, Q5, Q7	D7, D10
5	Q1, Q4, Q5	-
0	-	-
-1	Q3, Q7	D5, D8, D9

-2	Q2, Q3	D5
-3	Q3, Q6	D1
-4	Q3, Q6, Q7	D8, D9
-5	Q2, Q3, Q6	-

The earlier thought can be used to different MLI topologies using numerous sources also. The components required of generating 7 levels in MLI when match up to other conventional MLI as shown in Table 4. By using those equations the components required for various MLI topologies with HSCMLI is shown in Table 5. It indicates that by comparison, HSCMLI uses only 20 semiconductor devices for generating 7 levels whereas for NPCMLI it uses 96 such components, FCMLI uses 68 such components and CHBMLI uses 36 components. The two sources in HSCMLI can be replaced with converters fed by solar PV of 250 W for effective outcome.

Table 4. Apparatus requirements for single phase MLI [4]

S.No	Devices	HSC MLI	NPC MLI	FC MLI	CHB MLI
1	Main switches	(N+19)/4	2(N-1)	2(N-1)	2(N-1)
2	Main diodes	N+1	2(N-1)	2(N-1)	2(N-1)
3	DC bus capacitor	(N+7)/4	(N-1)/3	(N-1)/3	(N-1)/2
4	Flying capacitor	0	0	(N-1)* (N-2)/2	0
5	Total	(3/2)* (N+5)	(N-1)* (3N+7)/3	(N-1)* (3N+20)/3	(9/2)* (N-1)

Table 5. Assessment of similar seven-level MLI topologies

Components	HSC MLI	NPC MLI	FC MLI	CHB MLI
Main switch	6	16	16	16
Secondary switches	1	0	0	0
Diode	11	72	16	16
Capacitor	2	8	36	4
Total	20	96	68	36

3. Multi Carrier Pulse Width Modulation

In PWM, the magnitude of the output voltage can be controlled with a regulating waveform. Diminished filter necessities to reduction of harmonics and the control of the output voltage magnitude are the hindrance of PWM [5]. Control of the switches for sinusoidal PWM requires a reference called control signal and a carrier signal, which is a triangle wave signal that controls the exchanging recurrence in switches. The guideline of sinusoidal bipolar PWM demonstrates a sinusoidal reference signal and a triangular carrier signal. The instant rate of the sine reference is better than the triangular carrier, the output is at $+V_{dc}$, and when the reference is a smaller amount than the carrier, the output is at $-V_{dc}$.

$$V_0 = +V_{dc1} \quad \text{for } V_{reference} > V_{carrier} \tag{1}$$

$$V_0 = -V_{dc1} \quad \text{for } V_{reference} < V_{carrier} \tag{2}$$

In multi-carrier, PWM technique different stages of carrier signals are evaluate with the sinusoidal reference signal which operates at the fundamental frequency of the system to generate pulses to switching devices with respect to inverter voltage levels. In PWM for N level inverter (N-1), carriers are used. For inverter analysis purpose multi-carrier PWM strategy is used with constant and variable switching frequency. Modulation index of a sine multi-carrier PWM can be given as

$$M_a = \frac{A_m}{(m-1)A_c} \tag{3}$$

The modulation frequency is defined as a ratio of the carrier frequency to that of the modulation frequency used. The multi-carrier PWM techniques [6] are categorized in to phase sifted and level shifted PWM. In level shifted PWM a detailed analysis are done in HSCMLI using different constant frequency PWM generating techniques [7] like In phase disposition (PD), Inverse phase disposition (IPD), Phase opposition disposition (POD), Alternative phase opposition and disposition (APOD), carrier overlap (CO)

3.1. Invariable switching frequency pulse width modulation

In phase disposition (PD) in-phase carrier signals are level shifted and they operate on a frequency of 2 kHz as shown in Fig .3. The level shifted carrier signals are evaluate with the reference signal which is at a fundamental frequency. Here different levels of the output wave are observed and muxed to produce the pulses for triggering inverter switches.

In inverse phase disposition (IPD) PWM technique the level shifted carrier signals are 180˚ out of phase when compared to PD or it is the inverse of PD as shown in Fig .4.

In phase opposition disposition (POD) technique all carrier waveforms above zero reference value are in phase and the carrier wave below reference value is 180˚ phase shifted from carriers above zero references as shown in Fig .5.

In alternative phase opposition disposition (APOD) all carrier waves above and zero references are shifted 180˚ to each level of carriers in an alternative manner to generate PWM signal as shown in Fig .6.

In carrier overlap (CO) technique, each carrier is level shifted in which it has same frequency and amplitude. The overlapping distance between each carrier should be 50% of its amplitude as shown in Fig .7.

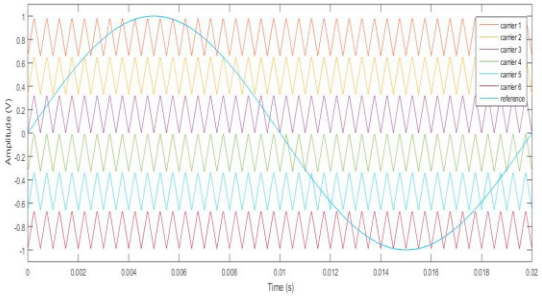

Fig. 3. Multi carrier PWM frequency spectrum of PD.

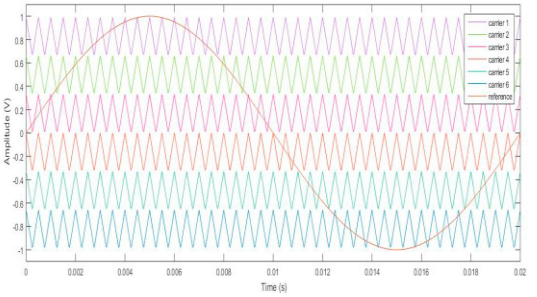

Fig. 4.Multi carrier PWM frequency spectrum of IPD.

4. Results and Discussion

To investigate the proposed scheme a simulation replica for a single phase 7 level HSCMLI is implemented in MATLAB/simulink. The HSCMLI generates output voltage of 250V when an input voltage of 115V fed to two sources in inverter. Simulation model tests are conceded to approve the anticipated idea. The main idea of this work is to find the best performance of the inverter operating under various constant frequency PWM techniques. The

performance constraints considered for determining in the inverter performance are RMS voltage, Peak voltage, THD [8]. The HSCMLI is connected with LC filter to reduce the ripples across load operating with parameters of inductor and capacitor 100mH and 300μF with single phase RL load 33Ω and 53mH.

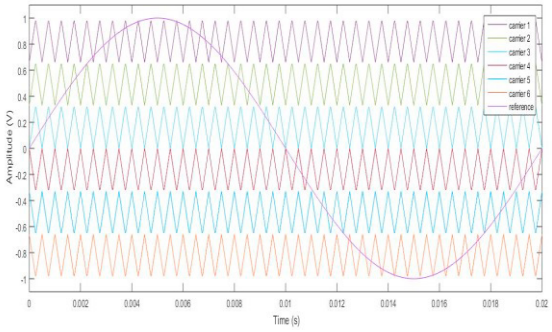

Fig. 5. Multi carrier PWM frequency spectrum of POD.

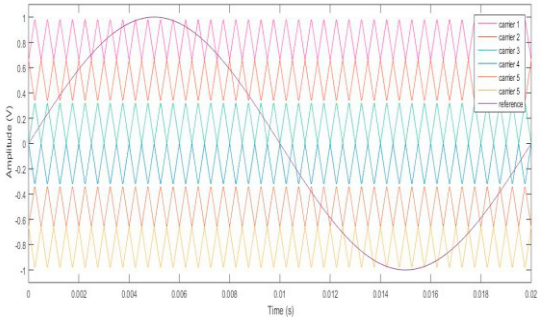

Fig. 6. Multi carrier PWM frequency spectrum of APOD.

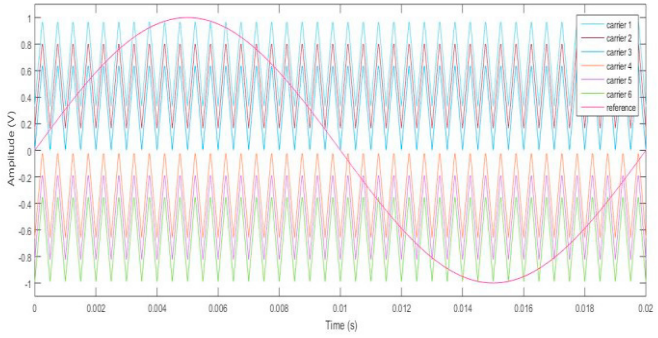

Fig. 7. Multi carrier PWM frequency spectrum of CO.

In this CO shows better RMS voltage at different modulation index. In Fig.8 the 7 level output voltage and current from the simulation are shown which meets the power generating limits (voltage and current) for single phase inverter for grid applications. In Fig.9 the voltage and current waveform after LC filter are shown. The peak voltage of the system under test at different modulation index and different output voltage for various PWM generating techniques [9] are shown in Table 6. The RMS voltage of the system under test at different modulation index and different output voltage for various PWM generating techniques are shown in Table 7. The voltage THD of the system under test at different modulation index and different output voltage for various PWM generating techniques are shown in Table 8. In inverter analysis THD has a great impact over other performance criteria, by considering THD aspect CO PWM technique shows the better result when compared to other PWM techniques at constant frequency PWM generating methods. It is analyzed that to minimize THD and to get better voltage RMS CO PWM method [10] shows better result at the modulation index of 1 for proposed PV configuration when compared to conventional MLI's [11] [12].

Table. 6. Peak voltage obtained using constant frequency multicarrier PWM Techniques with different modulation index and output voltage levels

levels	M_a	PWM	V_{Peak} (V)				
			PD	IPD	POD	APOD	CO
7	1	CF	341.3	341.3	341.4	341.7	340.4
	0.9		340.9	340.9	340.2	340.7	342.5
	0.8		339.1	339.2	339.3	339.3	348.3
	0.7		340	339.8	340.8	339.5	351.7
9	1	CF	316.9	316.8	317.1	316.6	330.7

	0.9	321	321	321.1	321.3	338.9
	0.8	326.9	327	327.6	327.7	344.7
	0.7	333.4	339.8	334.6	334.7	347.7

Table.7. RMS voltage obtained using constant frequency multicarrier PWM Techniques with different modulation index and output voltage levels

levels	M_a	PWM	V_{rms} (V)				
			PD	IPD	POD	APOD	CO
7	1	CF	241.3	241.3	241.4	241.6	240.6
	0.9		241	241.0	240.4	240.9	242.1
	0.8		239.7	239.8	239.9	239.9	246.2
	0.7		240	240.2	240.9	240.0	248.6
9	1	CF	223.4	224.0	224.2	223.8	233.8
	0.9		227.0	226.9	227.0	227.1	239.6
	0.8		231.1	231.2	231.6	231.7	243.7
	0.7		235.7	240.2	236.5	236.6	245.8

Table.8. Voltage THD obtained using constant frequency multicarrier PWM Techniques with different modulation index and output voltage levels.

levels	M_a	PWM method	Voltage THD (%)				
			PD	IPD	POD	APOD	CO
7	1	CF	1.17	1.18	1.18	1.18	0.95
	0.9		0.71	0.72	0.69	0.71	0.86
	0.8		0.76	0.76	0.77	0.77	0.88
	0.7		0.85	0.85	0.86	0.86	0.97
9	1	CF	0.67	0.66	0.69	0.7	1.19
	0.9		0.58	0.58	0.6	0.61	0.91
	0.8		0.62	0.62	0.64	0.63	0.92
	0.7		0.74	0.85	0.74	0.72	0.97

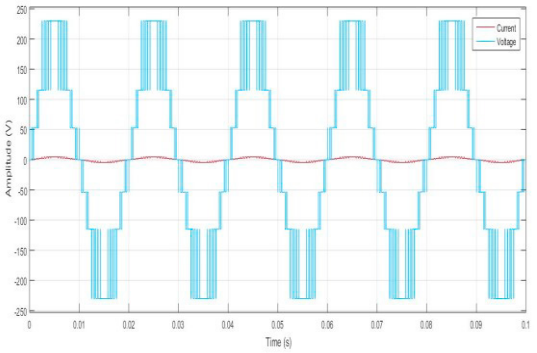

Fig. 8. Voltage and Current Waveform From CO MCPWM.

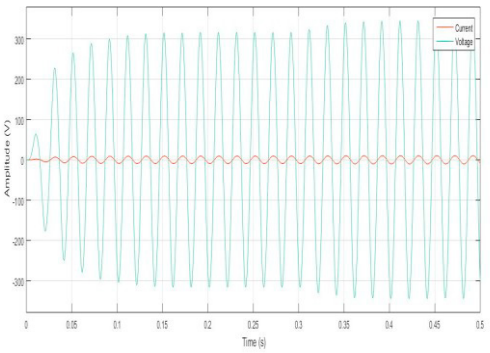

Fig. 9. Voltage and Current Waveform From LC Filter.

5. Conclusion

In this paper, a hexagonal switch cell multi level inverter with reduced device count for PV based grid application is studied. The proposed topology can produce 7,9 and 11 level output with only 7 switches. The proposed topology is validated for determining the best performance of the inverter under various constant frequency PWM generation techniques under MATLAB/Simulink. The simulation results show that the carrier overlap PWM technique acquires better RMS voltage and THD for the proposed configuration when compared to other techniques. This reduced device count topology can be implemented in PV configuration with converter for grid application to reduce the size, circuit complexity and better performance compared to conventional MLI's.

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