A survey on multipliers, adders and adiabatic logic styles suitable for power reduction

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A survey on multipliers, adders and adiabatic logic styles suitable for power reduction

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Abstract: Low power circuits and designs are the need of the hour as they find applications in electronic components which have power efficient processing capabilities. High speed processors are power consuming and multipliers contribute to a maximum extent for this power consumption. Thus, to achieve low power designs, adiabatic logic is one of the noted technologies in this regard. Adiabatic logic can be implemented for different types of circuit designs and this paper concentrates on a survey of various multipliers and adders that can be modified into a low power multiplier using adiabatic logic.

1. Introduction

Multipliers and adders implemented using adiabatic logic are an ingredient to low power circuit design, but the dilemma in choosing a multiplier, adder and an adiabatic logic style from numerous multiplier, adder and adiabatic styles is a concern for researchers. This paper gives a brief survey about the multiplier, adder and adiabatic architectures commonly used and tries to get a solution to yield a low power design.

2. Multipliers

Multipliers are defined as the process of repeated addition and are an integral part of all processors. Multipliers are time consuming and power consuming units and if the power consumption is reduced, it will lead to subsequent reduction in the power consumption of the overall design. The three main parts of the multiplier are,

1. Partial product generation
2. Partial product accumulation
3. Final addition

1 1 0 1	Multiplicand
* 1 1	Multiplier
1 1 0 1	
1 1 0 1	Partial products
1 0 0 1 1 1	Final product

Generally partial product generation is the main area of concern when coming to implementing strategies regarding power reduction. Partial product accumulation is mainly shifting operation, and

weightage in terms of low power implementation techniques is less. Finally, the addition part can also be altered for low power design.

2.1 Types of multipliers

The following multipliers are taken into consideration for analysing the multipliers suitable for adiabatic logic implementation:

1. Tree Multiplier
2. Array Multiplier
3. Vedic Multiplier
4. Carry Save Multiplier

Tree multiplier is a weight based multiplier design and has two phases of operation. In the first phase, AND operation of each bit takes place and the wires are awarded weights based on their position. In the second phase, full adder and half adder are used to reduce the partial products. Finally, a normal adder is used to do the normal addition for the last stage.

Array multiplier is similar to the conventional mathematical multiplier which is implemented using AND gates, shift registers and adders. It is a time consuming process, but the underlying principle is the simplest of all.

Vedic multipliers are based on the 16 vedic techniques mentioned in ancient Indian mathematical analysis. Present day usage of these techniques using modern EDA (Electronic Design Automation) tools has resulted in designing circuits with minimal hardware.

Carry save multiplier is based on rearranging the array multiplier design slightly in order to avoid carry propagation onto each row and finally adding the carry value to the results of each row.

3. Adders

Adders are an integral part of multipliers, and are the last step in multiplication. Major part of research has been undertaken in the partial product generation side, but considering power reduction in adders will add to the cause of generating low power designs.

3.1 Types of adders

The following adders are taken into consideration for analysing the addition process in the multipliers defined in the previous section.

1. Full Adder
2. Carry Look Ahead Adder

Full adder is a three bit adder which can be implemented using two exclusive OR gates, two AND gates and an OR gate. It is the most basic adder design and is the base for all other adders.

Carry look ahead adder is aimed at increasing the speed of higher bit addition by implementing parallelism. It eliminates the carry rippling effect by modifying the logic in adder design. Thus, n-bit adder can perform the addition of n bits simultaneously without waiting for the previous carry to propagate to the current stage of addition.

4. Adiabatic logic

Adiabatic logic works on the following two principles, “Never turn on a transistor when there is a voltage potential between the source and drain” and “Never turn off a transistor when there is current flowing through it.”[1]

Switching power dissipation of CMOS (Complementary Metal Oxide Semiconductor) circuit with capacitive load has a lower limit of $C_L V_{dd}^2/2$ (where C_L: Load Capacitance, V_{dd}: Supply Voltage). Adiabatic switching circuits the switching power dissipation below this lower limit. It allows recycling of energy to reduce the total energy drawn from the power source. Thus, the power which may otherwise get wasted can be reused for the power requirement of the same system.

4.1 Challenges in adiabatic system

Adiabatic technique cannot be implemented for a single part of a single circuit as it is not recommendable in terms of design cost, manufacturing cost and time. So, part of the circuit which consumes large amount of power should be identified and possibility of applying adiabatic logic has to be checked. Also, the more the same type of circuit repeats, more is the gain in the power sector. A repetitive circuit which is bad in terms of power consumption and power dissipation and has a feasibility of applying adiabatic logic has to be first identified. Multiplier is one of the possible circuits as it is power consuming and also a common part in most of the processors. Another main problem that has to be addressed in adiabatic logic is increase in area.

4.2 Types of adiabatic logic styles

The following are some of the adiabatic logic styles commonly used in the low power principles,

1. ECRL (Efficient Charge Recovery Logic)
2. Clocked CMOS adiabatic logic

In ECRL, the power lost during capacitance discharge is reused by providing feedback mechanism to power devices. It performs precharge and evaluation simultaneously. It is a dual rail circuit.

Clocked adiabatic logic is also a dual rail logic to integrate all power control circuitry on the chip which leads to reduced expenses and good power control. Clocked adiabatic logic can also be operated from a dc power supply in a non energy-recovery mode compatible with standard CMOS logic.

5. State of the art

Adiabatic logic systems have been investigated by reasearchers and some of the works carried out are discussed in brief.

Wallace Dadda and Vedic Dadda multiplier have been implemented using ECRL (Efficient Charge Recovery Logic) adiabatic design and achieved 77% less power compared to conventional CMOS[2]. An array multiplier has been implemented using CEPAL (Complementary Energy Path Adiabatic Logic) in 32nm HSPICE tool and 47% reduction in power consumption was achieved[3]. A 8*8 tree multiplier has been implemented using ECRL (Efficient Charge Recovery Logic) adiabatic design in 22nm CADENCE tool and 61.5% less power consumption was observed compared to conventional CMOS[4]. A 16 bit logarithmic signal processor has been implemented using clocked adiabatic logic in 0.35μm and 10 times less power consumption than conventional CMOS was achieved[5]. 2*2, 4*4 and 8*8 vedic multipliers have been implemented using EEAL(Energy Efficient Adiabatic Logic) and the researchers achieved power saving of 64.3%, 56% and 41% respectively in 0.18μm CADENCE[6]. Adiabatic logic has been implemented in 8*8 tree multiplier and yielded 33% less power compared to conventional CMOS[7].

A full adder has been implemented in ECRL and SQAL (Secured-Quasi Adiabatic Logic) and the researchers achieved 69% less power in ECRL and 71.8% less power in SQAL in 45nm technology[8]. Adiabatic logic has been implemented in 4-bit carry look ahead adder and resulted in 25-30% less power compared to the conventional CMOS[9]. A semi-custom design has been implemented using PFAL (Positive Feedback Adiabatic Logic) and a power saving factor of 17 times at 10MHz and 7 times power saving at 100MHz was achieved compared to conventional CMOS[10]. NAND/NOR gates have been implemented using adiabatic logic and it has been reported that adiabatic logic is best suitable for less than 30MHz applications rather than 1MHz or lower applications[11]. A 0.8V CMOS adiabatic differential switch logic circuit has been implemented using bootstrap technique and resulted in 26% less power consumption and 52% smaller propagation delay[12]. A 8 bit carry look ahead adder has been implemented using Energy Recovery Adiabatic Logic Family and 2 to 5 times less dissipative circuit was achieved was achieved[13].

Adiabatic QSERL (Quasi Static Energy Recovery Logic) has been implemented in a 8*8 carry save multiplier using two complementary sinusoidal supply clocks and 34% energy saving has been reported[14]. Clocked CMOS adiabatic logic has been implemented using 1.8μm technology in inverters[15].

6. Conclusion

From a comprehensive review of the literature, it is evident that the types of multipliers and adders contribute to a lesser extent in power saving and the way in which type of adiabatic logic is used plays a major extent in power saving as seen in figure 1.

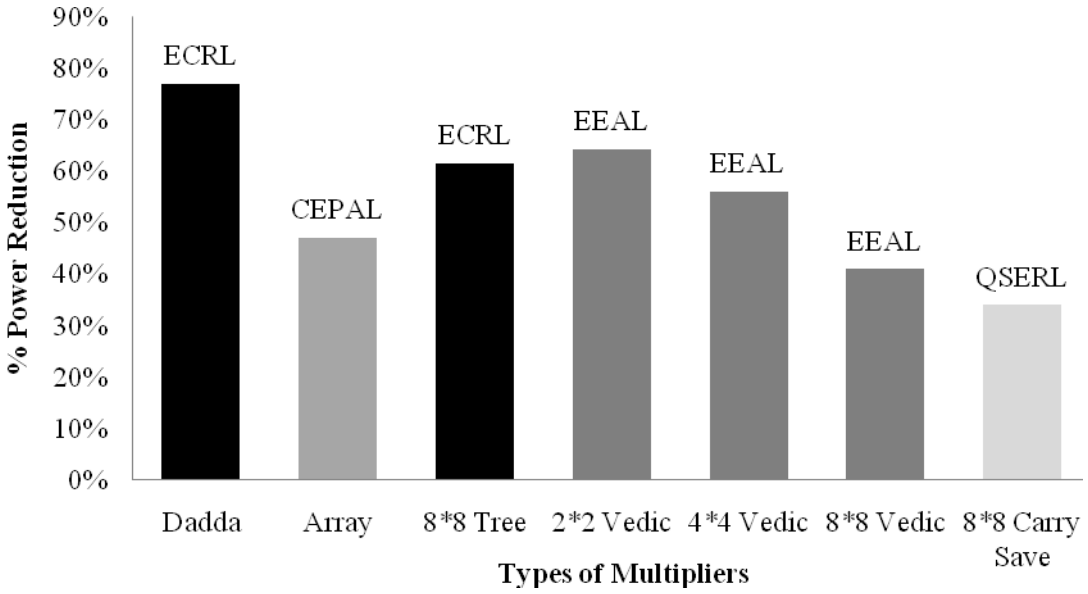

Figure 1. Power saving in multipliers by adiabatic logic.

ECRL (Efficient Charge Recovery Logic) and Clocked Adiabatic Logic are types of adiabatic logic which can be looked upon for constructing efficient low power designs using multipliers and adders.

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