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An Efficient High Gain DC-DC Converter for Automotive Applications

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ABSTRACT

This paper presents a high gain DC-DC converter which uses a clamp circuit to achieve soft switching. The proposed converter is designed to supply a high intensity discharge (HID) lamp used in automobile head lamps. The converter operates from a 12V input supply and provides an output voltage of 120V at 35W output power. A clamp circuit consisting of a clamp capacitor, clamp switch and resonant inductor will help to achieve zero voltage switching (ZVS) of the both main and clamp switches. The practical performance of the converter was validated through experimental results. Results obtained from the prototype hardware prove that the converter meets the requirements of HID lamp application and can be a very good alternative to existing converters.

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1. INTRODUCTION

The high gain boost converter has become essential in all present day applications such as automobile applications, photovoltaic systems, medical equipments and UPS systems. In all such applications, a DC-DC converter with voltage gain equal to or greater than 10 is essential. The classical boost converter fails to provide a voltage gain of 10 because of the limited duty ratio. Increased duty ratio leads to high reverse recovery problems, high switching stress resulting in reduced efficiency and increased electromagnetic interference (EMI) [1]. Other alternative topologies for obtaining high voltage ratio include flyback converters, coupled inductor (CI) based topologies, switched capacitor and other boost derived topologies. Flyback converters are capable of providing high gain but presence of winding leakage inductance leads to higher component current stress as depicted in [2].

In coupled inductor based topologies, high gain is obtained by varying the number of turns in the coupled inductor. This reduces the switching stress and eliminates the reverse recovery problem also as demonstrated in [3]. However, the use of a coupled inductor leads to voltage ringing across the switch due to the leakage inductance and the stray capacitance. Therefore, it becomes necessary to use a snubber circuit or a switch with relative high ON state resistance ($R_{DS,ON}$). Consequently, this results in degraded converter efficiency.

In [4] and [5], a converter topology which used the active clamp circuit to effectively recycle the stored energy present in the coupled inductor was proposed. Further, the stored energy in the stray inductance can be absorbed by using a coupled inductor with a passive regenerative snubber as claimed in [6]. A coupled inductor based topology which used multi-winding and a voltage doubler circuit was presented in [7]. The topology proposed in [8] used a coupled inductor with appropriate turns ration to obtain high conversion ratio. This topology integrated a flyback arrangement and a step-up converter. The topologies incorporating

the coupled inductor or flyback transformer do not provide the required high gain at high output power ratings. This is mainly due to the limited capacity of magnetic core which has to be substantially increased based on the incremental output power.

For low power applications, high step-up converter based on the switched-capacitor circuit is preferred. Since inductors are not used, the switched capacitor converter helps to achieve high power density as proposed in [9]-[11]. However, regulating the output voltage results in reduced efficiency. By integrating the switch capacitor with boost converter, higher conversion ratios at better efficiencies are possible. However, such topologies require more number of components as presented in [12]. Topologies proposed in [13] and [14] use only a single switch. These topologies were developed using switched capacitor and switched inductor hybrid circuit. These circuits possess reduced switch and diode voltage stress. Further, by adding voltage multiplier capacitor stages, the voltage gain at a given duty ratio can be increased.

Cascading of boost converter also can provide high gain even under normal duty ratio as described in [15]-[17]. However, the switch voltage stress will be extremely high. Further, the switching frequency and operating efficiency is limited due to hard switching. In order to avoid this, soft switching, using an active clamp circuit, can be employed as proposed in [18] and [19].

A soft switched high gain DC-DC converter is presented in this paper. The proposed converter consists of two boost stages that use a single power switch and an auxiliary switch. The active clamp circuit is used to realise soft switching of both the main and auxiliary switches Q and Qa respectively. This arrangement reduces the switching stress and increases the converter's operating efficiency. The circuit configuration, operating modes, analysis details, design methodology and experimental results are discussed in the subsequent sections.

2. CIRCUIT DESCRIPTION

The conventional boost converter cannot provide high gain due to limitations of duty cycle and reverse recovery problems. One method to obtain high gain without increasing the duty ratio is to connect two boost stages in cascade configuration as shown in Figure 1. To reduce the complexity of the two-stage boost converter, the power switches Q_1 and Q_2 in Figure 1 can be reduced to single power switch Q as shown in Figure 2. The power switch Q operates in hard switching causing high switching stress. To achieve soft switching of the switch, an active clamp circuit comprising of an auxiliary switch Q_a, clamp capacitor C_C and resonant inductor L_r in added as shown in Figure 3.

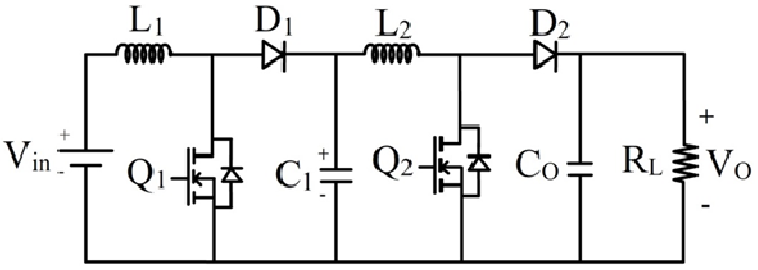

Figure 1. Two-stage boost converter

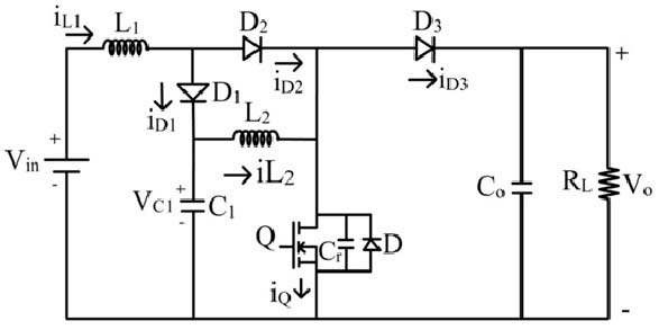

Figure 2. Two-stage boost converter with single switch

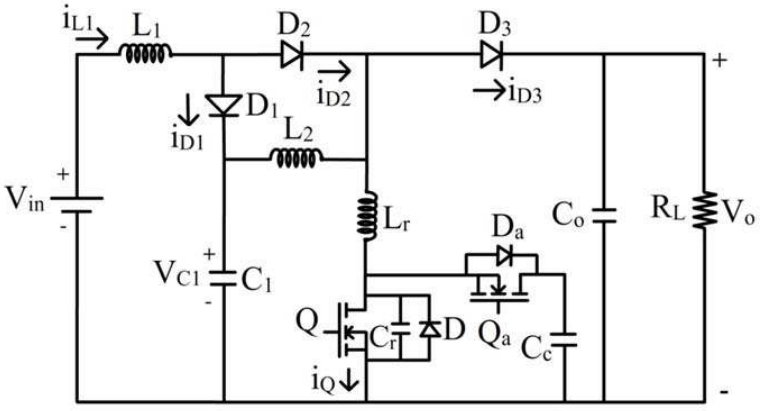

Figure 3. Proposed high gain soft switched boost converter

In this soft switched topology, circuit components L_1, D_1, D_2, C_1 and Q act as the first stage of the boost converter and provides a voltage conversion ratio of

$$\frac{V_{C1}}{V_{in}} = \frac{1}{1-D} \tag{1}$$

where D is the duty ratio of Q. The second stage boost converter consisting of components C_1, L_2, Q_2, D_3 and C_o and voltage conversion ratio is

$$\frac{V_o}{V_{C1}} = \frac{1}{1-D} \tag{2}$$

Thus, the effective conversion ratio of the cascaded boost converter is obtained as

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \tag{3}$$

3. CIRCUIT OPERATION

The operating modes of the proposed converter are elaborated by assuming that (i) the value of the inductor L_1 and L_2 are greater than L_r, (ii) the resonant inductor stores more energy than the resonant capacitor C_r to achieve soft switching and (iii) the capacitance of C_1, Cc and Co are large enough so that voltage across them are constant. There are eight modes of operation for proposed converter as detailed below.

Mode 1 ($t_0 < t < t_1$): *In this mode, the main switch Q is turned ON and auxiliary switch Q_a remains in OFF state.* The diode D_2 is conducting while diodes D_1 and D_3 are OFF. The output capacitor C_o discharges through the load. Since L_1 and L_2 is greater than L_r, inductor currents i_{L1} and i_{L2} increase and are given by

$$i_{L1}(t_1) \cong i_{L1}(t_0) + \frac{V_{in}}{L_1} DT \tag{4}$$

$$i_{L2}(t_1) \cong i_{L2}(t_0) + \frac{V_{C1}}{L_2} DT \tag{5}$$

where D is the duty ratio of the main switch Q and T is time period. This mode ends by the main switch Q is turned OFF at time t_1.

Mode 2 ($t_1 < t < t_2$): The main switch Q is turned OFF. Positive inductor current of i_{Lr} now charges the capacitor C_r from 0 to V_{C1}-$V_{Lr} \approx V_{C1}$ since L_1 and L_2 are greater than L_r. The capacitor voltage $V_{Cr} < V_{C1}$, the diodes D_1 and D_3 are reversed biased while diode D_2 is still conducting. When $V_{Cr} = V_{C1}$, diode D_1 is forward biased as the voltage across the diode D_1 and C_1 is same V_{C1}.Thus, at time t_2, this mode ends when D_1 is turned ON.

Mode 3 ($t_2 < t < t_3$): In this mode, the diodes D_1 and D_2 are conducting with diode current i_{D1} increasing and i_{D2} decreasing. This mode ends at time t_3 when $V_{Cr} = V_{CC}$ which causes the anti-parallel body diode of Q_a to become forward biased.
Mode 4 ($t_3 < t < t_4$): This mode begins when the anti-parallel diode of Q_a becomes forward biased. Now the resonant inductor current i_{Lr} will flow through the anti-parallel diode Q_a to ground. Therefore, the drain to source voltage is zero for Q_a. The switch Q_a is now turned ON, thus achieving ZVS during this interval. This mode comes to an end at time t_4 when diode current i_{D2} becomes zero and the diode D_2 is reversed biased while diode D_3 is turned ON.
Mode 5 ($t_4 < t < t_5$): This mode commences at time t_4. At this time interval, D_2 is reverse biased while D_3 is turned ON. The inductor currents i_{L1}, i_{L2} and the resonant inductor current i_{Lr} decrease from positive to negative magnitude. The switch Q_a should be turned OFF before i_{Lr} becomes negative to achieve ZVS. Therefore, switch Q_a is turned OFF at time t_5 which marks the end of this mode.
Mode 6 ($t_5 < t < t_6$): In this mode, the resonant inductor current i_{Lr} is negative and the switch Q_a is turned OFF while diode D_3 still conducts. Since i_{Lr} is negative, it is understood that the voltage across capacitor C_r discharges. Hence, the capacitor voltage V_{Cr} starts to decreases from $V_{Cc.}$ ZVS operation of the main switch is ensured since the capacitor voltage V_{Cr} becomes zero and forward biases the anti-parallel diode. This mode ends when $V_{Cr} = 0$ at time t_6.
Mode 7 ($t_6 < t < t_7$): In this mode, capacitor voltage $V_{Cr}=0$ due to which the anti-parallel diode is forward biased. The inductor current i_{Lr} increases towards positive value from a negative value. The main switch Q is turned ON at ZVS interval. The diode D_1 and D_3 are still conducting. By the end of this mode, at time t_7, the output diode D_3 is turned OFF and the diode D_2 is forward biased.
Mode 8 ($t_7 < t < t_8$): In this mode, the diode D_3 is turned OFF. The diodes D_1 and D_2 are in commutation interval. The voltage across capacitor C_1 will be same as the induced voltage drop across the resonant inductor. This causes the inductor current i_{Lr} to increase. This mode ends when diode D_1 is turned OFF with $i_{D1}=0$ and marks the commencement of the next cycle. Figure 4 shows the characteristic waveform of the considered converter and Figure 5 shows the equivalent circuit diagrams during various operating modes.

4. ANALYSIS OF THE PRESENTED CONVERTER

The steady state analysis of the circuit is used to derive important characteristic equations like voltage gain and device stress. By volt-second balance principle applied across the inductors L_1 and inductor L_2, without considering the duty cycle loss in each mode, the steady state voltage gain equation can be derived.

When the switch Q remains in ON state, the voltage across the inductor L_1 is equal to the supply voltage V_{in}. When the switch Q is OFF, the voltage across L_1 will be $V_{L1}=V_{in}-V_{C1}$. Now, by applying volt-second balance, we get

$$V_{in}D + (V_{in} - V_{C1})(1 - D) = 0 \quad (6)$$

Rearranging equation (6), we get

$$\frac{V_{C1}}{V_{in}} = \frac{1}{1 - D} \quad (7)$$

When the switch Q is ON, the voltage across the inductor L_2 will be same as the voltage across capacitor C_1. When the switch Q is tuned OFF, the voltage across the inductor is given by

$$V_{L2} = V_{C1} - V_o \quad (8)$$

Applying volt-second balance across inductor L_2 gives

$$V_{C1}D + (V_{C1} - V_o)(1 - D) = 0 \quad (9)$$

Rearranging equation (9), we get

$$\frac{V_o}{V_{C1}} = \frac{1}{1 - D} \quad (10)$$

Combining the equations (7) and (10), the overall conversion ratio of the proposed converter is derived as

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \tag{11}$$

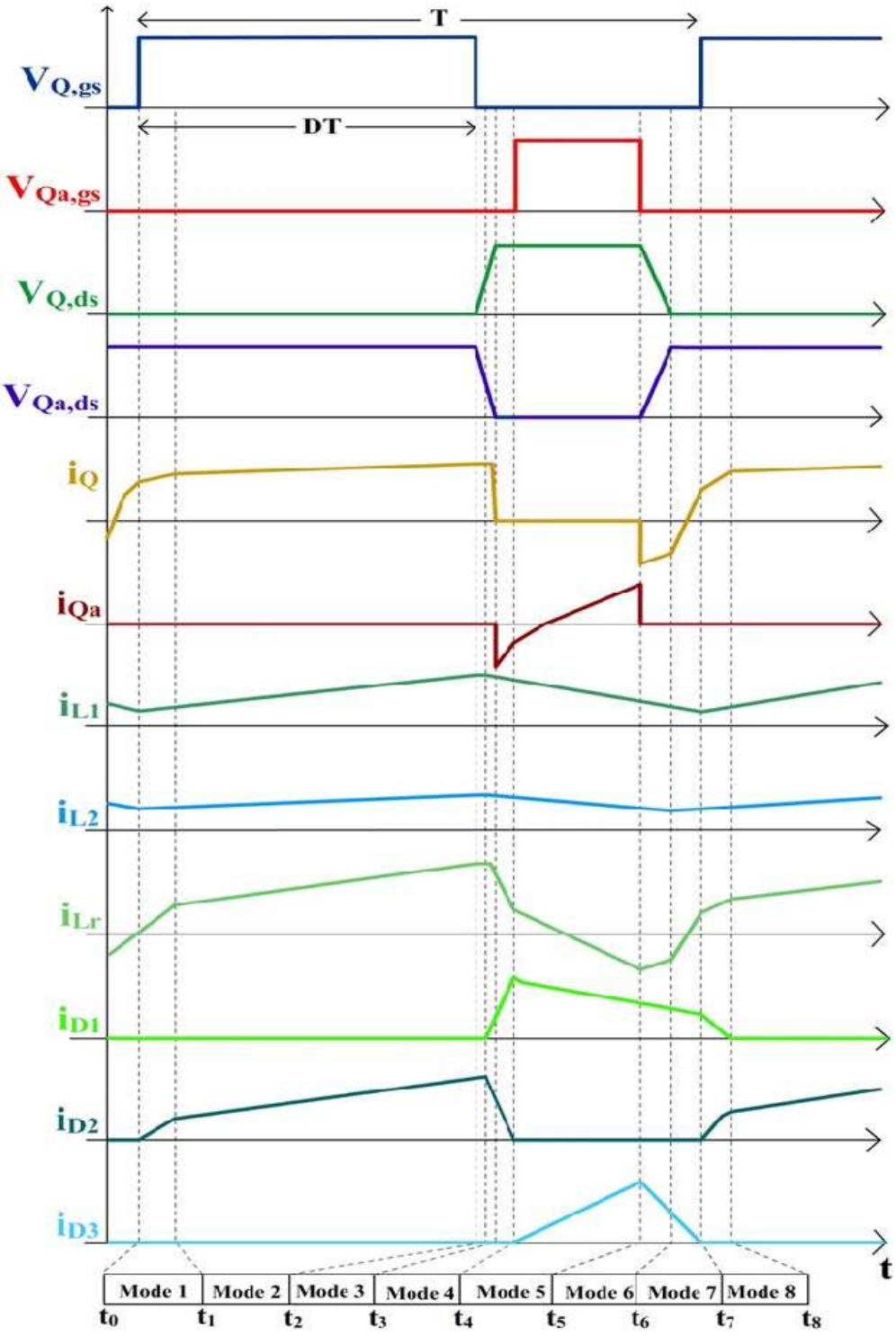

Figure 4. Characteristic waveforms of the presented converter

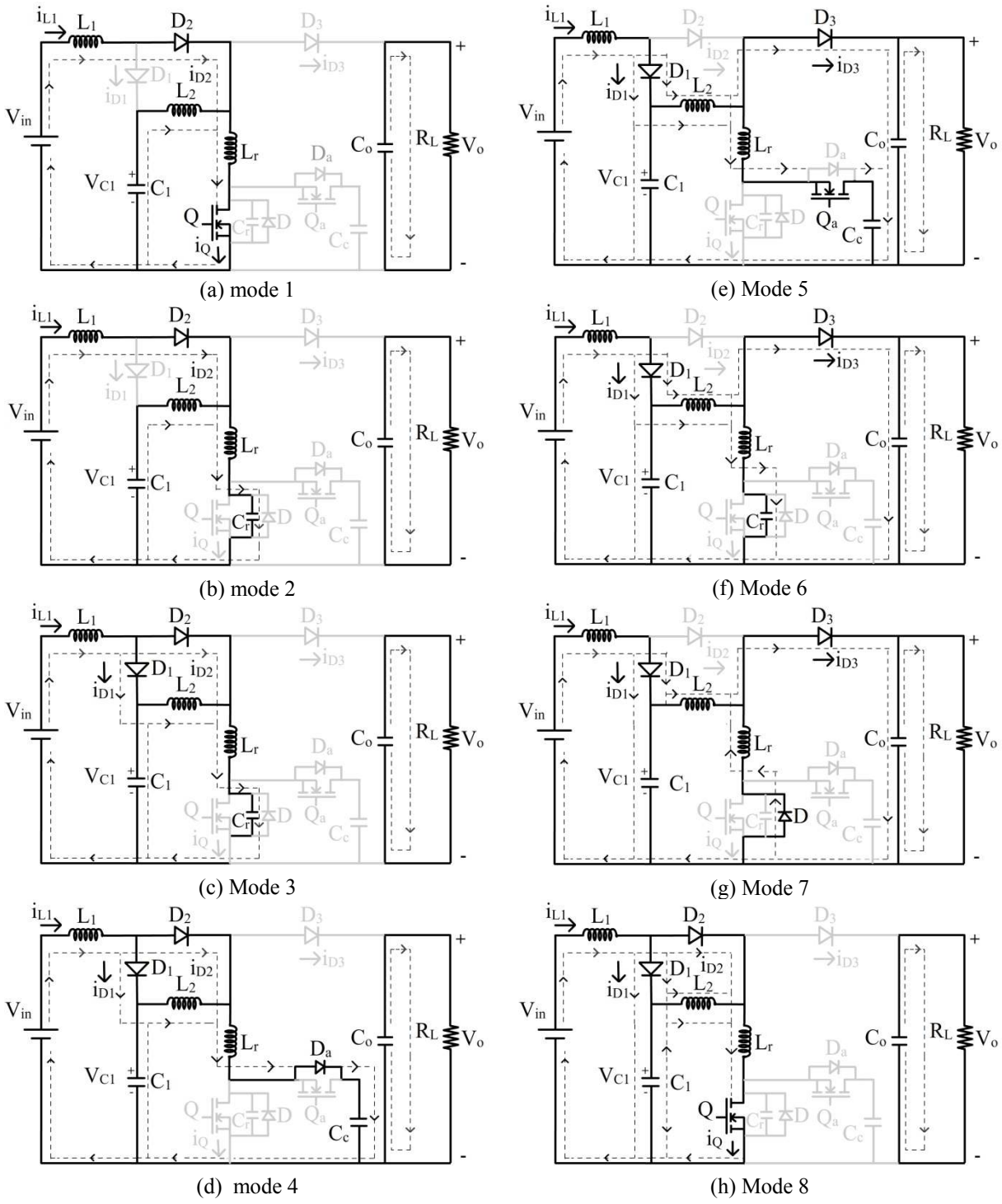

Figure 5. Equivalent for various operating modes

5. DESIGN SPECIFICATIONS

The reactive elements (L_1, L_2 and C_C) and the maximum duty cycle of the proposed converter can be designed from equation (11) as

$$D_{max} = 1 - \sqrt{\frac{V_{in,max}}{V_o}} \tag{12}$$

Based on the specified inductor ripple current Δi_{L1} and Δi_{L2} values, the inductance values are derived as

$$L_1 \geq \frac{DTV_{in}}{\Delta i_{L1}} \tag{13}$$

$$L_2 \geq \frac{DTV_{in}}{\Delta i_{L2}(1-D)} \tag{14}$$

For successful soft switching of the main and auxiliary switches, the energy stored in the resonant inductor L_r should be greater than energy stored in resonant capacitor C_r. The expression relating this condition is derived by considering the operating modes and is given by

$$L_r \geq \frac{C_r V_{Cc}^2}{\left(i_{Lr}(t_3)\right)^2} \tag{15}$$

The gating time delay between the main and the auxiliary switch is given by

$$t_d = \frac{\pi\sqrt{L_r C_r}}{2} \tag{16}$$

From the known C_r value, the value of the L_r can be calculated using equation (14) as

$$L_r \cong \frac{4t_d^2}{\pi^2 C_r} \tag{17}$$

The value of clamp capacitance is derived from the expression

$$C_C \gg \frac{(1-D)^2 T^2}{L_r \pi^2} \tag{18}$$

6. EXPERIMENTAL RESULTS

The adopted converter was fabricated in the laboratory and operated from an input voltage of 12V, provided an output voltage of 120V at 50kHz switching frequency and delivered an output power 35W. The values of inductors L_1 and L_2 were computed and designed to be 471µH and 4mH respectively. The switching frequency was maintained same as the resonant frequency. Therefore, the value of resonant inductor was designed to be 4.7µH for a resonant capacitor with value 4.7µF/160V. The values of clamp and output capacitors were designed as 1nF/160V and 100µF/160V respectively. The gate pulses were obtained by suitably programming PIC18F45k20 flash microcontroller. The power devices used were IRFP250 and all the diodes were MUR460 fast recovery power diodes. The experiment was carried out with a resistive load which was adjusted to draw the required power at the rated voltage condition.

Figure 6 shows the gate pulse of the main switch, auxiliary switch and the output voltage. It is observed that the gate pulses are provided with the desired duty cycle and are complimentary to each other. The average output voltage obtained from the converter is 106V which is very close to the designed value. The reduction in output voltage is due to incremental voltage drop across the inductor and the switches. This drop could be compensated by suitably adjusting the duty cycle.

Figure 7 shows the gate pulses applied to main switch Q, auxiliary switch Q_a, the voltage stress across the switch Q and the output voltage. It is clear that the main switch experiences a voltage stress which is close to the output voltage.

Figure 8 shows the gate pulses applied to the switches and the voltage stress experienced by them. The switch duty cycle, operating frequency, proper turn ON and turn OFF of both the switches and the complimentary behaviour of the switches can be confirmed. Further, it is clear that the switch voltage stress is close to the output voltage. It is interesting to notice that the voltage across the switch exhibits ringing since snubber circuits were not used.

Figure 9 shows the measured waveform of gate pulse, voltage stress and current stress of the switch Q. The magnitude of the switch current is in accordance with the expected value. The zero voltage switching (ZVS) of the main switch Q is shown in Figure 10. Before the switch is turned ON, the switch current is

negative and voltage across the switch is reduced to zero. This confirms the proper operation of the soft switching circuit which was added to the cascaded boost converter. Figure 11 shows the photograph of the implemented converter.

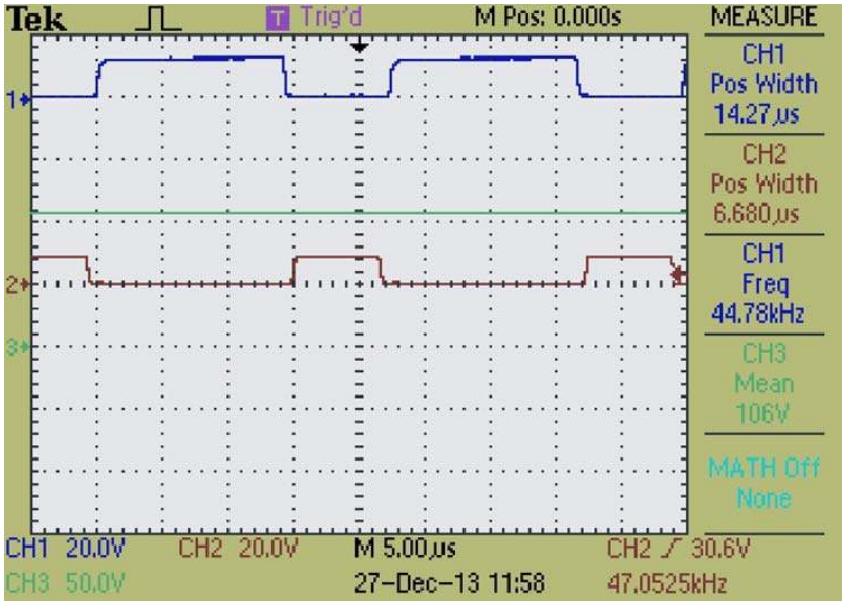

Figure 6. Gate pulse of main switch Q, auxiliary Q_a and output voltage

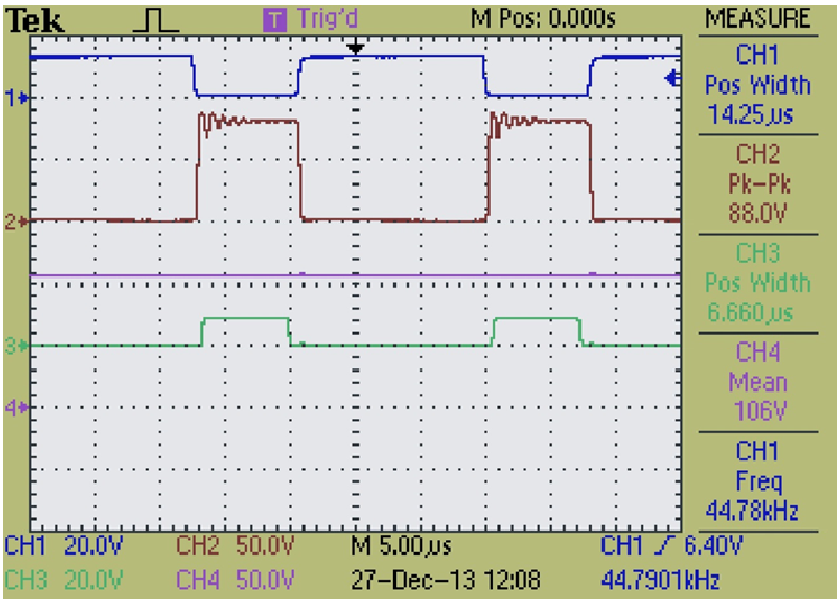

Figure 7. Gate pulses of Q and Q_a, voltage stress of Q and output voltage

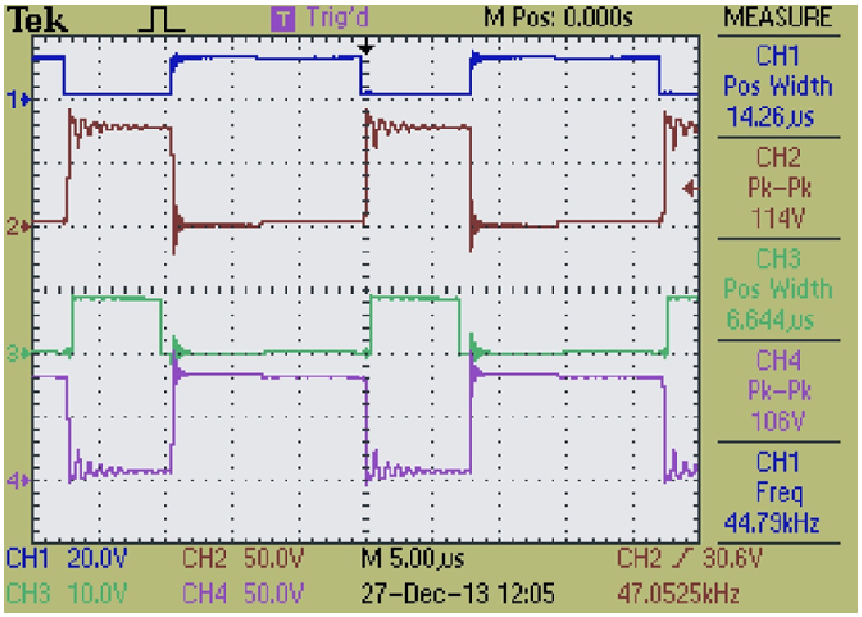

Figure 8. Gate pulses and voltage stresses of switches Q and Qa

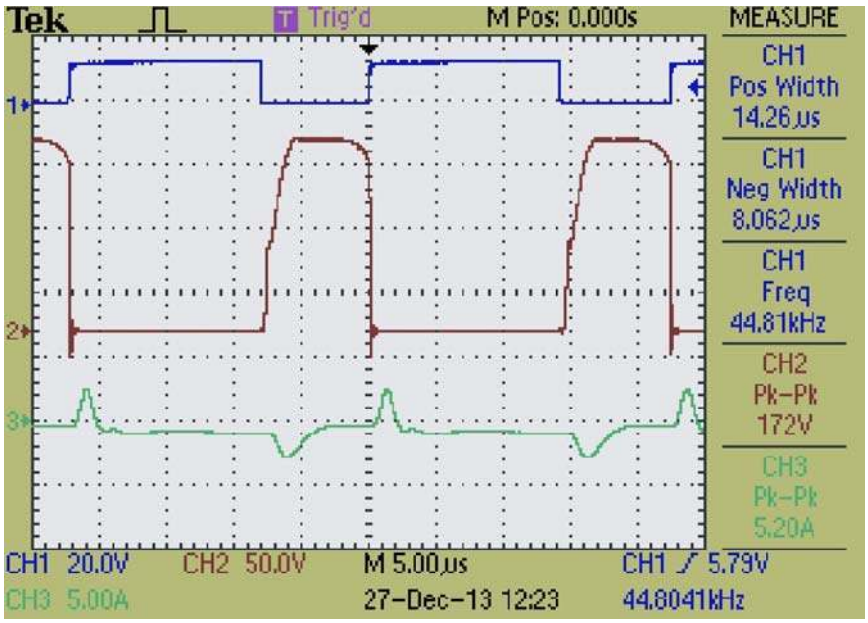

Figure 9. Gate pulse, voltage across switch Q and current through the main switch Q

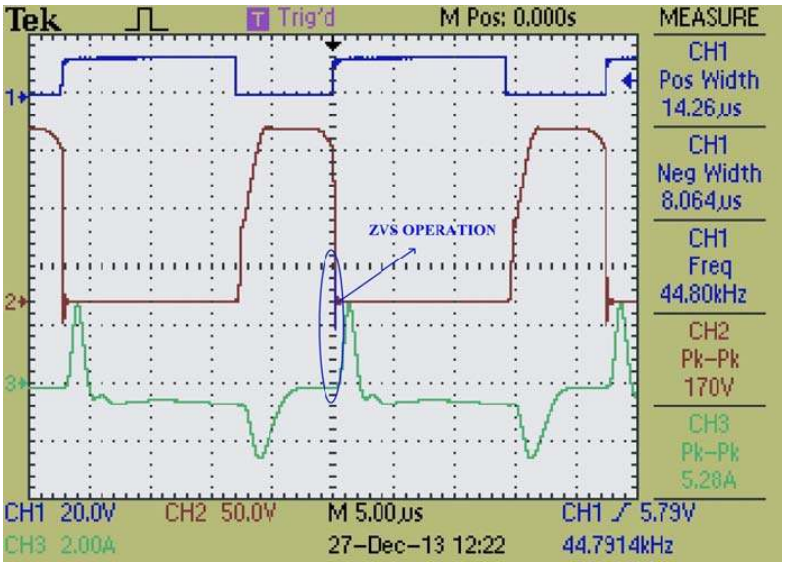

Figure 11. Zero Voltage Switching (ZVS) of main switch Q

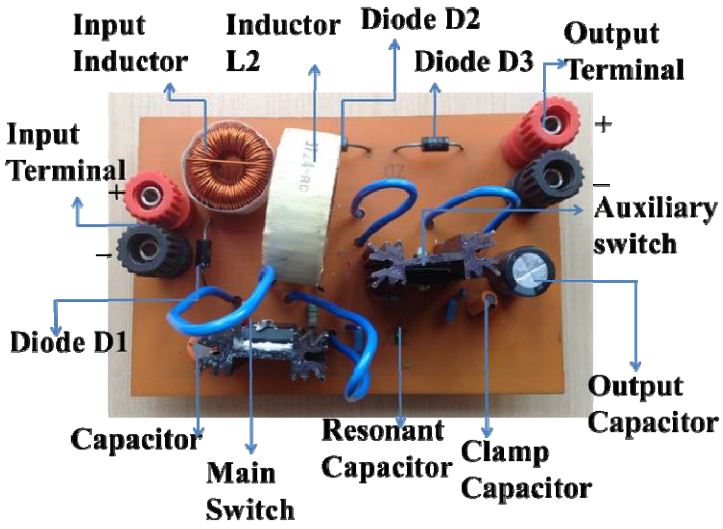

Figure 12. Photograph of the implemented converter

7. CONCLUSION

This paper presented the analysis, design and experimental verification of a soft switched DC-DC converter, which was designed for automotive HID lamp application. The converter provided the required voltage gain at the designed power level. Experimental results prove the validity of the design. The main desirable features of this converter are (i) its ability to operate under soft switching condition (ii) reduced device stress and (iii) high voltage gain at lower duty ratio. By proper choice of inductor and switches, the required voltage gain can precisely be achieved.

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