Received June 10, 2019, accepted July 13, 2019, date of publication July 19, 2019, date of current version August 6, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2929836

Analysis of Logic Gates for Generation of Switching Sequence in Symmetric and Asymmetric Reduced Switch Multilevel Inverter

KANIKE VINOD KUMAR AND R. SARAVANA KUMAR
School of Electrical Engineering, Vellore Institute of Technology, Vellore 632014, India
Corresponding author: R. Saravana Kumar (rsaravanakumar@vit.ac.in)

ABSTRACT Analysis of logic gates for the switching sequence operation of reduced switch multilevel inverter (MLI) is introduced in this paper. Two variants of MLI with reduced switches are considered for the analysis of the logic gates to obtain proper output voltage level. One MLI is with the symmetrical voltage, and the other is with the asymmetrical voltage. The analysis of the proposed logical operation is presented through the single-phase seven-level output voltage for both symmetrical and asymmetrical inverters. Input pulse pattern for the operation of the logic gates are chosen from the multi carrier pulse width modulation (PWM) techniques as phase disposition (PD), phase opposition disposition (POD), and alternate POD (APOD). The analysis for the generation of the required pulse pattern to operate the switches in MLI is presented as logical equations. The simulation work is performed and evaluated with the MATLAB/Simulink. The real-time simulation is performed for the required pulse pattern and generated with the support of dSPACE 1104. The THD comparative analysis is analyzed with a modulation index and various PWM methods.

INDEX TERMS 5 switch module, 8 switch module, logic gates, multilevel inverter, pulse pattern, multi carrier sinusoidal pulse width modulation, total harmonic distortion.

I. INTRODUCTION

Binary logic consists of various logical operations which represent a logical meaning for various conditions based on the output of systems. In many computer and processor operations, computational analysis and decision making systems, binary logic operations play the key role for system control. Binary logic mainly depends on two values with different names like 'True and False', 'Yes and No', 'On and Off' etc. In this paper, the values with '1' and '0' are preferred for convenience. '1' assigned for 'On' condition of the switch and '0' assigned for 'Off' condition. The combination of binary logic and a proper logical operation called Boolean algebra.

Boolean algebra basically consists of three logical operations, which are called basic logic gates: AND, OR and NOT. Each logical operation produces a binary output based on their operation presented as truth table in Table 1 for two input signals. These logic gates are electronic circuits which operate on two or more input signals and generate desired output based on the logical operation except NOT gate. NOT gates operate with one signal and its truth table is given in Table 2. Input signals may be a communication signal,

TABLE 1. Truth table of OR, AND, NOR, NAND, EXOR and EXNOR logic gates for two inputs.

Inputs		Outputs					
A	B	OR	AND	NOR	NAND	EXOR	EXNOR
0	0	0	0	1	1	0	1
0	1	1	0	0	1	1	0
1	0	1	0	0	1	1	0
1	1	1	1	0	0	0	1

TABLE 2. Truth table for NOT gate.

Input	Output
0	1
1	0

The associate editor coordinating the review of this manuscript and approving it for publication was Yang Han.

2169-3536 © 2019 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

TABLE 3. Required components for traditional MLIs.

Type of MLI	No. of DC Sources	No. of Switches	No. of Capacitors for DC- bus	Clamping Capacitors	Clamping Diodes
Diode Clamped	1	2 x (L-1)	L-1	-	(L-1) x (L-2)
Flying Capacitor	1	2 x (L-1)	L-1	(L-1) x ((L-2)/2)	-
Cascaded H-Bridge	(L-1)/2	4 x ((L-1)/2)	-	-	-

electrical voltage or current signal, etc. The output signal of the logic gates are used to On/Off a switch in the proposed work. An exclusive gate is available for the critical situations of the switching operations. EXOR and EXNOR gates are mostly used for the operation of switches and the truth tables are given in Table 1 for both. OR gate is represented with " +", AND gate with " •", NOR gate with "$\bar{+}$", NAND gate with " $\bar{\bullet}$", EXOR gate with " $\oplus$ ", EXNOR gate with " $\odot$ " and NOT gate with " $^{-}$ " [1].

Several Reduced Switch Multilevel Inverters (RSMLI) are proposed to achieve the cost minimization, optimal voltage stress, reduced power losses, frequency operations, less harmonic distortions. Cascaded H-Bridge, Neutral Point Clamped, Diode Clamped, and Flying Capacitors are the Conventional MLI. Operation of these conventional MLI's are performed with the support of gating signals (Pulses) to the power switches of respective inverter design [2]. Generation of gating signals is achieved by various pulse modulation techniques. Different pulse modulation techniques are proposed by researchers for the operation of MLI. Control and estimation of switching losses and the total harmonic distortion is obtained by modulation techniques [3], [4]. Switching frequency is an important criterion for the operation of MLI. Based on the value of frequency modulation, techniques are categorized into two major types. Fundamental frequency with less number of cycles and high switching frequency has repeating signal per cycle.

The sequence of switching operation of various RSMLI's are presented in many research works with one of the modulation methods. But, to obtain the required sequence of the pulse pattern is a critical part of the presented works. Level shifting and phase shifting multi carrier sinusoidal PWM methods are widely used in the previous works [3], [5], [6]. Obtained pulse pattern from the traditional modulation method is not exactly matching with the required pulse pattern of MLI operation. To achieve the required pulse pattern, basic logic gates are used and convert the generated pulse pattern to the required pulse pattern. Analyzing the logic gates for the generation of the required pulse pattern is the major task of the MLI operation. Using the logic gates for the operation of various MLI's are not properly explained in many researchers work [7]–[16].

Design of multilevel inverter with reduce switch is the novel content of many researchers. To obtain the desired output voltage level of reduced switch MLI, a different type of switching operations are performed for the switches. Microcontrollers, microprocessors, real-time simulators are used for the switching operation [17]–[22]. Among these methods, the boolean algebra and logic gates are preferred for the operation of switches in this work as per the switching sequence is shown in Table 4 and 5 [23], [24].

This paper is organized into six sections as, multilevel inverters in section 2, Pulse width modulation methods in section 3, Analysis of logical equations for switching operations in section 4. The results obtained from MATLAB/ Simulink and dSPACE 1104 for proposed work are presented in section 5 and section 6 which conclude the present work.

II. MULTILEVEL INVERTER

The inverter is a power electronic circuit which can convert AC to DC with a basis of two level voltages. The basic inverter is having many issues with its distortion factors, switching losses, and less efficiency. To overcome these issues, multilevel inverters are designed and analyzed by many researchers to provide better features. In the early decades, the integration of inverted power from many power electronic applications is difficult because of distortions in the converted power. The problems causing due to the voltage and current distortions, multilevel inverters are highly preferable from the family of power electronic circuits [25]–[27]. The multilevel inverter is having a starting level with three voltage values. Multilevel inverters have been preferred with various levels like 3, 5, 7, 9, 11, 27, etc. Multilevel inverters are having many features and are mostly required for the domestic, commercial and industrial applications based on the selection of voltage and connectivity.

Based on the operation of the multilevel inverter, three topologies have been presented in many research works. Diode clamped and flying capacitor are operated with single DC voltage source and Cascaded Multilevel Inverter (CMLI) is operated with (L-1)/2 DC voltage sources where 'L' is the level of CMLI. Usage of power semiconductor switches, numbers of DC sources, linear and nonlinear elements are more as given in Table 3. To perform the specified and desired operation of the selected multilevel inverter, various modulation methods have been analyzed [28]–[30].

Many researchers are working on the reduced switch multilevel inverter. Among many researchers work, the most reduced switch multilevel inverter is preferred. Based on observations, 5 switch seven level multilevel inverter [24] and 8 switch seven level multilevel inverter [23] is considered for the research work.

TABLE 4. Switching sequence of 5 switch multilevel inverter.

Level	S_1	S_2	S_3	S_4	S_5
0V	0	0	0	0	0
+V	0	0	1	0	1
+2V	0	1	0	0	1
+3V	1	0	0	0	1
+3V	1	0	0	0	1
+2V	0	1	0	0	1
+V	0	0	1	0	1
0V	0	0	0	0	1
0V	0	0	0	1	0
-V	1	0	0	1	0
-2V	0	1	0	1	0
-3V	0	0	1	1	0
-3V	0	0	1	1	0
-2V	0	1	0	1	0
-V	1	0	0	1	0
0V	0	0	0	0	0

TABLE 5. Switching sequence of 8 switch multilevel inverter.

Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0V	1	1	0	0	0	0	0	0
+V	1	1	0	0	0	1	1	0
+2V	1	1	0	0	1	0	0	1
+3V	1	1	0	0	0	1	0	1
+3V	1	1	0	0	0	1	0	1
+2V	1	1	0	0	1	0	0	1
+V	1	1	0	0	0	1	1	0
0V	1	1	0	0	0	0	0	0
0V	0	0	1	1	0	0	0	0
-V	0	0	1	1	0	1	1	0
-2V	0	0	1	1	1	0	0	1
-3V	0	0	1	1	0	1	0	1
-3V	0	0	1	1	0	1	0	1
-2V	0	0	1	1	1	0	0	1
-V	0	0	1	1	0	1	1	0
0V	0	0	1	1	0	0	0	0

Structure of 5 switch seven level multilevel inverter is shown in Figure.1(a) and 8 switch seven level multilevel inverter is shown in Figure.1(b). 5 switch seven level multilevel inverter is with four symmetrical DC voltage sources. Three switches S_1, S_2, and S_3 are doing an operation of level shift for the output voltage. Switches S_4 and S_5 are operating for the positive half cycle and negative half cycle which leads to the generation of AC voltage and current to the load. 8 switch seven level multilevel inverter is structured with two asymmetrical DC voltage sources. If the first voltage source is of V volts, then the second voltage source should be the double of the first voltage source (2V). Switches S_1, S_2, S_3, and S_4 are used for the positive half cycle and negative half cycle operation of the output. Switches S_5, S_6, S_7, and S_8 are

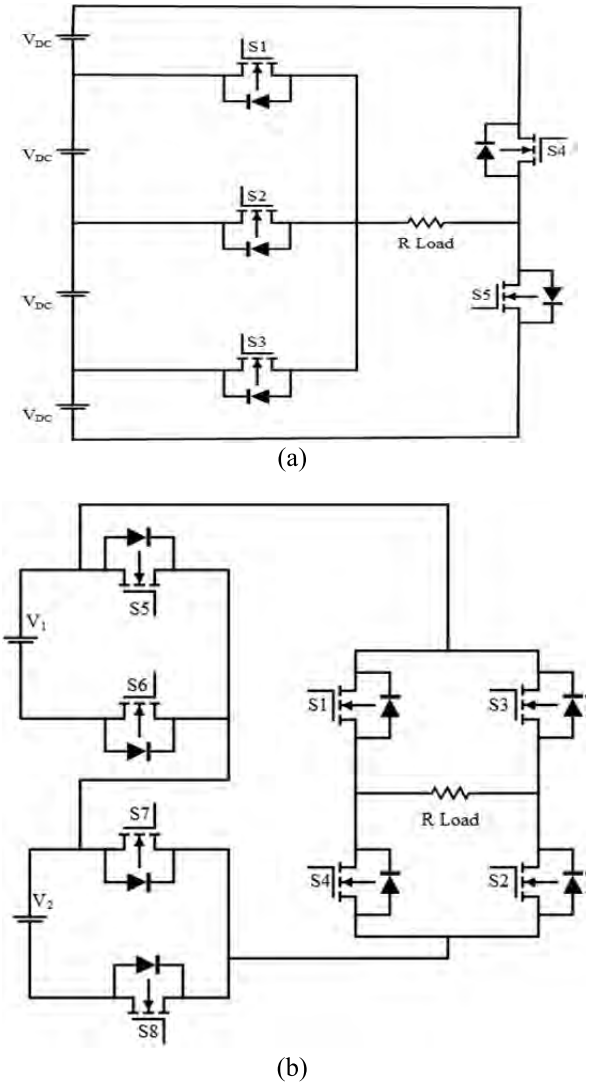


FIGURE 1. (a) Structure of 5 Switch MLI. (b) Structure of 8 Switch MLI.

presented as DC link module for the operation of output level shift. Switching sequences of both the inverters are given in Table 4 and 5.

III. PULSE WIDTH MODULATION TECHNIQUES

To operate the multilevel inverter, low and high switching frequency modulation techniques have been carried out for the research. Based on the suitability of operation and the output requirements, various modulation techniques like Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM), staircase modulation, trapezoidal modulation, harmonic injection modulation, etc, are implemented [29], [31]–[34]. Among all these PWM methods, multiple carriers PWM offers several advantages over single carrier PWM. Selection of the number of carrier signals for the operation of the PWM technique is chosen by [35], [36]

$$\text{Number of carrier signals} = \text{L} - 1 \quad (1)$$

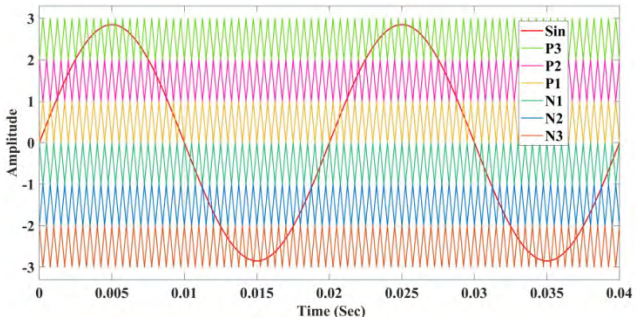


FIGURE 2. Multi Carrier SPWM for 7 level MLI.

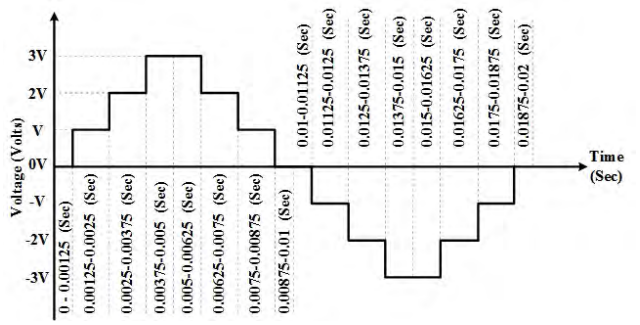


FIGURE 3. Time distribution of one cycle for 7 level MLI.

TABLE 6. Binary representation of pulse pattern for 6 triangular carrier signals.

Time Interval(Sec)	Level	P_3	P_2	P_1	N_1	N_2	N_3
0 - 0.00125	0V	0	0	0	1	1	1
0.00125-0.0025	+V	0	0	1	1	1	1
0.0025-0.00375	+2V	0	1	1	1	1	1
0.00375-0.005	+3V	1	1	1	1	1	1
0.005-0.00625	+3V	1	1	1	1	1	1
0.00625-0.0075	+2V	0	1	1	1	1	1
0.0075-0.00875	+V	0	0	1	1	1	1
0.00875-0.01	0V	0	0	0	1	1	1
0.01-0.01125	0V	0	0	0	1	1	1
0.01125-0.0125	-V	0	0	0	0	1	1
0.0125-0.01375	-2V	0	0	0	0	0	1
0.01375-0.015	-3V	0	0	0	0	0	0
0.015-0.01625	-3V	0	0	0	0	0	0
0.01625-0.0175	-2V	0	0	0	0	0	1
0.0175-0.01875	-V	0	0	0	0	1	1
0.01875-0.02	0V	0	0	0	1	1	1

Multiple carrier modulation techniques are divided into level shifting and phase shifting techniques. Level shifting technique is divided into constant switching frequency multi carrier signal and variable switching frequency multi carrier signal techniques. PD, POD, and APOD are the subdivisions of switching frequency techniques.

In this work, a sinusoidal modulating signal for SPWM with triangular multi carrier signals are used to produce

TABLE 7. Binary representation of pulse pattern for 6 triangular carrier signals and zero carrier signal.

Level	P_3	P_2	P_1	PN_0	N_1	N_2	N_3
0V	0	0	0	1	1	1	1
+V	0	0	1	1	1	1	1
+2V	0	1	1	1	1	1	1
+3V	1	1	1	1	1	1	1
+3V	1	1	1	1	1	1	1
+2V	0	1	1	1	1	1	1
+V	0	0	1	1	1	1	1
0V	0	0	0	1	1	1	1
0V	0	0	0	0	1	1	1
-V	0	0	0	0	0	1	1
-2V	0	0	0	0	0	0	1
-3V	0	0	0	0	0	0	0
-3V	0	0	0	0	0	0	0
-2V	0	0	0	0	0	0	1
-V	0	0	0	0	0	1	1
0V	0	0	0	0	1	1	1

TABLE 8. Binary representation switching operation for S_1 in 5 switch module.

Level		P_3	N_1	N_2	$N_1 \oplus N_2$	$P_3 + (N_1 \oplus N_2)$	S_1
0V	Positive Half Cycle	0	1	1	0	0	0
+V		0	1	1	0	0	0
+2V		0	1	1	0	0	0
+3V		1	1	1	0	1	1
+3V		1	1	1	0	1	1
+2V		0	1	1	0	0	0
+V		0	1	1	0	0	0
0V		0	1	1	0	0	0
0V	Negative Half Cycle	0	1	1	0	0	0
-V		0	0	1	1	1	1
-2V		0	0	0	0	0	0
-3V		0	0	0	0	0	0
-3V		0	0	0	0	0	0
-2V		0	0	0	0	0	0
-V		0	0	1	1	1	1
0V		0	1	1	0	0	0

PWM pulses for the operation of switches in 5 switch and 8 switch module [37]. Level shifting pulse width modulation technique is implemented with constant switching frequency and variable switching frequency with their subdivisions. 'L-1' triangular carrier signals are used with the amplitude of 'A_c' and frequency of 'f_c'. A modulating signal of sinusoidal waveform with the amplitude of 'A_m' and frequency of 'f_m' to generate the pulse for the ON/OFF conditions of the switch is done with the signal comparison of the reference and carrier of PWM method. Based on the amplitude and frequency of the modulating and the carrier signal, modulation index 'M_i' and frequency ratio 'M_f' is estimated as

TABLE 9. Binary representation switching operation for S_2 in 5 switch module.

Level		P_3	P_2	$P_3 \oplus P_2$		N_2	N_3	$N_2 \oplus N_3$		$(P_3 \oplus P_2) + (N_2 \oplus N_3)$	S_2
0V	Positive Half Cycle	0	0	0		1	1	0		0	0
+V		0	0	0		1	1	0		0	0
+2V		0	1	1		1	1	0		1	1
+3V		1	1	0		1	1	0		0	0
+3V		1	1	0		1	1	0		0	0
+2V		0	1	1		1	1	0		1	1
+V		0	0	0		1	1	0		0	0
0V		0	0	0		1	1	0		0	0
0V	Negative Half Cycle	0	0	0		1	1	0		0	0
-V		0	0	0		1	1	0		0	0
-2V		0	0	0		0	1	1		1	1
-3V		0	0	0		0	0	0		0	0
-3V		0	0	0		0	0	0		0	0
-2V		0	0	0		0	1	1		1	1
-V		0	0	0		1	1	0		0	0
0V		0	0	0		1	1	0		0	0

TABLE 10. Binary representation switching operation for S_3 in 5 switch module.

Level		P_1	P_2	$P_1 \oplus P_2$		N_3	$\overline{N_3}$		$(P_1 \oplus P_2) + \overline{N_3}$	S_3
0V	Positive Half Cycle	0	0	0		1	0		0	0
+V		1	0	1		1	0		1	1
+2V		1	1	0		1	0		0	0
+3V		1	1	0		1	0		0	0
+3V		1	1	0		1	0		0	0
+2V		1	1	0		1	0		0	0
+V		1	0	1		1	0		1	1
0V		0	0	0		1	0		0	0
0V	Negative Half Cycle	0	0	0		1	0		0	0
-V		0	0	0		1	0		0	0
-2V		0	0	0		1	0		0	0
-3V		0	0	0		0	1		1	1
-3V		0	0	0		0	1		1	1
-2V		0	0	0		1	0		0	0
-V		0	0	0		1	0		0	0
0V		0	0	0		1	0		0	0

TABLE 11. Binary representation switching operation for S_4 and S_5 in 5 switch module.

Level		N_1	$\overline{N_1}$	S_4		P_1	S_5
0V	Positive Half Cycle	1	0	0		0	0
+V		1	0	0		1	1
+2V		1	0	0		1	1
+3V		1	0	0		1	1
+3V		1	0	0		1	1
+2V		1	0	0		1	1
+V		1	0	0		1	1
0V		1	0	0		0	0
0V	Negative Half Cycle	1	0	0		0	0
-V		0	1	1		0	0
-2V		0	1	1		0	0
-3V		0	1	1		0	0
-3V		0	1	1		0	0
-2V		0	1	1		0	0
-V		0	1	1		0	0
0V		1	0	0		0	0

shown in (2) and (3) [29].

$$M_i = [A_m/(L-1)A_c] \tag{2}$$

$$M_f = [f_c/f_m] \tag{3}$$

For the operation of seven level multilevel inverter, (7-1) carrier signals are considered. Six triangular waveforms as carrier signals with amplitude of 1 for each signal. Switching frequency equals to the carrier signal frequency. The relational operator is used for the comparison of the modulating signal and carrier signal to produce pulses. Modulating signal and carrier signal arrangement is shown in Figure 2. Pulses generated are equals to the number of carrier signals. The number of pulses produced are six which are not equal to switch count. It's a challenge to operate the switches to produce proper output with the available pulses. For 5 switch module, more pulses are present and for 8 switch module, fewer pulses are present which is not in the required switching sequence. To operate these switches, the basic logic gates are considered for the operation and are presented in the design of logical equations section.

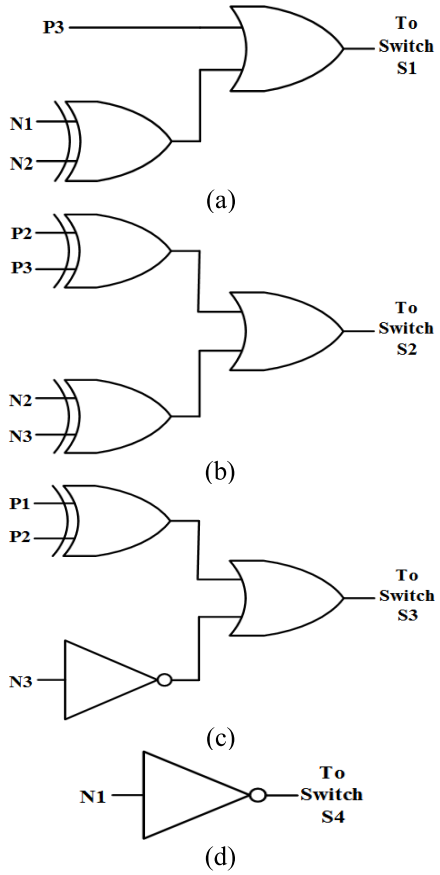


FIGURE 4. Logic gate representation for 5 switch module. (a) To Switch S1 (b) To Switch S2 (c) To Switch S3 (d) To Switch S4.

IV. LOGICAL EQUATIONS FOR SWITCHING SCHEME

As explained in the previous Section, L-1 numbers of carrier signals are needed for L level output voltage. For 7 level output voltage, 6 triangular carrier signals are needed. For 7 level output voltage of MLI, the total time of one cycle is to be distributed for one cycle of 7 level output voltage as shown in Figure. 3. The total number of divisions per cycle and time interval of each division is given in (6) and (7).

$$\text{Frequency of the proposed system (f)} = 50 \text{ Hz} \quad (4)$$

$$\text{Total time period of one cycle (t)} = 1/\text{f} = 0.02 \text{ sec} \quad (5)$$

$$\text{Number of divisions/cycle } (D_t) = (L^*2) + 2 \quad (6)$$

$$\text{Time interval of each } D_t(t_d) = [(L^*2) + 2]/t \quad (7)$$

In many research works for the reduced switch multilevel inverter, the switching sequence pattern is provided for the successful operation of the proposed work for obtaining the outputs as expected. But, the generation of the pulse pattern which is required for the switching sequence is not provided. The technical explanation and the logical relation between pulses generated by the PWM method and pulses required for the switching sequence are properly presented in this section.

With the help of binary representation of pulse pattern for 6 triangular carrier signals and zero carrier signal are shown in Table 6 and 7. For the generation of pulses required for the switching, the sequence is the main objective. Use of logical gates is the major role for switching sequence pulse generation. In this section, various conditions are considered

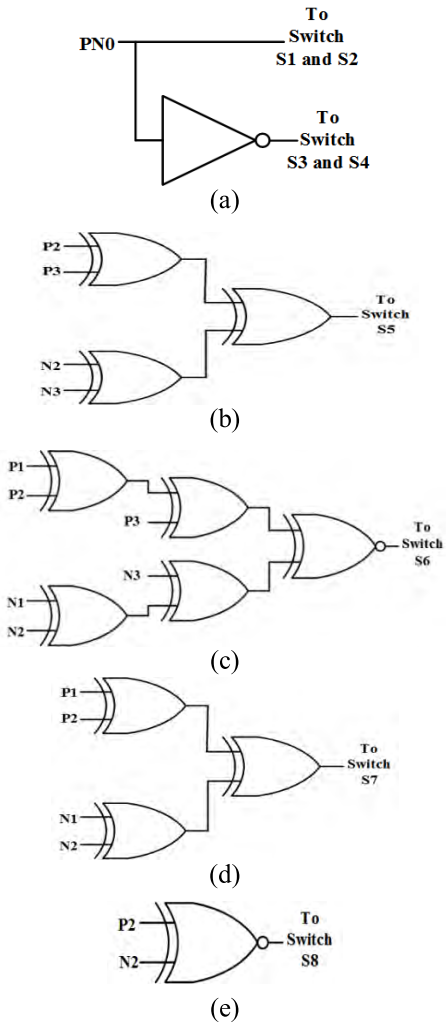


FIGURE 5. Logic gate representation for 8 switch module. (a) To Switch S1, S2, S3 and S4 (b) To Switch S5 (c) To Switch S6 (d) To Switch S7 (e) To Switch S8.

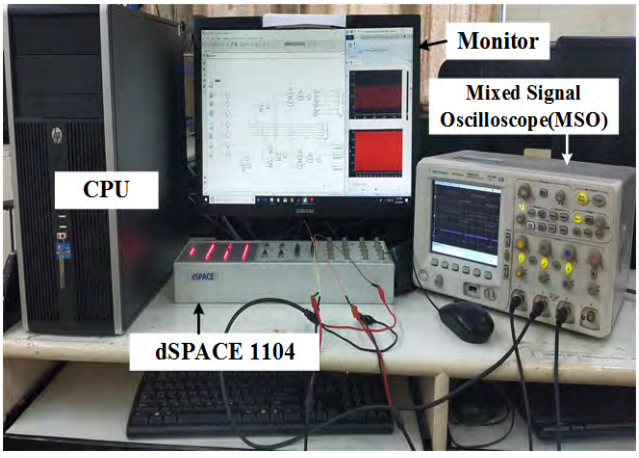


FIGURE 6. Real time interface setup of dSPACE 1104.

TABLE 12. Binary representation switching operation for S_1, S_2, S_3 and S_4 in 8 switch module.

Level		PN_0	S_1 and S_2	$\overline{PN_0}$	S_3 and S_4
0V	Positive Half Cycle	1	1	0	0
+V		1	1	0	0
+2V		1	1	0	0
+3V		1	1	0	0
+3V		1	1	0	0
+2V		1	1	0	0
+V		1	1	0	0
0V		1	1	0	0
0V	Negative Half Cycle	0	0	1	1
-V		0	0	1	1
-2V		0	0	1	1
-3V		0	0	1	1
-3V		0	0	1	1
-2V		0	0	1	1
-V		0	0	1	1
0V		0	0	1	1

TABLE 13. Binary representation switching operation for S_8 in 8 switch module.

Level		P_2	N_2	$P_2 \odot N_2$	S_8
0V	Positive Half Cycle	0	1	0	0
+V		0	1	0	0
+2V		1	1	1	1
+3V		1	1	1	1
+3V		1	1	1	1
+2V		1	1	1	1
+V		0	1	0	0
0V		0	1	0	0
0V	Negative Half Cycle	0	1	0	0
-V		0	1	0	0
-2V		0	0	1	1
-3V		0	0	1	1
-3V		0	0	1	1
-2V		0	0	1	1
-V		0	1	0	0
0V		0	1	0	0

as a case. Each case provides a proper logical operation of the system to produce a proper pulse for the switch. In order to explain logic equations for 5 switch module and 8 switch module, the switches S_2 and S_6 have been chosen.

A. LOGICAL EQUATION FOR SWITCH S_2 IN 5 SWITCH MODULE

In this analysis, one full cycle is considered. The time duration of one full cycle equals to the time duration of the modulating signal. For this proposed work, the sinusoidal modulating signal time period is 0.02 seconds for one cycle i.e., frequency of 50Hz. Carrier signal frequency is 1.5KHz. One full cycle is the combination of a positive half cycle and negative half cycle with time duration of 0.01seconds each. Positive half cycle starting period is 0.00 and the ending period is 0.01seconds and the negative half cycle starts at 0.01 and ends at 0.02 seconds. Application of the logical gate is considered for each half cycle as per the switching sequence. Finally, both half cycle operations are logically combined for the final switching sequence. Operation of switch S_2 in 5 switch module is expressed in the following steps.

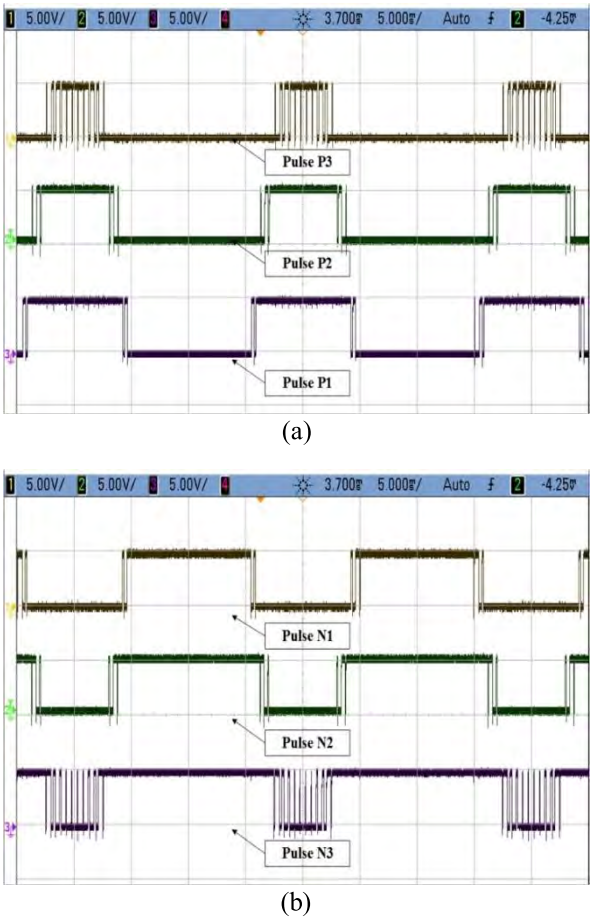


FIGURE 7. PWM pulse pattern for 5 switch module. (a) Positive half cycle (b) Negative half cycle.

Step 1: All obtained pulse patterns are expressed in binary representation form as shown in Table 6.

Step 2: For seven level output, 16 stages of time duration is considered. 1 to 8 stages are for the positive half cycle and 9 to 16 stages are for the negative half cycle. Each stage time interval is 0.00125seconds.

Step 3: Observe the positive half cycle binary representation of switching sequence S_2. Use the required pulses from the binary representation of pulse pattern. P_2 and P_3 are the required pulse pattern for the positive half switching sequence of S_2 with the EXOR gate.

Step 4: Similar to the positive half cycle of S_2, the negative half cycle switching sequence is obtained with the EXOR gate of pulse pattern N_2 and N_3.

TABLE 14. Binary representation switching operation for S_5 in 8 switch module.

Level		P_2	P_3	$P_2 \oplus P_3$	N_2	N_3	$N_2 \oplus N_3$	$(P_2 \oplus P_3) \oplus (N_2 \oplus N_3)$	S_5
0V	Positive Half Cycle	0	0	0	1	1	0	0	0
+V		0	0	0	1	1	0	0	0
+2V		1	0	1	1	1	0	1	1
+3V		1	1	0	1	1	0	0	0
+3V		1	1	0	1	1	0	0	0
+2V		1	0	1	1	1	0	1	1
+V		0	0	0	1	1	0	0	0
0V		0	0	0	1	1	0	0	0
0V	Negative Half Cycle	0	0	0	1	1	0	0	0
-V		0	0	0	1	1	0	0	0
-2V		0	0	0	0	1	1	1	1
-3V		0	0	0	0	0	0	0	0
-3V		0	0	0	0	0	0	0	0
-2V		0	0	0	0	1	1	1	1
-V		0	0	0	1	1	0	0	0
0V		0	0	0	1	1	0	0	0

TABLE 15. Binary representation switching operation for S_6 in 8 switch module.

Level		P_1	P_2	$P_1 \oplus P_2$	P_3	$(P_1 \oplus P_2) \oplus P_3$	N_1	N_2	$N_1 \oplus N_2$	N_3	$(N_1 \oplus N_2) \oplus N_3$	$[(P_1 \oplus P_2) \oplus P_3] \odot [(N_1 \oplus N_2) \oplus N_3]$	S_6
0V	Positive Half Cycle	0	0	0	0	0	1	1	0	1	1	0	0
+V		1	0	1	0	1	1	1	0	1	1	1	1
+2V		1	1	0	0	0	1	1	0	1	1	0	0
+3V		1	1	0	1	1	1	1	0	1	1	1	1
+3V		1	1	0	1	1	1	1	0	1	1	1	1
+2V		1	1	0	0	0	1	1	0	1	1	0	0
+V		1	0	1	0	1	1	1	0	1	1	1	1
0V		0	0	0	0	0	1	1	0	1	1	0	0
0V	Negative Half Cycle	0	0	0	0	0	1	1	0	1	1	0	0
-V		0	0	0	0	0	0	1	1	1	0	1	1
-2V		0	0	0	0	0	0	0	0	1	1	0	0
-3V		0	0	0	0	0	0	0	0	0	0	1	1
-3V		0	0	0	0	0	0	0	0	0	0	1	1
-2V		0	0	0	0	0	0	0	0	1	1	0	0
-V		0	0	0	0	0	0	1	1	1	0	1	1
0V		0	0	0	0	0	1	1	0	1	1	0	0

Step 5: Total switching sequence of switch S_2 is obtained by the OR gate of two switching sequences obtained from step 3 and step 4. The resultant logical equation for switching sequence S_2 is given in (8). Binary representation operation is shown in Table 9.

$$S_2 = (P_3 \oplus P_2) + (N_2 \oplus N_3) \tag{8}$$

Similarly, logical equations for switch S_1, S_3, S_4, and S_5 have obtained the step by step operation as presented for switch S_2. Binary representation operation of switches S_1, S_3, S_4 and S_5 are given in Tables 8, 10 and 11 respectively. Resultant logical equations of switches S_1, S_3, S_4, and S_5 are given in equations (9), (10), (11), and (12). Individual switch logic gate representations are shown in Figure.4. Switch S_5 is directly connected with pulse pattern P_1, no logic gate representation is presented.

$$S_1 = P_3 + (N_1 \oplus N_2) \tag{9}$$

$$S_3 = (P_1 \oplus P_2) + \bar{N_3} \tag{10}$$

$$S_4 = \bar{N_1} \tag{11}$$

$$S_5 = P_1 \tag{12}$$

TABLE 16. Binary representation switching operation for S_7 in 8 switch module.

Level		P_1	P_2	$P_1 \oplus P_2$		N_1	N_2	$N_1 \oplus N_2$		$(P_1 \oplus P_2) \oplus (N_1 \oplus N_2)$	S_7
0V	Positive Half Cycle	0	0	0		1	1	0		0	0
+V		1	0	1		1	1	0		1	1
+2V		1	1	0		1	1	0		0	0
+3V		1	1	0		1	1	0		0	0
+3V		1	1	0		1	1	0		0	0
+2V		1	1	0		1	1	0		0	0
+V		1	0	1		1	1	0		1	1
0V		0	0	0		1	1	0		0	0
0V	Negative Half Cycle	0	0	0		1	1	0		0	0
-V		0	0	0		0	1	1		1	1
-2V		0	0	0		0	0	0		0	0
-3V		0	0	0		0	0	0		0	0
-3V		0	0	0		0	0	0		0	0
-2V		0	0	0		0	0	0		0	0
-V		0	0	0		0	1	1		1	1
0V		0	0	0		1	1	0		0	0

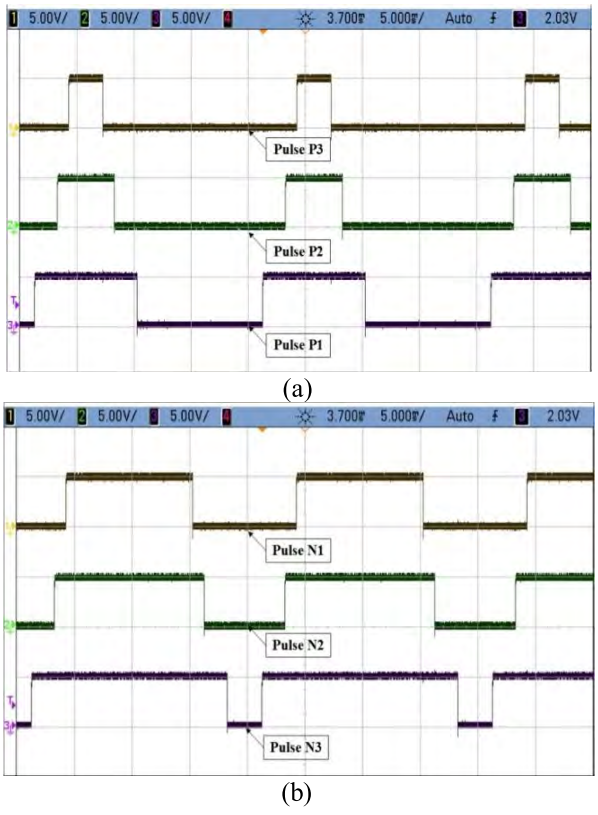


FIGURE 8. PWM pulse pattern for 8 switch module. (a) Positive half cycle (b) Negative half cycle.

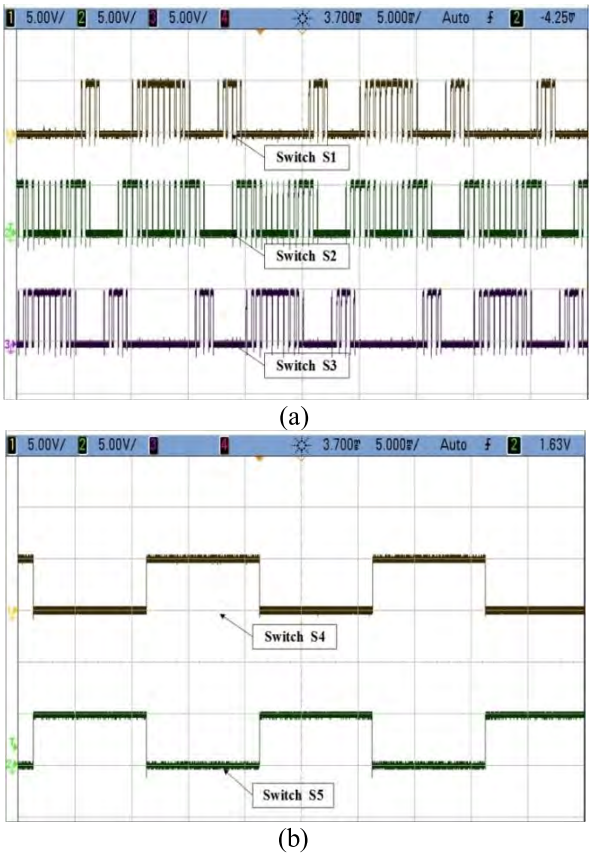
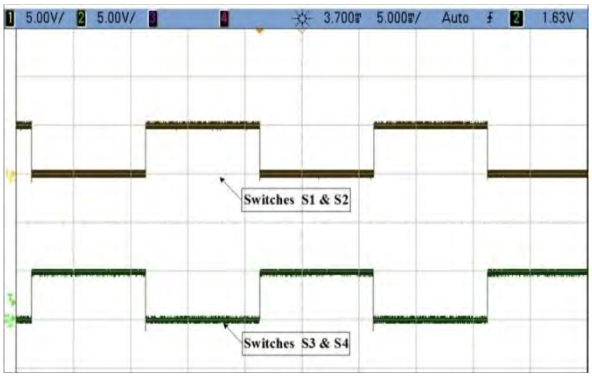


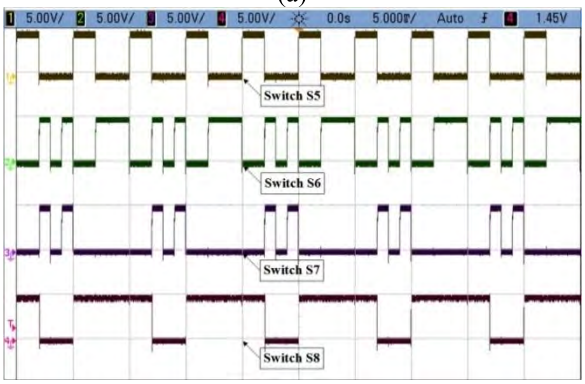
FIGURE 9. Switching sequence pulse pattern for 5 switch module. (a) Switches S_1 , S_2 and S_3 (b) Switches S_4 and S_5.

B. LOGICAL EQUATION FOR SWITCH S_6 IN 5 SWITCH MODULE

Selection of 8 switch module is to extend the analysis of logic gates operation for more switches compared to the output level. The switching frequency of 2KHz is selected to observe the operation with a different parameter. A similar analysis of the 5 switch module is carried out for the



(a)



(b)

FIGURE 10. Switching sequence pulse pattern for 5 switch module. (a) Switches S_1 , S_2 , S_3 and S_4 (b) Switches S_5 , S_6 , S_7 and S_8.

operation of 8 switch module. Required operation of switch S_6 is presented with the support of binary representation.

Step 1: The binary representation of all pulse patterns is to be expressed along with the pulse pattern of the zero sequence carrier signal shown in Table 7.

Step 2: Positive half cycle of switching operation is obtained with the combination of three pulse patterns. EXOR combination of P_1 and P_2, then the output is combined with P_3 to obtain the switching sequence operation for the positive half cycle of switch S_6. Combination of P_1 and P_2 with EXOR gate is used for the operation of switch S_7.

Step 3: For the operation of switch S_6 negative half cycle pulse patterns N_1 and N_2 are combined with EXOR gate then, its output is combined with N_3. The output of a sequence of EXOR gate with N_1 and N_2 is used for the negative half cycle operation of switch S_7.

Step 4: Complete switching sequence of switch S_6 is obtained by EXNOR of the positive half cycle and negative half cycle switching sequences which are given in the above two steps. Resultant logical equation of switching sequence for switch S_6 is given in (13) and represented in Table 15.

$$S_6 = [(P_1 \oplus P_2) \oplus P_3] \odot [(N_1 \oplus N_2) \oplus N_3] \quad (13)$$

Step 5: Switches S_1 and S_2 are operated for the response of the positive half cycle. S_3 and S_4 are for the negative half cycle. Switching sequence of these switches are obtained by zero sequence carrier signal which provides a pulse pattern of PN_0 and $\overline{PN_0}$.

A similar method of logical analysis is applied as given in the above steps to obtain the logical equations for switch S_1, S_2, S_3, S_4, S_5, S_7, and S_8. Resultant logical equations are given in (14), (15), (16), (17) and (18). Binary representation operation is given in Tables 12, 13, 14, and 16. Individual switch logical gate representations are shown in Figure.5.

$$S_1 \text{ and } S_2 = PN_0 \quad (14)$$

$$S_3 \text{ and } S_4 = \overline{PN_0} \quad (15)$$

$$S_5 = (P_2 \oplus P_3) \oplus (N_2 \oplus N_3) \quad (16)$$

$$S_7 = (P_1 \oplus P_2) \oplus (N_1 \oplus N_2) \quad (17)$$

$$S_8 = P_2 \odot N_2 \quad (18)$$

TABLE 17. % THD comparison of 5 switch module with various PWM methods.

Modulation index (M_i)	%THD of MLI Output Voltage		
	PD PWM	POD PWM	APOD PWM
1.1	4.67	4.15	3.97
1	1.71	1.48	1.11
0.9	1.82	1.43	1.23
0.8	1.67	1.66	1.42
0.7	1.96	2.03	1.97

TABLE 18. % THD comparison of 8 switch module with various PWM methods.

Modulation index (M_i)	%THD of MLI Output Voltage		
	PD PWM	POD PWM	APOD PWM
1.1	5.62	5.47	5.08
1	4.01	3.99	1.90
0.9	4.32	4.49	1.01
0.8	4.84	5.08	0.59
0.7	5.24	2.35	0.52

V. RESULTS

Operation of 5 switch module is performing with the help of seven pulse pattern obtained by multi carrier PWM method. A major task of the proposed work is to obtain the pulse pattern for switches of reduced switch multilevel inverter. Obtained pulse patterns are more in number as compared with the 5 switch module and less in number as compared with 8 switch module. The selected switch is operated as switching sequence pattern presented in Tables 4 and 5. Pulse pattern has to match with the switch sequence pattern to generate the desired level output of the multilevel inverter.

Analysis to obtain the logical equations for the 5 switch module and 8 switch module is explained in section 4. Generation of basic pulse patterns from multi carrier PWM is shown in Figure 7 and 8. Results of switching sequence pulse pattern for 5 switch module and 8 switch module are shown in Figure 9 and 10. All presented results in this work are

TABLE 19. Parameters of proposed work.

Type of Inverter	Input and Output Parameters							
	Input Voltage (Volts)	Modulating Frequency (f_m)(Hz)	Carrier Frequency (f_c)(Hz)	R Load (Ohms)	Output Voltage Peak (Volts)	Output RMS Voltage (Volts)	Output RMS Current (Amps)	Output Power (Watts)
5 Switch Module (Symmetric)	$V_{DC} = 90$	50	2000	100	270	190.9	1.9	362.7
8 Switch Module (Asymmetric)	$V_1 = 72$ $V_2 = 144$	50	1500	100	216	152.7	1.5	229

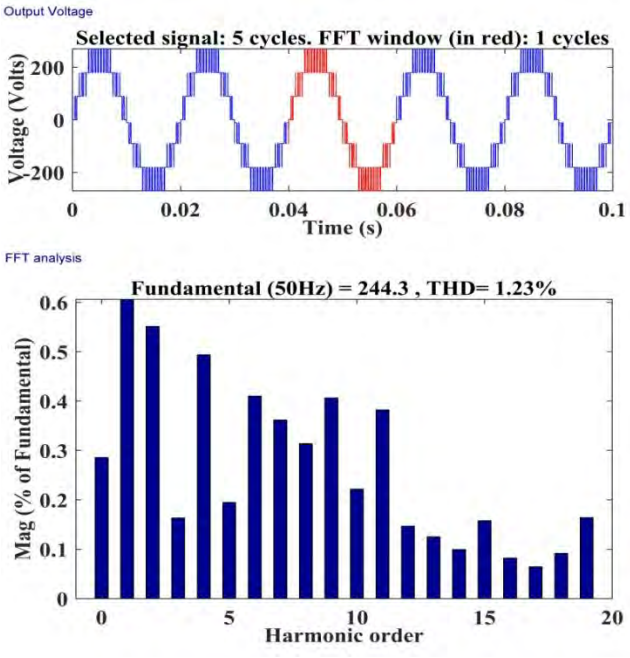


FIGURE 11. Output Voltage and FFT plot for 5 switch module.

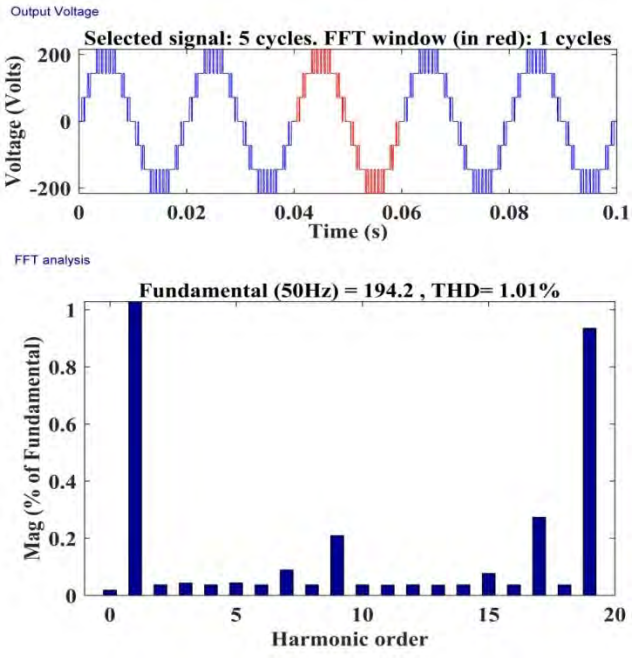


FIGURE 12. Output Voltage and FFT plot for 8 switch module.

done with MATLAB/Simulink. Real time simulation of the required pulse patterns are obtained by dSPACE 1104 with the interface to MATLAB. Real-time interface setup is shown in Figure. 6.

5 switch module is symmetric MLI with input DC voltage of 90V each. Four input voltages sources are used for the operation of 5 switch module to obtain 7 level output voltage for R load of 100Ω. A result of $270V_{Peak}$ is obtained with the simulation of the proposed MLI and the switching control operation by logic gates. 8 switch module is asymmetric MLI with two input DC voltages. V_1 is with the voltage of 72V and V_2 is with 144V. 7 level output voltage of $216V_{peak}$ is obtained with the simulation of 8 switch module for R load of 100Ω.

Comparative THD analysis of 5 switch module and 8 switch module are presented with respect to various modulation index values for APOD, POD, and PD PWM methods. Obtained %THD values of the two proposed modules are clearly mentioned in Table 17 and 18. As per IEEE 519 harmonic distortion standards, the allowable %THD is of 15 to 25% without a filter in the inverter design. The modulation analysis of switching sequence is obtained for THD values which are less by 6% in the case of over modulation. The least harmonic content of 0.52% in resultant voltage is achieved. THD values provided in Table 17 and 18 are the values generated without a filter of the proposed design. If the proposed modules are operated with filter, then they may achieve better results than the previous condition. Based on IEEE 519 standards, 5%THD is allowed for the inverter design with filter. To obtain better results, the designing of the filters are to be focused for the proposed inverters. FFT analysis of the 5 switch and 8 switch module under APOD PWM method is given in Figure 11 and 12 for the output voltage.

5 switch symmetric module and 8 switch asymmetric module are operated with R load. The resultant peak voltage

of 270Volts for 5 switch module and peak voltage of 216Volts for 8 switch module are obtained with a constant fundamental frequency of 50Hz. The input voltage, switching frequency, modulating frequency, output RMS voltage, current and power of the proposed modules are mentioned in Table 19.

VI. CONCLUSION

In this study, a new analysis is proposed for the operation of various reduced switch MLI with the logical gates. The proposed analysis of logical operation is flexible and reliable for the various reduced switch MLI inverter with seven level output voltage. Generated pulse pattern from the analysis is most relevant for the operation of switches based on the switching pattern of the MLI. Main constraints of the proposed work are to present the pulse pattern of multi carrier PWM in binary representation form and analyzing with the basic logic gates to obtain the logical equation for each switch in MLI. Proposed analysis can also be applied for various MLI circuits which are not in this work. This analysis is most useful for the researchers who are presenting their work on novel reduced switch MLI. The simulation work done with MATLAB/Simulink is presented for the considered MLI with their THD analysis. Real time simulation is performed for the generation of pulse pattern of the switching sequences with the help of dSPACE 1104. All obtained results and THD values are compared with various multi carrier sinusoidal PWM methods with respect to various modulation index. Results obtained are satisfying the IEEE 519 standards of the harmonic content.

REFERENCES

[1] M. M. Mano and M. D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL and System Verilog*. London, U.K.: Pearson, 2013.
[2] J. Chen, C. Wang, and J. Li, "Single-phase step-up five-level inverter with phase-shifted pulse width modulation," *J. Power Electron.*, vol. 19, no. 1, pp. 134–145, Jan. 2019.
[3] N. Prabaharan and K. Palanisamy, "Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies," *IET Power Electron.*, vol. 9, no. 15, pp. 2808–2823, 2016.
[4] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renew. Sustain. Energy Rev.*, vol. 76, pp. 1248–1282, Sep. 2017.
[5] D. Karthikeyan, V. Krishnaswamy, and M. A. J. Sathik, "Development of a switched diode asymmetric multilevel inverter topology," *J. Power Electron.*, vol. 18, no. 2, pp. 418–431, Mar. 2018.
[6] C. Dhanamjayulu and S. Meikandasivam, "Performance verification of symmetric hybridized cascaded multilevel inverter with reduced number of switches," in *Proc. Int. Conf. Innov. Power Adv. Comput. Technol.*, Apr. 2017, pp. 1–5.
[7] T. Poompavai and P. V. Priya, "Comparative analysis of modified multilevel DC link inverter with conventional cascaded multilevel inverter fed induction motor drive," *Energy Procedia*, vol. 117, pp. 336–344, Jun. 2017.
[8] M. D. Krishna and S. Vadhera, "Comparative study of hybrid and cascaded H-bridge multilevel inverters," *Int. J. Res. Eng. Technol.*, vol. 2, no. 8, pp. 405–410, 2013.
[9] A. Chitra and S. Himavathi, "Reduced switch multilevel inverter for performance enhancement of induction motor drive with intelligent rotor resistance estimator," *IET Power Electron.*, vol. 8, no. 12, pp. 2444–2453, Dec. 2015.
[10] Y. Viswanath, K. Muralikumar, P. Ponnambalam, and M. P. Kumar, "Symmetrical cascaded switched-diode multilevel inverter with fuzzy controller," in *Soft Computing for Problem Solving*. Singapore: Springer, 2019, pp. 121–137.
[11] J. S. Choi and F. S. Kang, "Seven-level PWM inverter employing series-connected capacitors paralleled to a single DC voltage source," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3448–3459, Jun. 2015.
[12] S. S. Lee, "Single-stage switched-capacitor module (S^3CM) topology for cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018.
[13] S. Narendiran and S. K. Sahoo, "A single phase reduced device count multilevel inverter topology using MCPWM for renewable energy systems," *Energy Procedia*, vol. 117, pp. 244–251, Jun. 2017.
[14] K. A. Aganah, C. Luciano, M. Ndoye, and G. Murphy, "New switched-dual-source multilevel inverter for symmetrical and asymmetrical operation," *Energies*, vol. 11, no. 4, p. 984, Apr. 2018.
[15] B. Mahato, S. Majumdar, and K. C. Jana, "Carrier-based PWM techniques for multi-level inverters: A comprehensive performance study," *J. Sci. A, Eng. Innov.*, vol. 5, no. 3, pp. 101–111, Sep. 2018.
[16] N. Bhargava, S. Gupta, and S. P. Phulambrikar, "Analysis of assymetrical cascaded 7 level and 9 level multilevel inverter for design for asynchronous motor," *Int. J. Eng. Res. Technol.*, vol. 3, no. 8, pp. 499–505, Aug. 2014.
[17] S. Jain and V. Sonti, "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2865–2875, Apr. 2017.
[18] H. Zhang, A. von Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.
[19] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.
[20] K. Thakre, K. B. Mohanty, and A. Chatterjee, "Reduction of circuit devices in symmetrical voltage source multilevel inverter based on series connection of basic unit cells," *Alexandria Eng. J.*, vol. 57, no. 4, pp. 2703–2712, Dec. 2018.
[21] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156–1169, Feb. 2017.
[22] R. Nagarajan and M. Saravanan, "Performance analysis of a novel reduced switch cascaded multilevel inverter," *J. Power Electron.*, vol. 14, no. 1, pp. 48–60, 2014.
[23] R. Uthirasamy, U. S. Ragupathy, and V. K. Chinnaiyan, "Structure of boost DC-link cascaded multilevel inverter for uninterrupted power supply applications," *IET Power Electron.*, vol. 8, no. 11, pp. 2085–2096, Nov. 2015.
[24] S. Umashankar, T. S. Sreedevi, V. G. Nithya, and D. Vijayakumar, "A new 7-level symmetric multilevel inverter with minimum number of switches," *ISRN Electron.*, vol. 29, p. 9, Aug. 2013.
[25] J. Rodríguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Nov. 2002.
[26] C. I. Odeh, "A cascaded multi-level inverter topology with improved modulation scheme," *Electr. Power Compon. Syst.*, vol. 42, no. 7, pp. 768–777, May 2014.
[27] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.
[28] Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "DC-AC cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications," *IEEE Trans. Ind. Appl.*, vol. 45, no. 3, pp. 963–970, May 2009.
[29] K. V. Kumar and R. S. Kumar, "Advanced PWM techniques for control of power electronic converters in PV and motor drive systems," *Int. J. Pure Appl. Math.*, vol. 118, no. 24, pp. 1–21, Apr. 2018.
[30] M. Malinowski, K. Gopakumar, J. Rodríguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
[31] J. Holtz, "Pulsewidth modulation-a survey," *IEEE Trans. Ind. Electron.*, vol. 39, no. 5, pp. 410–420, Oct. 1992.
[32] A. M. Hava and E. Ün, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan. 2009.
[33] S. Umashankar, V. K. A. Shankar, K. Harini, and P. Sanjeevikumar, *Common-Mode Voltage Regulation of Three-Phase SVPWM-Based three-Level NPC Inverter*. Singapore: Springer, 2018.

[34] E. R. C. da Silva, E. C. dos Santos, and C. B. Jacobina, "Pulsewidth modulation strategies," *IEEE Ind. Electron. Mag.*, vol. 5, no. 2, pp. 37–45, Jun. 2011.
[35] N. Prabaharan and K. Palanisamy, "Investigation of single phase reduced switch count asymmetric multilevel inverter using advanced pulse width modulation technique," *Int. J. Renew. Energy Res.*, vol. 5, no. 3, pp. 879–890, 2015.
[36] N. Prabaharan and K. Palanisamy, "A single phase grid connected hybrid multilevel inverter for interfacing photo-voltaic system," *Energy Procedia*, vol. 103, pp. 250–255, Dec. 2016.
[37] P. Palanivel and S. S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," *IET Power Electron.*, vol. 4, no. 8, pp. 951–958, Sep. 2011.

KANIKE VINOD KUMAR received the B.Tech. degree in EEE from the St. Johns College of Engineering and Technology, Yemmiganur, in 2011, and the M.Tech. degree in power electronics from the G Pulla Reddy Engineering College, Kurnool, in 2013. He is currently a Research Scholar with the School of Electrical Engineering (SELECT), Vellore Institute of Technology (VIT), Vellore. His research interests include power electronic converters, PWM methods, and renewable energy systems.

R. SARAVANA KUMAR received the B.E. degree in EEE from the Thiagarajar College of Engineering, Madurai, in 1996, the M.E. degree in power electronics and drives from the College of Engineering, Guindy, Anna University, in 1998, and the Ph.D. degree from the Vellore Institute of Technology (VIT), Vellore, in 2010, where he is currently a Professor with the School of Electrical Engineering (SELECT). He has completed industrial consultancy on power quality issues. His research interests include power electronics applications in drives and renewable energy systems.