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Area and power efficient flipped voltage follower based symmetrical floating impedance scaler with improved accuracy for fully differential filters

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ABSTRACT

A Source Follower based Symmetrical Floating Impedance Scaler (SF-SFIS) circuits are reported in the prior works, which realize large capacitors with the low area for a fully differential filter. In this paper, a novel Flipped Voltage Follower based Symmetrical Floating Impedance Scaler (FVF-SFIS) with high accuracy is presented. The proposed circuit based on flipped voltage follower with cascaded current mirrors can detect low base capacitors which have lower area and power than the prior SF-SFIS circuits. In order to evaluate its performance and comparison, a 500 pF capacitor is realized by multiplying the base capacitor of 10 pF using both FVF-SFIS and SF-SFIS methods. The magnitude and phase of these impedance scalers are obtained through post-layout simulation. It is found that the proposed impedance scaler requires 51.58% lower area, 69.23% lower power dissipation, and 91.33% higher accuracy than the SF-SFIS. The accuracy of the proposed FVF-SFIS is compared with SF-SFIS circuit by designing a 3rd order Chebyshev low pass filter (LPF) using FVF-SFIS and SF-SFIS with cut-off frequency 100 Hz. The circuit has been designed and simulated in UMC 180 nm technology.

1. Introduction

Bio-medical systems such as ECG, EMG, EEG, and EOG require filters operating at low-frequency range (1 mHz to 10 KHz) [1]. These filters require large resistors and capacitors. To minimize the area, the resistors are realized using operational transconductance amplifiers (OTAs) with low transconductance (g_m). A number of design techniques such as current division (CD) and current cancellation (CC), bulk driven and Floating gate with CD (CC) are proposed in the literature [1–4] to realize these OTAs. The low-frequency filters realized using these OTAs are reported in [1–4]. However, reduction of g_m increases the noise level, as there is a tradeoff between g_m and noise [1]. Hence, to realize filters with lower cutoff frequency, a higher value of capacitance is required. The capacitors that can be fabricated in integrated circuits are limited to less than 50 pF due to silicon area limitations [1]. To overcome this problem, a large capacitor (C_{equ}) may be realized using either Voltage mode or Current mode Impedance scalers with a small base capacitor (C_b). In Voltage mode impedance scaler, the base capacitor (C_b) is connected between the inverting input and output of an inverting voltage amplifier whose voltage gain is $|A_V|$. Due to Miller effect [5], the equivalent capacitance (C_{equ}) at the inverting input of the amplifier becomes $C_b(1+|A_V|)$. The Voltage mode impedance scalers provide high multiplication factor only in a limited frequency range and the multiplication factor is supply voltage and process parameter dependent [5]. These limitations are overcome by Current mode impedance scalers.

In [5–15], the current mirror is used to scale up the current through a base capacitor (C_b) with multiplication factor of K and an equivalent capacitor (C_{equ}) of $C_b(1+K)$ is obtained. Current mode impedance scalers may also be implemented using OTAs, dual output differential amplifiers and current conveyors [16–19] as active elements. The current mode impedance scalers are used to realize large grounded capacitors required for the low frequency filters in [1,5,6,9,15,17]. In [20,21], a pseudo differential floating capacitor multiplier consisting of two grounded capacitor multipliers is reported. A current mode floating capacitor multiplier with differential unity gain amplifier and dual output current mirror is reported in [22]. However, Current mode impedance scalers cannot be used for realizing fully differential floating capacitors required for fully differential band-pass, high-pass and low pass filters with low cut off frequencies. To overcome this problem, a symmetrical

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floating impedance scaler denoted as Source Follower based Symmetrical Floating Impedance Scaler (SF-SFIS) circuit is proposed in [23–25]. It consists of a pair of source followers whose currents are multiplied by a factor N and fedback to the inputs. However, higher multiplication factor in SF-SFIS reduce low frequency limit of equivalent capacitor and, the accuracy of this circuit is lower and not able to detect and multiply small value of base capacitor (C_b).

To overcome the limitations in SF-SFIS, an impedance scaler denoted as Flipped Voltage Follower based Symmetrical Floating Impedance Scaler (FVF-SFIS) is proposed in this paper. The proposed FVF-SFIS circuit feasibility is confirmed and compared with SF-SFIS circuit by the design of a fully differential 3rd order Chebyshev LPF by simulation.

This paper is organized as follows: In Section 2, an overview of the SF-SFIS circuit and its limitations are presented. In Section 3, the details of the FVF-SFIS proposed in this paper are presented. In Section 4, the impedance function of FVF-SFIS is derived using the equivalent small signal half circuit. In Section 5, the post-layout simulation results on the implementation of 500 pF capacitors in UMC 180 nm technology using both FVF-SFIS and SF-SFIS are presented. Results on the equivalent capacitance and accuracy in terms of %error due to process, voltage, and temperature variations are presented, additionally SF-SFIS and FVF-SFIS circuits equivalent capacitance and accuracy in terms of %error are compared by considering various multiplication factor and base capacitor in this section. In Section 6, the results on the implementation of 3rd order Chebyshev LPF using capacitors realized using FVF-SFIS and SF-SFIS are given. In Section 7, the expression for the common mode impedance of the FVF- SFIS is derived. Section 8 concludes this paper.

2. Conventional source follower based symmetrical floating impedance scaler

The circuit diagram of source follower based symmetrical floating impedance scaler [SF-SFIS] proposed in [23–25] and the bias circuit used are shown in Fig. 1a and b. The small signal current through base capacitor (C_b) is sensed by transistors M6 (M5) and mirrored to differential input terminals through transistors M10 (M9) with mirror gain N. The equivalent capacitance between the differential input terminals is NC_b [23–25]. The cascode transistors M11-M14 are used in Fig. 1a to improve the impedance in input terminals.

Since gate terminal of M12 (M11) are connected to a constant voltage, the finite drain to source impedance of transistor M6 (M5), which results in poor accuracy for equivalent capacitor (C_{equ}).

The total current (I_{total}) consumed by the SF-SFIS can be shown to be

$$I_{total} = 2I_R(N+2) \tag{1}$$

where I_R is the reference current. From Eq. (1) total current consumption of SF-SFIS linearly increases with N. This leads to higher power dissipation as N increases. The drain-source resistance (r_o) of transistors M9-10 is decreases as N increases ($r_o = 1/\lambda N I_R$), it reduce the low frequency limit of the equivalent capacitor C_{equ} [20,21].

The major limitations of the SF-SFIS circuit are poor accuracy and higher power dissipation. We propose FVF-SFIS circuit to overcome these limitations.

3. Proposed flipped voltage follower based symmetrical floating impedance scaler circuit

The proposed Flipped Voltage Follower based Symmetrical Floating Impedance Scaler (FVF – SFIS) circuit is shown in Fig. 2. (The bias circuit shown in Fig. 1b is used in FVF – SFIS). The differential signals v_{in2} and v_{in1} are fed to the gates of the transistors M_1 and M_1'.

The differential inputs are also fed to the gates of M_3 (M_3') in order to make the voltages at the drains of M_2 and M_4 (M_2' and M_4') to be equal. The parasitic current in the output impedance of M2 (M2′) is efficiently canceled by its counterpart M3 (M3′) and M4 (M4′) transistors; hence, the small signal drain current of M3 (M3′) is an accurate imitation of a small signal current flowing through base capacitor (C_b) [9]. The small signal drain current in M_3 (M_3') is scaled up and fed back to input terminals v_{in1} (v_{in2}) through the cascaded current mirror stages M_7-M_{10}, M_{11}-M_{14} and M_{15}-M_{18} (M_7'-M_{10}', $M_{11'}$-M_{14}' and M_{15}'-M_{18}') with a current gain of N_1, N_2, and N_3 respectively. The equivalent capacitance between the terminals v_{in1} and v_{in2} is equal to $N_1N_2N_3C_b$. The transistors M_1 and M_2 (M_1' and M_2') act as a flipped voltage follower, since the drain terminal of M_1 (M_1'), is connected to the gate terminal of M_2 (M_2') which introduces shunt feedback and reduces the resistance at the source of M_1 (M_1') to $1/(g_{m1}g_{m2}r_{o2})$. This increases the high-frequency limit of the equivalent capacitor (C_{equ}).

The total current consumption of the proposed circuit is given by

$$I_{total} = 2(N_1+N_2+N_3+4)I_R \tag{2}$$

From Eqs. (1) and (2), it may be noted that the current and the power consumption of FVF-SFIS are $(N+2)/(N_1+N_2+N_3+4)$ times lower than that of SF-SFIS circuit when the reference currents of both FVF-SFIS and SF-SFIS are set to be equal. For example,

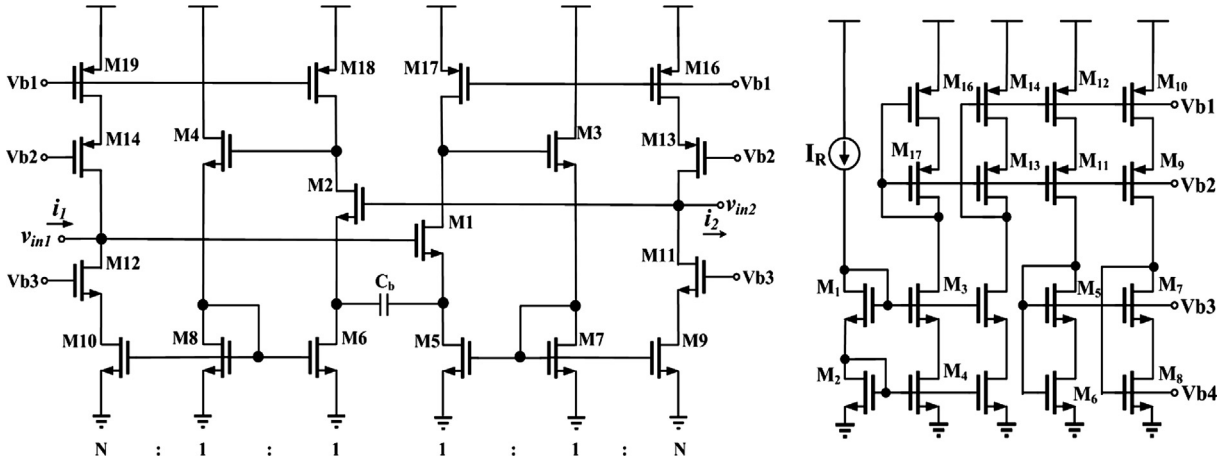


Fig. 1. (a) Circuit diagram of SF-SFIS [19–21]. (b) Bias circuit used for SF-SFIS.

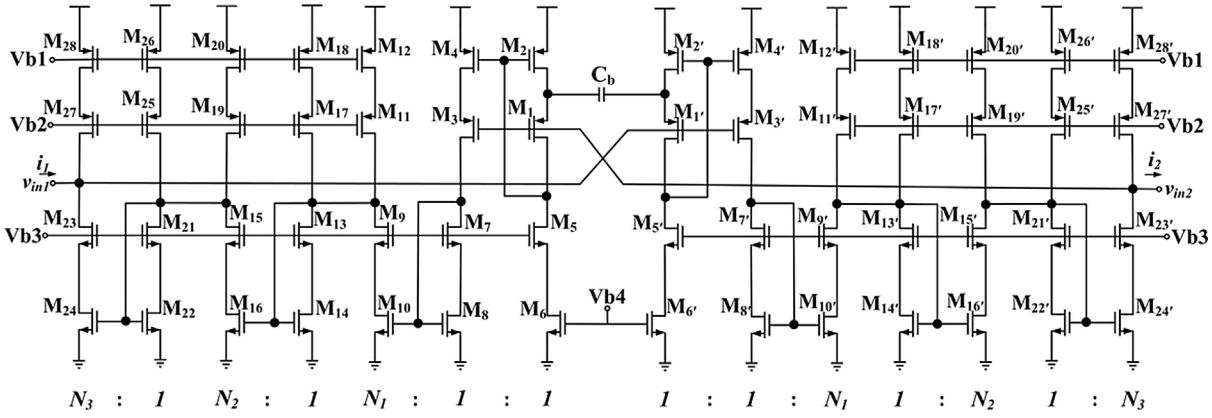


Fig. 2. Proposed FVF – SFIS.

for $N = 100$, $N_1 = N_2 = 5$, and $N_3 = 4$, The power and current consumption of FVF-SFIS is 5.66 times lower. Hence, the cascaded current mirror stages reduce current consumption and area, able to achieve a high multiplication factor.

4. Frequency analysis

Small signal half circuit equivalent of the FVF-SFIS circuit is given in Fig. 3. It may be noted that for proper operation impedance scaler, the transistors in Fig. 2 should be sized and biased such that

$$\left.\begin{aligned} &g_{m10} = N_1 g_{mn};\ g_{m16} = N_2 g_{mn};\ g_{m24} = N_3 g_{mn} \\ &g_{m8} = g_{m14} = g_{m22} = g_{mn};\ g_{m1} = g_{m3} = g_{m2} = g_{m4} = g_{mp} \end{aligned}\right\} \tag{3}$$

At node d, the resistance due to cascode stage formed by M_3, M_4 is very high compared to the impedance $(1/g_m)$ of the diode-connected cascode stage formed by M_7, M_8 and hence, the former can be neglected. The same observations are valid for nodes e and f. In Fig. 3, R_{D6} represents the impedance of the cascode stage formed by M_{27} and M_{28}, in parallel with the cascode stage formed by M_{23} and M_{24} and R_{D1} represents the impedance of the cascode stage formed by M_{25} and M_{26} in Fig. 2. Hence, R_{D6} and R_{D1} can be written as

$$R_{D6} \simeq g_{m23} r_{023} r_{024} \| g_{m27} r_{027} r_{028} \tag{4}$$

$$R_{D1} \simeq g_{m5} r_{05} r_{06} \tag{5}$$

The expressions for R_{D4} and R_{D2} can be obtained by substituting equivalent impedance of transistors corresponding to cascode stages at node f and e respectively in Eq. (4). Similarly, the expressions for R_{D3} and R_{D5} can be obtained by substituting equivalent impedance of transistors corresponding to cascode stage at node e and f respectively in Eq. (5).

Assuming that $g_m r_o \gg 1$ the impedance Z_1 of the half circuit is given by

$$Z_1 = \frac{v_{in1}}{i_1} \simeq \frac{\left[S + \frac{g_{m1} g_{m2} R_{D1}}{2C_b}\right]}{N_1 N_2 N_3 g_{m1} g_{m4} R_{D1} \left[S + \frac{1}{N_1 N_2 N_3 2C_b}\left(\frac{N_1 N_2 N_3}{r_{o2}} + \frac{1}{R_{D6}}\right)\right]} \tag{6}$$

From Eq. (6), it may be noted that the pole ω_p and the zero ω_z of Z_1 are given by

$$\omega_p \simeq \frac{1}{N_1 N_2 N_3 2C_b}\left(\frac{1}{R_{D6}} + \frac{N_1 N_2 N_3}{r_{o2}}\right) \tag{7}$$

$$\omega_z \simeq \frac{g_{m1} g_{m2} R_{D1}}{2C_b} \simeq \frac{g_{m1} g_{m2} g_{m5} r_{05} r_{06}}{2C_b} \tag{8}$$

From Eqs. (7) and (8), it may be noted that $\omega_p \ll \omega_z$. Z_1 Operates as a capacitor in the frequency range $\omega_p \ll \omega \ll \omega_z$. The impedance of the proposed circuit between nodes v_{in1} and v_{in2} is given by

$$Z_{sc} = 2Z_1 \simeq \frac{2}{N_1 N_2 N_3 g_{m1} g_{m4} R_{D1}} \frac{\omega_z\left(\frac{s}{\omega_z} + 1\right)}{s\left(1 + \frac{\omega_p}{s}\right)} \tag{9}$$

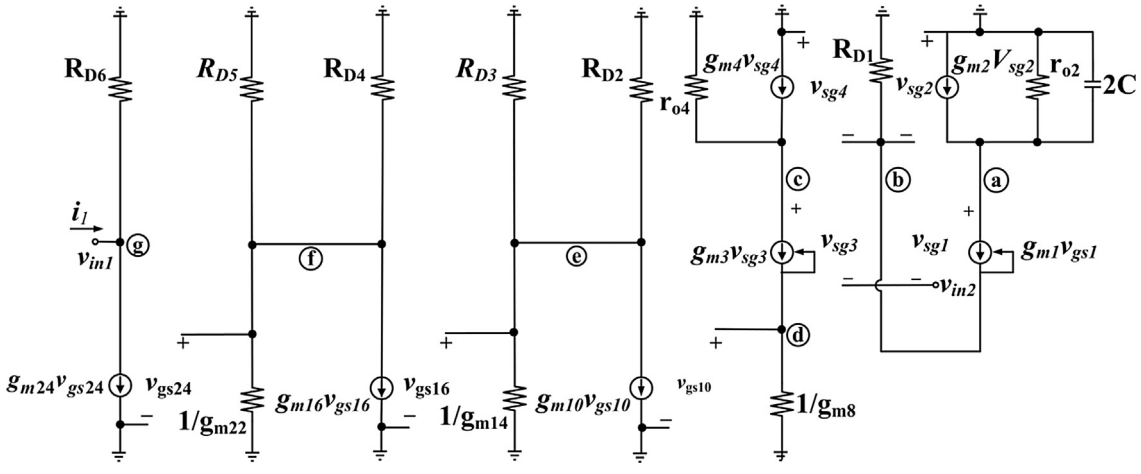


Fig. 3. Small-signal equivalent half circuit of FVF-SFIS.

Since $\omega_p \ll \omega \ll \omega_z$, Eq. (9) can be rewritten as

$$Z_{sc} \simeq \frac{2}{N_1 N_2 N_3 g_{m1} g_{m4} R_{D1}} \frac{\frac{g_{m1} g_{m2} R_{D1}}{2C_b}}{s} \tag{10}$$

By using Eq. (3), ($g_{m2} \equiv g_{m4}$) in (10), we get,

$$Z_{sc} \simeq \frac{1}{sN_1 N_2 N_3 C_b} \tag{11}$$

Hence, the proposed circuit multiplies the base capacitor (C_b) by "$N_1N_2N_3$".

Table 1
Size of the transistors of SF-SFIS and FVF-SFIS.

SF-SFIS		FVF-SFIS	
Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M1-M8	0.96/10	M_1-M_4($M_{1'}$-$M_{4'}$) M_{17}-M_{18}($M_{17'}$-$M_{18'}$) M_{25}-M_{26}($M_{25'}$-$M_{26'}$)	0.96/5
M9-M12	48/10	M_{11}-M_{12}($M_{11'}$-$M_{12'}$) M_{19}-M_{20}($M_{19'}$-$M_{20'}$) M_{27}-M_{28}($M_{27'}$-$M_{28'}$)	4.8/5 1.92/5
M17-M18, M15	0.96/5	M_1-M_2($M_{1'}$-$M_{2'}$) M_5-M_8($M_{5'}$-$M_{8'}$)	0.96/10
M13-14, M16, M19	48/5	M_9-M_{10}($M_{9'}$-$M_{10'}$) M_{15}-M_{16}($M_{15'}$-$M_{16'}$) M_{23}-M_{24}($M_{23'}$-$M_{24'}$)	4.8/10 1.92/10

5. Simulation results

5.1. Simulation and comparison of SF-SFIS and FVF-SFIS

In order to evaluate the performance of the proposed FVF-SFIS and to compare its performance with SF-SFIS, an equivalent capacitance of 500 pF is realized using both of these circuits in UMC 180 nm technology [29] with a base capacitance of 10 pF, the supply voltage of 1.8 V and bias current of 100 nA. The multiplication factors used for the current mirrors are formed by M_7-M_{10}, M_{11}-M_{14}, and M_{15}-M_{18} ($M_{7'}$-$M_{10'}$, $M_{11'}$-$M_{14'}$, and $M_{15'}$-$M_{18'}$) are chosen to be 5, 5 and 2 respectively. The size of the transistors used in the FVF-SFIS and SF-SFIS are given in Table 1. The layout of both FVF-SFIS and SF-SFIS are shown in Fig. 4. The impedance and phase of the impedance scalers using both the circuits are obtained through post-layout simulation, and the results are given in Fig. 5a and b respectively. From Fig. 5a, it may be noted that the variation of the amplitude of the impedance of the FVF-SFIS with

Table 2
Power consumption and area of the SF-SFIS and the FVF-SFIS.

	Power (μW)	Area (mm^2)	Frequency range (Hz)	Base capacitor (pF)
SF-SFIS	18.72	0.095	10–30 k	10
FVF-SFIS	5.76	0.046	2–28 k	10

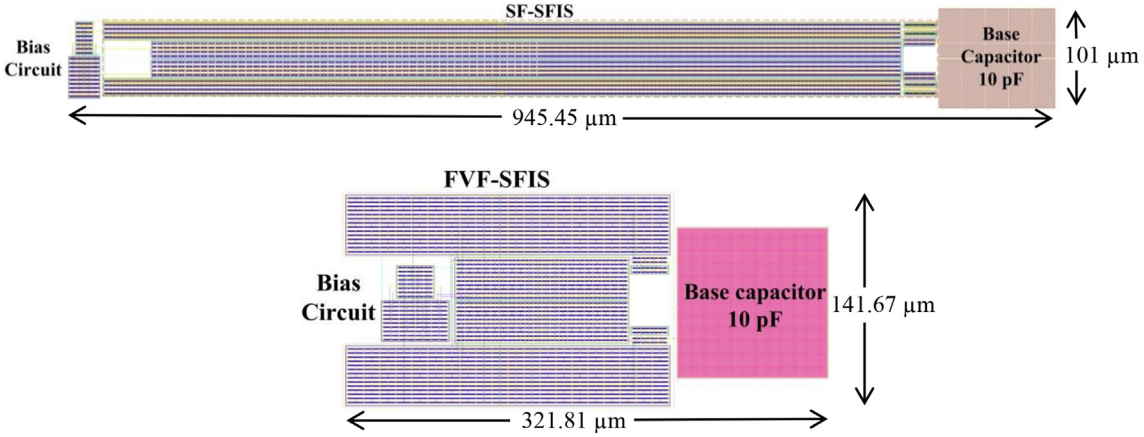


Fig. 4. Layout of the SF-SFIS and FVF-SFIS.

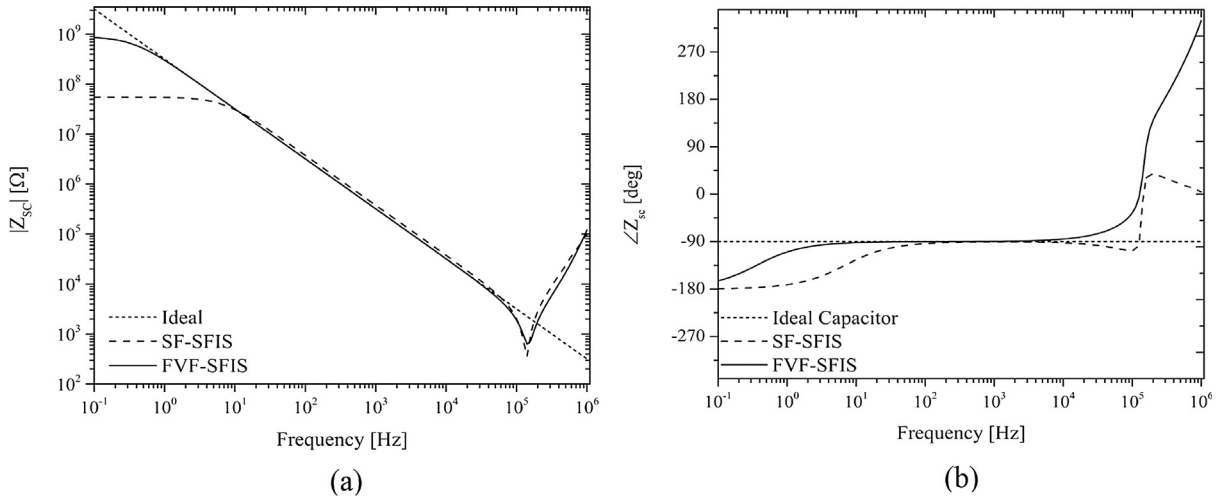


Fig. 5. (a) Magnitude of Z_{SC} for the SF-SFIS, the FVF-SFIS and an ideal capacitor. (b) Phase of Z_{SC} for the SF-SFIS, the FVF-SFIS and an ideal capacitor.

Table 3
C_{equ} and %error in C_{equ} for various VDD, temperature, and process corners.

	Supply variation			Temperature variation			Process variation				
	1.68 V (−10%)	1.8 V	1.92 V (+10%)	−50°	27°	70°	tt	ff	ss	fnsp	snfp
Equivalent capacitance C_{equ} (pF)	457.13	493.35	437.73	499.79	493.35	468.88	493.35	469.34	481.49	491.08	489.47
%Error	−8.57	−1.33	−12.4	−0.032	−1.33	−6.2	−1.33	−6.13	−3.70	−1.78	−2.10

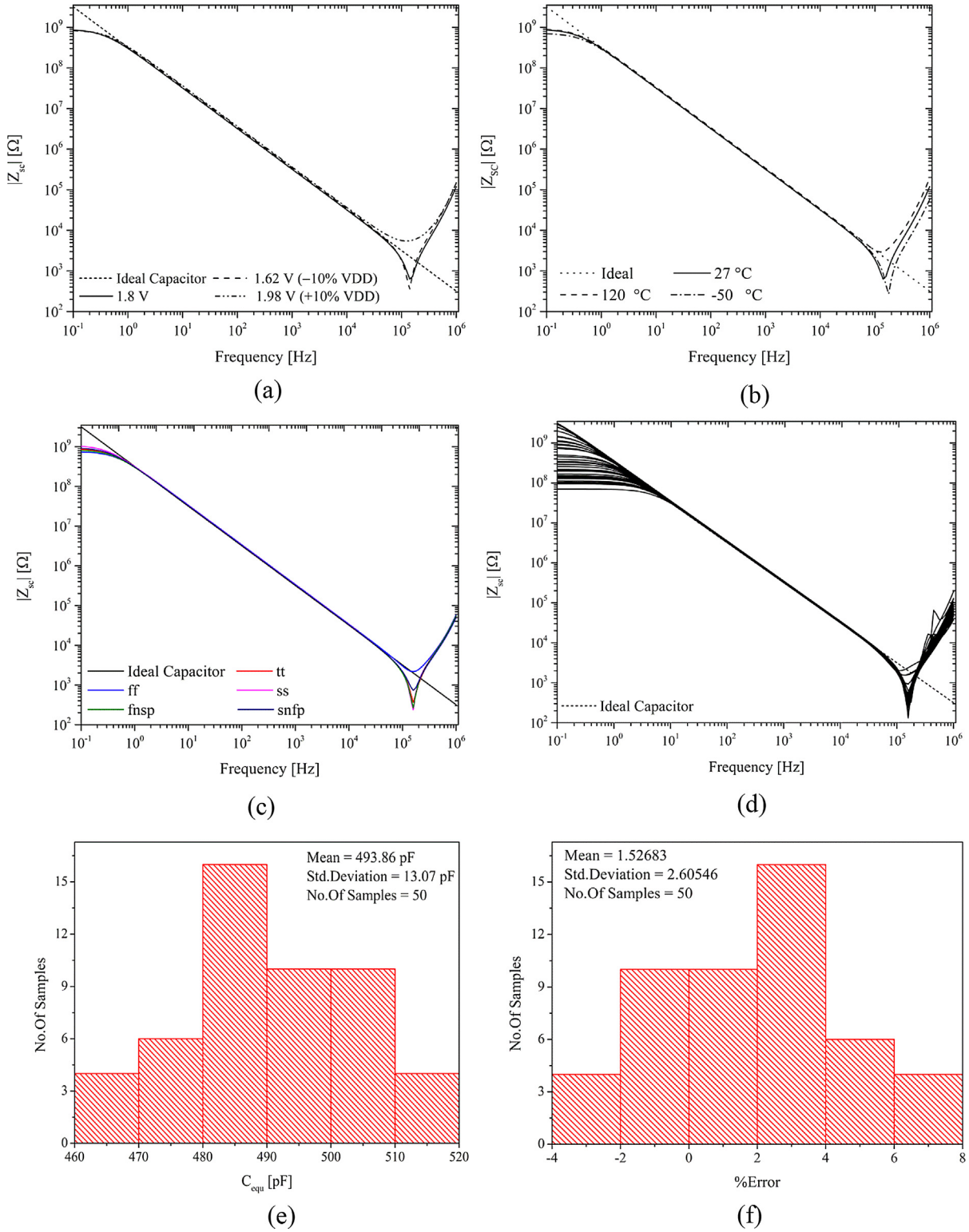


Fig. 6. Supply, temperature, corner and Monte Carlo simulation of the proposed circuit.

Table 4
C_{equ} and % error in C_{equ} for various base capacitors and multiplication factors.

Base capacitor C_b (F)	Multiplication factor	SF-SFIS		FVF-SFIS	
		C_{equ}	% Error	C_{equ}	% Error
50f	1	48.43f	−3.14	45.46f	−9.08
	8	373.88f	−6.53	388.47f	−2.88
	125	6.54p	+4.64	6.17p	−1.28
	1000	51.32p	+2.64	49.06p	−1.88
100f	1	90.5f	−9.5	94.77f	−5.23
	8	710.93f	−11.13	784.69f	−1.91
	125	11.80p	−5.6	12.35p	−1.2
	1000	95.56p	−4.44	98.46p	−1.54
1p	1	851.96f	−14.8	987.34f	−1.26
	8	6.80p	−15	7.92p	−1
	125	107.10p	−14.32	123.68p	−1.06
	1000	902.81p	−9.72	989.62p	−1.04
10p	1	8.47p	−15.3	9.91p	−0.9
	8	67.71p	−15.36	79.27p	−0.91
	125	1.06n	−15.2	1.24n	−0.8
	1000	8.52n	−14.8	9.90n	−1

frequency is the same as that of an ideal 500 pF capacitor in the frequency range 2 Hz to 28 kHz. SF-SFIS operates as a capacitor in the range 10 Hz to 30 kHz, and its range is smaller than that of FVF-SFIS. The phase of the impedance realized using both FVF-SFIS and SF-SFIS as a function of frequency are shown in Fig. 5b. The performance metrics such as power consumption, the occupied area and frequency range of both SF-SFIS and the proposed circuit are given in Table 2. It is observed that the power dissipation of the proposed circuit is 3.25 times less compared to that of SF-SFIS. This is expected, as the total current computed using Eqs. (1) and (2) for the SF-SFIS, and the proposed circuit are $32I_R$ and $104I_R$ respectively. As the result, the proposed circuit requires 51.58% lower area than SF-SFIS.

5.2. Study of the process, voltage and temperature variations of the FVF-SFIS

The impedance frequency characteristics of the FVF-SFIS impedance scaler used for realizing a 500 pF capacitor using a base capacitor of 10 pF is evaluated under different supply voltages (1.98 V(+10%, of Vdd), 1.8 V, 1.62 V (−10% of Vdd)), temperatures (−50 °C, 27 °C, 70 °C) and process corners (tt, ff, fnsp, ss, and snfp) through simulations. As in [9], the C_{equ} of the impedance scaler and the %error in C_{equ} is calculated by considering the bandwidth, where phase error is $\leq\pm1^\circ$ with respect to -90°. $f_{1^\circ L}$ and $f_{1^\circ H}$ denote the lower and upper limits of the frequencies where the phase error is $\leq\pm1^\circ$. If f^* is any frequency within this range and $|Z_{SC}(f^*)|$ is the magnitude of the input impedance, then the equivalent capacitance C_{equ} is given by

$$C_{equ} = [|Z_{sc}(f^*)|2\pi f^*]^{-1} \tag{12}$$

For each case, C_{equ} obtained, and %error in the C_{equ} are calculated and are given in Table 3. The maximum %error in C_{equ} due to variation in the supply voltage, temperature, and process corner is found to be −12.4%, −6.2%, and −6.13% respectively. For a supply voltage of 1.8 V and temperature of 27 °C, the amplitude of the impedance realized using FVF-SFIS, are obtained using post-layout simulation for various process corners such as tt, ff, ss, fnsp, and snfp and the results are shown in Fig. 6. Since the current mirror stages M_7-M_{10}, M_{11}-M_{14}, and M_{15}-M_{18} ($M_{7'}$-$M_{10'}$, $M_{11'}$-$M_{14'}$, and $M_{15'}$-$M_{18'}$) use NMOS devices, for fast corners, the drain current is higher due to higher mobility, thinner gate oxide, and lower threshold voltage. The parasitic resistors, inductors, capacitors extracted from the layout are considered to be MIN in the fast corner as it corresponds to high currents and higher speed. Hence, the fast corner has poor accuracy compared to other corners. The reverse is true for slow corners [27].

The FVF-SFIS circuit is studied through Montecarlo simulation using 50 runs and the results shown in Fig. 6d. Fig. 6e–f shows histogram plots of the equivalent capacitor C_{equ} and its corresponding %error. The Mean and the standard deviations of samples variations are acceptable and show the robustness of proposed FVF-SFIS. It can be noted that the impedance of the FVF-SFIS matches with that of an ideal capacitor in the band of interest despite the mismatches in the transistors.

In order to study the accuracy of both of the impedance scalers, equivalent capacitance (C_{equ}) and the %error in C_{equ} obtained using both FVF-SFIS and SF-SFIS are found through simulation for a set of base capacitors (50 fF, 100 fF, 1 pF and 10 pF) and the scaling factors (1, 8, 125, and 1000), and the results are given in Table 4. From this table, it may be noted that error in C_{equ}, due to the parasitic capacitance which is in parallel with Z_{sc}, and its effect is negligible when both multiplication factor and base capacitor are large. The % error in C_{equ} of the FVF-SFIS is about −1.3%, and it is less compared to that of the SF-SFIS which is about −15%.

6. Implementation 3rd order fully differential Chebyshev LPF filter using FVF-SFIS

The capacitors realized using the proposed FVF-SFIS circuit is used for the implementation of a fully differential 3rd order G_m-C Chebyshev Low Pass Filter (LPF) with pass-band ripple of 0.5 dB and cut-off frequency of 100 Hz. The block diagram of the fully differential filter is shown in Fig. 7a. RLC equivalent of the filter is shown in Fig. 7b.

For the 3rd order G_m-C Chebyshev LPF, the capacitor values can be expressed in terms of the transconductance (g_m) of the OTA and the cut-off frequency (f_c) as follows:

$$\left.\begin{aligned} CC1 &= \tfrac{1.5963\times g_{m1}}{2\pi\times f_{cut-off}};\ CC2 = \tfrac{1.0967\times g_{m2}}{2\pi\times f_{cut-off}} \\ CC3 &= \tfrac{1.5963\times g_{m3}}{2\pi\times f_{cut-off}} \end{aligned}\right\} \tag{13}$$

From Eq. (13), it may be noted that the cut-off frequency can be reduced either by reducing the g_m or by increasing the capacitor. However, the noise is inversely proportional to g_m. For a cut-off frequency of 100 Hz, higher sized capacitors are required to reduce the noise level. Hence, the capacitors CC1, CC2 and CC3 shown in Fig. 7a are chosen to be large and realized using SF-SFIS, FVF-SFIS impedance scalers, and Ideal capacitors.

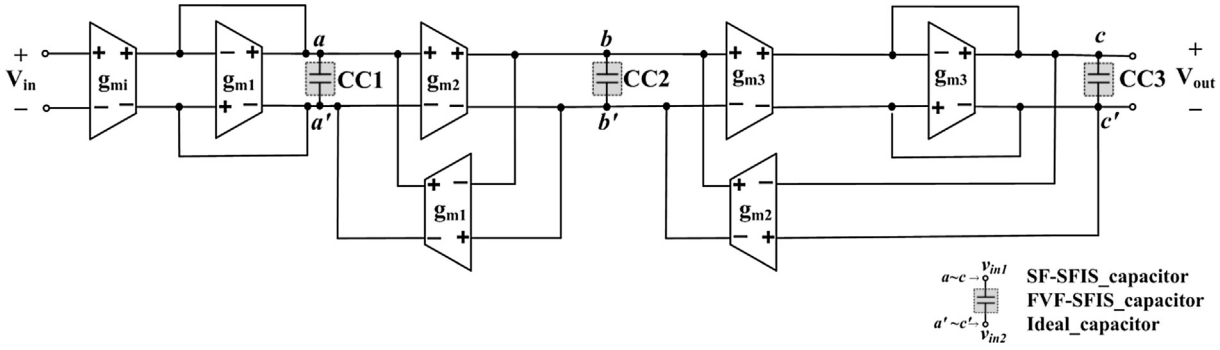
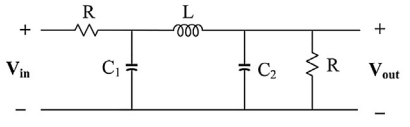


Fig. 7a. 3rd order G_m-C Chebyshev Low Pass Filter.



$R: 1\Omega$
$C_1 \& C_2: 1.5963F$
$L: 1.0967H$

Fig. 7b. 3rd Order Passive Filter.

The linearized low g_m OTA proposed in [26] is used to realize the g_{m1}-g_{m3} blocks in this paper and is shown in Fig. 8a. Is a fully differential OTA using current division (transistor M_M) and current cancellation (transistor M_N) techniques to achieve low g_m. Moreover, a source-degeneration transistor (M_R) operating in the triode region with drain to source conductance $g_{o,MR}$ is used to enhance the linearity and to minimize the harmonic distortion components [26]. The drain current in transistor M_R is divided by transistors M_M, M_N, and M_1. The overall transconductance of the OTA in Fig. 8a is given by [26].

$$G_m = \frac{i_{out}}{v_{id}} = \frac{1-N}{1+N+M} \cdot g_{oMR} \tag{14}$$

Assuming the bias current of 100nA in each of the tail current sources and supply voltage of 1.8 V, the dimensions of the transistors of the OTA implemented in UMC 180 nm technology are given in Table 5. For this bias current, the effective G_m each of the OTAs in Fig. 8a is 280 nS. The common mode feedback (CMFB) circuit is necessary to ensure the common mode (CM) signal level at the output to be VDD/2 in the fully differential (FD) OTAs. The CMFB circuit used in LPF is shown in Fig. 8b. The current through tail current source in the CMFB circuit is also assumed to be 100 nA. The size of the transistors used for the CMFB circuit is shown in Table 5.

Table 5
Transistor size of linearized Low g_m OTA and CMFB circuit.

Linearized low g_m OTA		CMFB circuit	
Transistor	W/L [μm/μm]	Transistor	W/L [μm/μm]
M_{BP1}-M_{BP2}	0.96/5	M_{BP1} – M_{BP2}	0.96/5
M_{BN1}-M_{BN2}	0.96/10	M_{VCM1}-M_{VCM2} M_{VCM}	1.92/5
M_M	3.8/5	M_{BN1}-M_{BN2}	0.96/10
M_N	2.88/5		
M_1	0.96/5		
M_R	30/50		
M_C	0.24/27.5		
M_{CN}	1.6/15		

The power consumption of the CMFB circuit is 360 nW. To reduce the power consumption of the 3rd order Chebyshev LPF, three common mode feedback (CMFB) circuits are used to sense the common mode voltages at the output nodes $a \sim c$ ($a' \sim c'$) and generate the control voltage (v_{fb}) for all the seven OTAs in the Fig. 8a. The 3rd order Chebyshev LPF with cut-off frequency (f_c) of 100 Hz is realized assuming transconductance of the each of the OTAs, g_{m1}, g_{m2}, and g_{m3} to be 280 nS. The values of capacitors

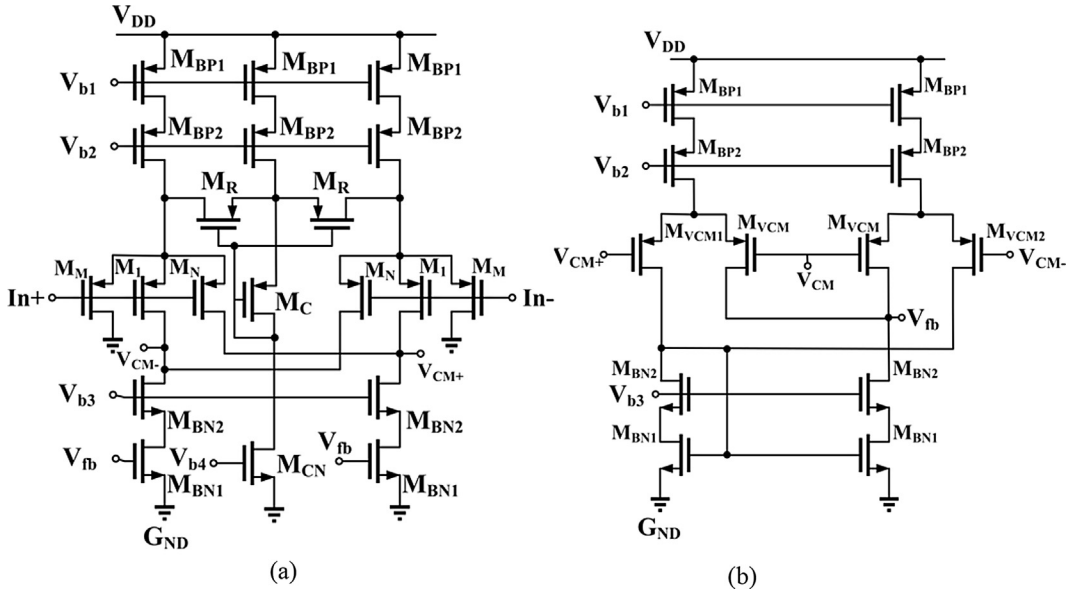


Fig. 8. (a) Linearized Low g_m OTA (b) Common mode feedback circuit.

CC1, CC2, and CC3, computed using Eq. (13) are 711.37 pF, 488.73 pF, and 711.37 pF respectively. These capacitors are realized using the FVF-SFIS and SF-SFIS (a base capacitor of 14.23 pF, 9.77 pF and 14.23 pF respectively with a multiplication factor of 50. (for FVF-SFIS $N_1 = N_2 = 5$, and $N_3 = 2$ and for SF-SFIS N = 50 is considered).

6.1. Filter simulation results

The frequency response of the LPF using ideal capacitor, the proposed FVF-SFIS, and conventional SF-SFIS are shown in Fig. 9a. These are indicated by short dashed line, solid line, and

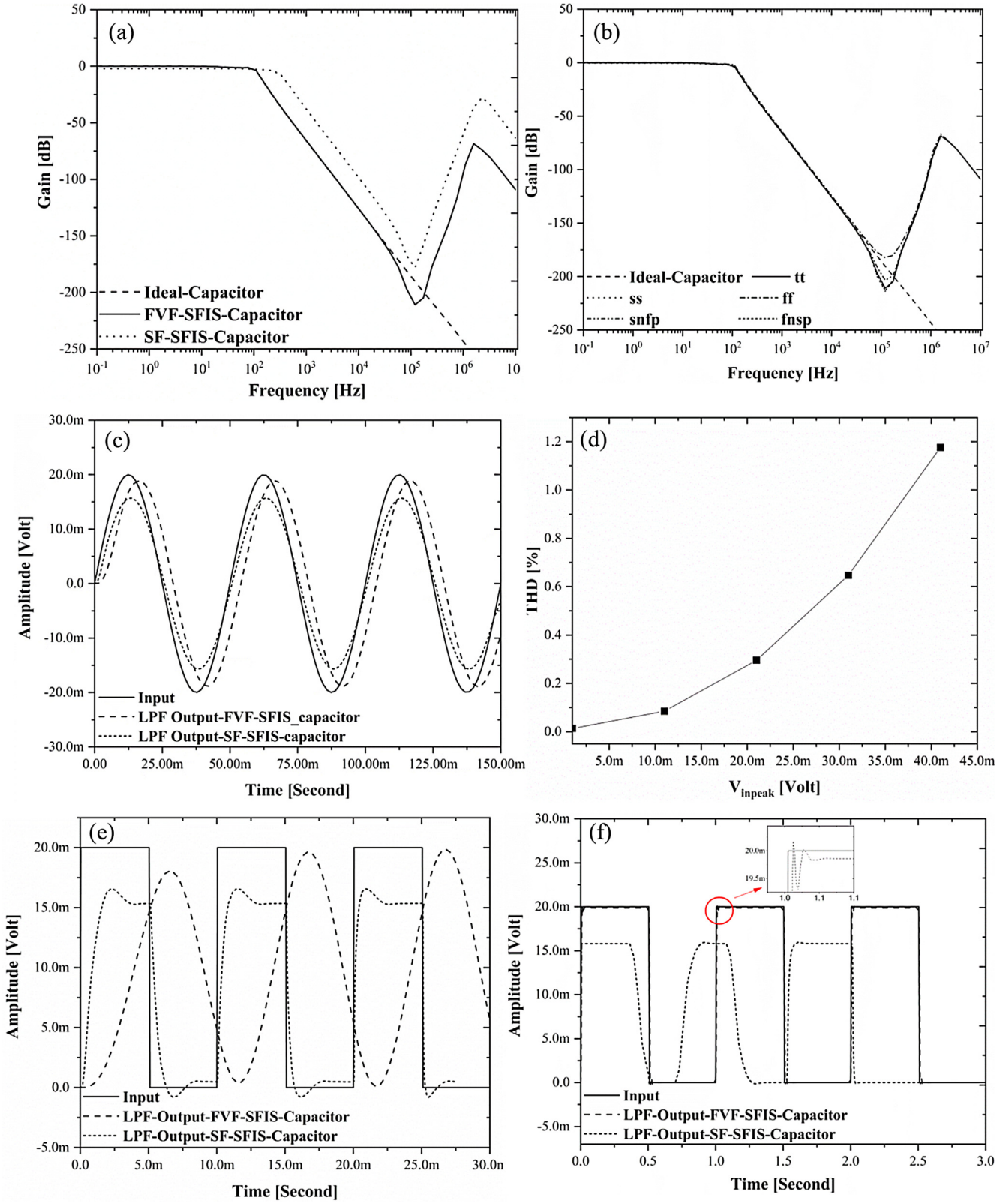


Fig. 9. (a) Frequency Response for typical corner (b) Frequency Response for different corners (c) Transient Response of LPF using FVF-SFIS and SF-SFIS for 20 Hz Sine wave (d) THD of LPF for different V_{inpeak} (e) Transient response of LPF for 100 Hz square wave (f) Transient response of LPF for 1 Hz square wave.

dotted lines respectively. Fig. 9a proves the LPF response using the proposed FVF-SFIS circuit cut-off frequency is closer to LPF response using Ideal capacitor and more accuracy compared to LPF using conventional SF-SFIS circuit, and the corresponding results are tabulated in Table 6. The frequency response of the LPF using the proposed FVF-SFIS under various process corners (ff, fnsp, ss, snfp, and tt) are studied through simulation and is shown in Fig. 9b. The passband gain and the cut-off frequency of the LPF for various corners are given in Table 7. The worst case deviation in the cut-off frequency is observed in ff corner.

Transient response of the LPF shown in Fig. 7a for a 20 Hz sine wave with the peak input voltage (Vinpeak) of 20 mV is obtained, and the results are given in Fig. 9c From Fig. 9c, it is observed that the attenuation and the phase shift between input and the output of the LPF with FVF-SFIS are smaller than that obtained using SF-SFIS circuit. The total harmonic distortion of LPF output is obtained by varying the peak voltage of the sine wave, and the results are given in Fig. 9d. From this, it may be noted that that THD of 1% occurs for Vinpeak of 36.7 mV. A 100 Hz square wave input with Vinpeak of 20 mV is applied to LPF, and the output of the filter is shown in Fig. 9e. From this, it is noted that the harmonics of square wave input is eliminated better with the LPF using FVF-SFIS than that with SF-SFIS. Fig. 9f shows under-damped output response [28] of the LPF with FVF-SFIS and SF-SFIS when 1 Hz square wave is applied to the LPF.

Table 6
Passband gain and the cut-off frequency of LPF.

	Passband gain (dB)	Cut-off frequency (Hz)
Ideal capacitor	0	100
SF-SFIS capacitor	−0.702	267.63
FVF-SFIS capacitor	−0.597	105.46

Table 7
Passband gain and cut-off frequency for different corners.

Type of corner	Passband gain (dB)	Cut-off frequency (Hz)
tt	−0.597	105.46
ff	−1.38	112.13
fnsp	−0.052	95.68
ss	−1.3	85.57
snfp	−0.917	104.02

7. Common-Mode impedance characteristics of FVF-SFIS

In this section, the common mode impedance of the proposed FVF-SFIS is derived and compared with that of SF-SFIS. In Fig. 7a, the common mode voltages of OTA g_{m1}, g_{m2} and g_{m3} are same. For example, common mode node voltages at *a*, and *a′* are the same. Hence, the current through the capacitor CC1 should be ideally zero. However, when CC1 is realized using FVF –SFIS, the common mode impedance (Z_{CM}) at the input v_{in1} and v_{in2} of the FVF-SFIS load the output of node *a*, and *a′*.

To minimize this loading, Z_{CM} should be made larger. An expression for Z_{CM} can be obtained as follows: When common mode input voltage (V_{cm}) is applied to FVF-SFIS, the output voltages of the flipped voltage followers in Fig. 2 are equal. i.e., the voltages at the two ends of the base capacitors (C_b) are equal, and the base capacitor acts as an open circuit; hence it can be removed in the equivalent circuit. Assuming $g_m r_o >> 1$ and making $v_{in1} \equiv v_{in2}$ in the half circuit equivalent given in Fig. 3 Z_{CM} can be shown to be,

$$Z_{CM} \simeq \frac{g_{m22}g_{m8}g_{m14}g_{m1}g_{m2}r_{o2}R_{D6}R_{D6}R_{D1}}{g_{m22}g_{m8}g_{m14}g_{m1}g_{m2}r_{o2}R_{D1} + g_{m24}g_{m16}g_{m10}g_{m3}g_{m1}R_{D1}R_{D6}} \tag{15}$$

Using Eq. (3) in (15), Z_{CM} becomes.

$$Z_{CM} \simeq \frac{(g_{mn})^3(g_{mp})^2 r_{o2}R_{D6}R_{D1}}{(g_{mn})^3(g_{mp})^2 r_{o2}R_{D1} + N_1N_2N_3(g_{mn})^3(g_{mp})^2 R_{D1}R_{D6}} \tag{16}$$

$$Z_{CM} \cong \frac{r_{o2}}{N_1N_2N_3} \tag{17}$$

The amplitude and phase characteristics of the common mode impedance of SF-SFIS and FVF-SFIS are obtained through simulation and are given in Fig. 10. From this figure, it may be noted that for the proposed FVF-SFIS, common mode impedance (Z_{CM}) is more than one decade larger compared to SF-SFIS. Since Z_{CM} for SF-SFIS is smaller to reduce the offset error, the bias current in CMFB is chosen to be ten times larger than of SF-SFIS [23]. However, when FVF-SFIS is used, bias currents of both FVF-SFIS and CMFB can be chosen to be the same. Hence, FVF-SFIS can be used to realize the capacitors for LPF, with less power consumption compared to SF-SFIS.

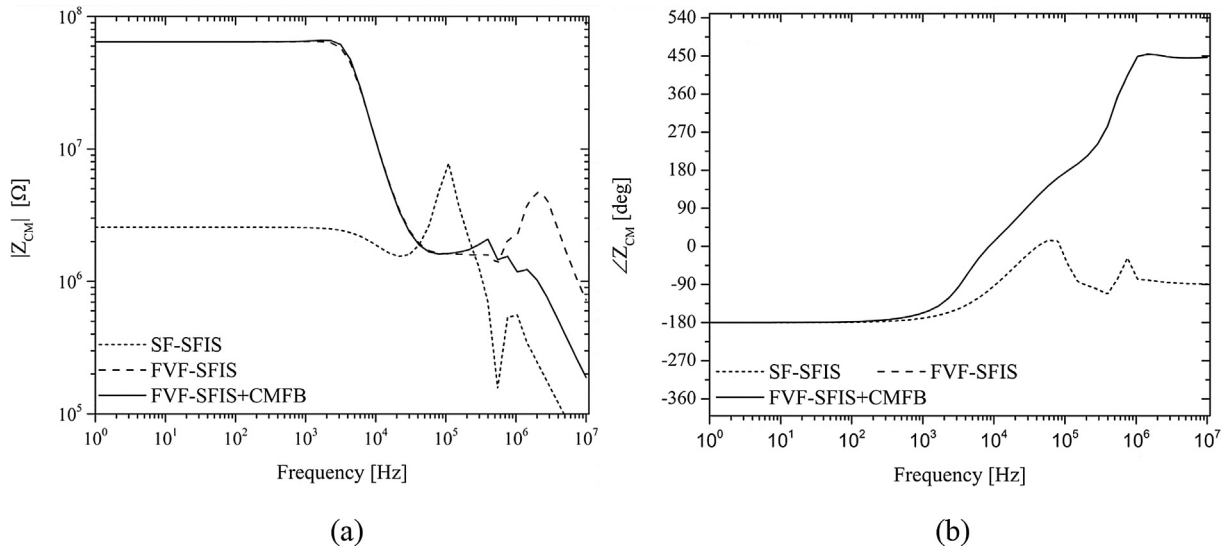


Fig. 10. Common mode impedance characteristics.

8. Conclusions

Flipped voltage follower based symmetrical floating impedance scaler proposed in this paper is used to realize a 500 pF in UMC 180 nm technology and studied through post-layout simulation. Its performance is also studied under different PVT and mismatches. From these studies, it is found that the proposed circuit has lower power dissipation, lower area, and higher accuracy compared to the SF-SFIS reported in the prior works. The proposed circuit is also used to realize capacitors required for a fully differential third order Chebyshev low-pass filter. The frequency response of this filter matches with that using ideal capacitors. The common mode impedance of the proposed circuit is larger than that of SF-SFIS, and this reduces the power consumption of the common mode feedback circuits used in the filter. The proposed impedance scaler can be used to realize floating impedance scalers for fully differential filters in biomedical applications.

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Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.aeue.2019.04.025.

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