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# Body-Biased Subthreshold Bootstrapped CMOS Driver*

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This paper proposes a body-biased bootstrapped CMOS driver for subthreshold applications. The proposed driver has been implemented with the same number of transistors as conventional bootstrapped CMOS driver. The performance of the subthreshold bootstrapped CMOS driver has been compared with the conventional bootstrapped CMOS driver. Our results show that the proposed body-biased subthreshold bootstrapped CMOS driver has 37% reduction in delay and 39% reduction in power dissipation compared to conventional bootstrapped CMOS driver. The proposed driver is more suitable to drive large loads compared to the conventional driver and operates better at subthreshold region.

*Keywords*: CMOS driver; bootstrapping; body biasing; subthreshold.



## 1. Introduction

Interconnects are used to carry the signals between transistors in integrated circuits (IC's). These interconnects have large RC load, which leads to delay. CMOS inverters are used as drivers to carry the signals for the interconnects. Operating the CMOS devices with lower voltage leads to reduced speed. The signal of the CMOS driver is to be boosted using bootstrapped driver circuits to improve its input voltage. A novel bootstrapped driver for eliminating the leakage from bootstrap node has been proposed.[1] Another CMOS driver has been proposed for improving the switching speed at lower supply voltages.[2] Direct bootstrapping technique used to improve the switching speed is better than the conventional bootstrapped driver circuit.[3] A bootstrapped driver has the ability to boost the signal during

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super-threshold region and to reduce the leakage current in subthreshold region.[4] A low-voltage bootstrapped CMOS driver which provides larger bootstrapped voltages for lower bootstrap capacitance has been proposed.[5] A single bootstrap capacitor is used to achieve switching for both the transitions and also results in lower area and power dissipation.[6] A bootstrapped driver circuit which produces an excellent voltage swing with lesser number of transistors has been proposed.[7] Another bootstrapped driver for driving large RC load, by eliminating the leakage path of the boosted nodes was designed.[8] The driver was able to improve the boosting efficiency and enhance the switching speed. Biasing is a technique used to vary the threshold voltage of the transistors. This technique is useful for faster switching.[9] Another driver circuit which offers better speed performance for larger loads was proposed.[10] The conventional bootstrapped CMOS driver circuit using two bootstrap capacitors to operate at low voltages is proposed.[11] Interconnects delay and power dissipation can also be reduced by repeater insertion. Different approaches in repeater insertion have been reviewed.[12] A repeater for high speed and low-power dissipation compared to the conventional repeater has been designed.[13] Modeling of mixed Carbon nanotube (CNT) bundles as interconnects was reviewed.[14] Performances of transmission gate buffers are better than CMOS buffers for mixed CNT interconnects at subthreshold region of operation.[15] Most of the works were concentrated on reducing the delay and power dissipation of interconnects at subthreshold operating region. Subthreshold operation is essential to achieve power efficient design for portable applications.[16] In this paper, we have designed a bootstrapped CMOS driver to reduce the delay and power dissipation by boosting the signal at the output node using body biasing technique. We have concentrated on reducing the rising delay and falling delay by body biasing technique. The rising delay is reduced by reducing the threshold voltage of transistor by proper body biasing and boosting the signal using bootstrap capacitor. The falling delay is reduced by boosting the signal strength of the transistor gate voltage using a capacitor. The proposed driver is more suitable for subthreshold operations.

This paper analyzes the delay and power dissipation of the proposed body-biased subthreshold bootstrapped CMOS driver and compares with conventional bootstrapped CMOS driver. In Sec. 2, we discuss the operation of conventional bootstrapped CMOS driver. In Sec. 3, the schematic design of the proposed bootstrapped CMOS driver is explained. Then in Sec. 4, we discuss the results and discussions and finally, Sec. 5 concludes the paper.

## 2. Conventional Bootstrapped CMOS Driver

The conventional bootstrapped CMOS driver is shown in Fig. 1. It consists of an inverter at the input. The driver transistors are made up of PMOS transistor MP1 and NMOS transistor MN1 to drive the output to high state and low state. The transistors MP2, MN3 and MN4 are used to pull-up the signal for the driver

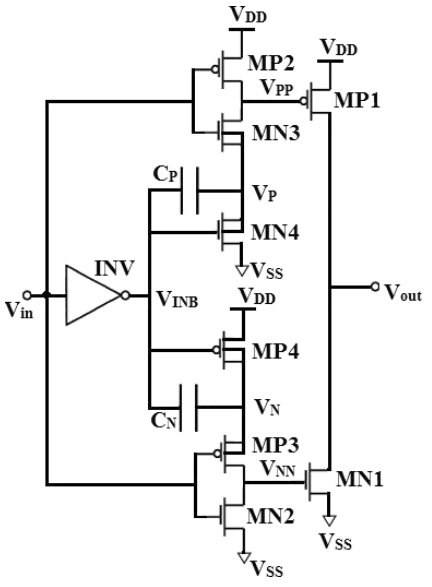



Fig. 1. Conventional bootstrapped CMOS driver.[11]

transistor MP1. The bootstrap capacitor $C_P$ is used to boost the signal at the node $V_P$. The transistors MN2, MP3 and MP4 are used to pull down the signal for driver transistor MN1. The bootstrap capacitor $C_N$ is used to boost the signal at node $V_N$. When $V_{\text{in}}$ is high, $V_{\text{INB}}$ becomes low, MN4 and MP2 will be OFF and MN3 is ON. MN3 makes the driver transistor MP1 to be turned ON. The bootstrap capacitor $C_P$ boosts the voltages at nodes $V_{\text{PP}}$ and $V_P$ below the ground, which turns on the transistor MP1 strongly to drive $V_{\text{out}}$ to high. When $V_{\text{in}}$ is low, $V_{\text{INB}}$ becomes high, MP4 and MN2 will be OFF and MP3 is ON. MP3 makes the driver transistor MN1 to be turned ON. The bootstrap capacitor $C_N$ boosts the voltage at nodes $V_{\text{NN}}$ and $V_N$ to be above $V_{\text{DD}}$ which allows MN1 to be turned on strongly to drive $V_{\text{out}}$ to low. The conventional bootstrapped CMOS driver is able to perform a positive and negative boosting of $2V_{\text{DD}}$ to $-V_{\text{DD}}$. The conventional bootstrapped CMOS driver has more number of series connected NMOS and PMOS transistors. The series connects MP2 with MN3 and MP3 with MN2, respectively. The faster switching of these series transistors have more chances of short circuit. The short circuit current leads to short circuit power dissipation. During the rising input transition, the node $V_P$ is boosted below the ground ($-V_{\text{DD}}$). But there is a large leakage path through the transistor MN4 which charges the node $V_P$. This will reduce the gate drive of MP1 and its boosting efficiency. Similar condition occurs in transistor MP4, which reduces the gate drive of MN1. Charge lost by these leakages leads to more power consumption.

## 3. Schematic Design of the Proposed Bootstrapped CMOS Driver

The proposed bootstrapped CMOS driver is shown in Fig. 2. It consists of an inverter (INV) at the input. The driver block consists of two transistors (MP4 and MN4) to drive the loads. The bootstrap block consists of six transistors (MN1, MN2, MP1, MP2, MP3 and MN3) and has two bootstrap capacitors $C_1$ and $C_2$. The pull-up circuit consists of MN1, MN2, MP3 and capacitor $C_1$. The pull-down circuit consists of MP1, MP2, MN3 and capacitor $C_2$. The proposed bootstrapped CMOS driver has been applied with the body biasing technique. The body of MN2 and MN1 are connected with $V_{in}$ and its complement, respectively. The change in the substrate voltage varies the threshold voltage of the device. When either MN1 or MN2 is ON, their threshold voltages drop and allows more ON current. This will boost the speed of the circuit. The body of MP1 and MP2 are connected with $V_{DD}$ and gnd, respectively, and their drain terminals to $V_{SS}$. During falling transition, the transistor MN1 is OFF and MN2 is ON, the voltage at node $V_P$ is charged to $V_{DD}$ as shown in Fig. 4. Since MP3 is OFF, the voltage at node $N_2$ is 0. Similarly, the transistor MP1 is OFF and MP2 is ON; the voltage at $V_{SS}$ applied at the terminal of MP2 is passed to node $V_N$, the node voltage at $V_N$ is $-V_{DD}$ as shown in Fig. 4. Since MN3 is ON, the voltage at node $N_2$ moves to $-V_{DD}$. During rising transition, the transistor MN1 is ON and MN2 is OFF, the capacitor $C_1$ is charged to high state $V_{DD}$. Due to that, the voltage at node $V_P$ is charged to $2V_{DD}$ as shown in Fig. 4. Since MP3 is also ON, the voltage at node $N_2$ is $2V_{DD}$. Similarly, the transistor MP1 is ON and MP2 is OFF, a $V_{SS}$ and $V_{DD}$ at the drain and body of transistor MP1 makes the voltage at node $V_N$ to 0 V. The bootstrap capacitor $C_2$ is charged. During falling transition, the transistor MP2 is ON, the capacitor $C_2$ starts discharging towards the gate of transistor MP2. This will boost the signal strength of MP2. For a rising and falling transition,

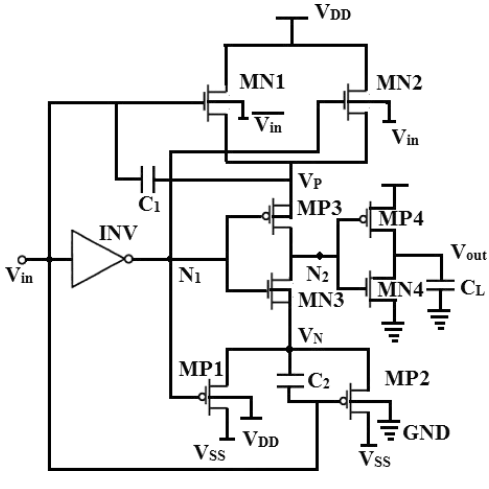
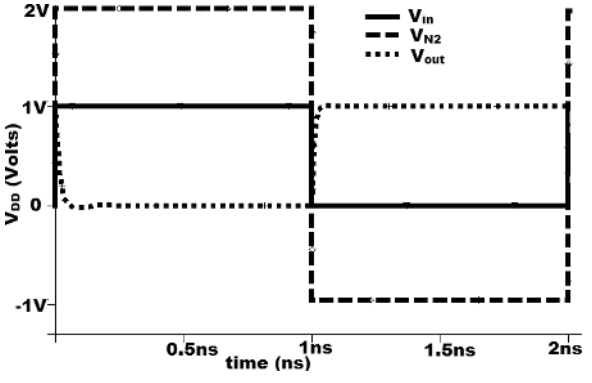


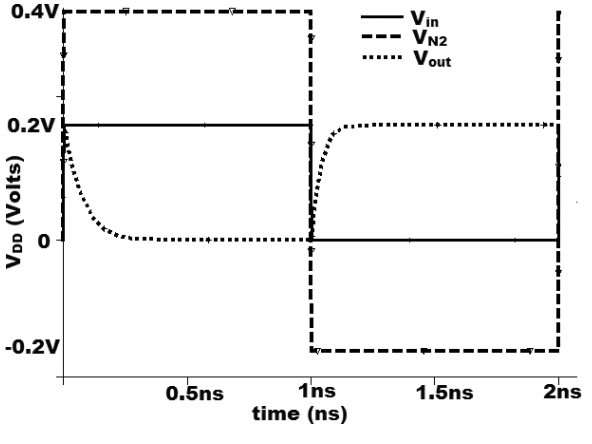

Fig. 2. Proposed body-biased subthreshold bootstrapped CMOS driver.

the $N_2$ is boosted to $2V_{DD}$ and $-V_{DD}$ to improve the capability of the driver. During switching, only transistor MN1 or MP2 is able to make a path to Node $N_2$ for pull-up or pull-down operation. So switching is due to only one of the parallel connected transistors, other transistor is used to hold the bootstrap state. Due to that reduced switching activity, power dissipation also reduced. Connecting the body terminals of MP1 to $V_{DD}$ is to have lower power dissipation. Connecting the drain and body of MP1 to $V_{SS}$ and $V_{DD}$, respectively is to make node $V_N$ to low during rising transition. Figures 3(a) and 3(b) shows the output of the proposed driver for a $V_{in}$ of 1 V and 0.2 V, respectively with the load capacitance of 1 fF. Figures 4(a) and 4(b) shows the voltages at nodes $V_P$ and $V_N$ during high and low transitions for a $V_{in}$ of 1 V and 0.2 V, respectively. Figure 4(c) shows the transient simulation of current drawn from



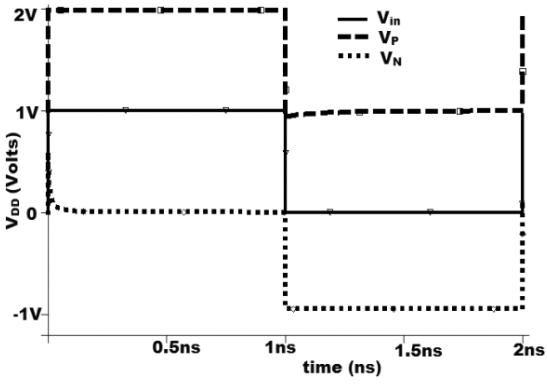



(a)

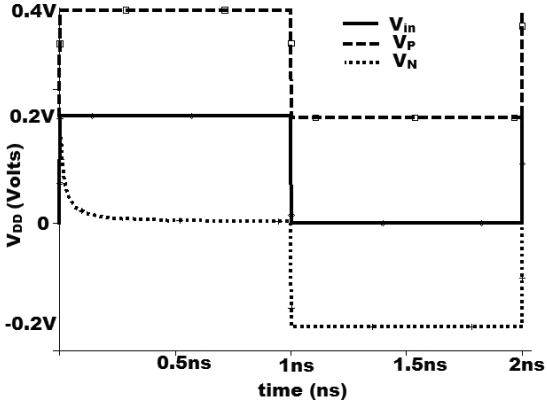



(b)

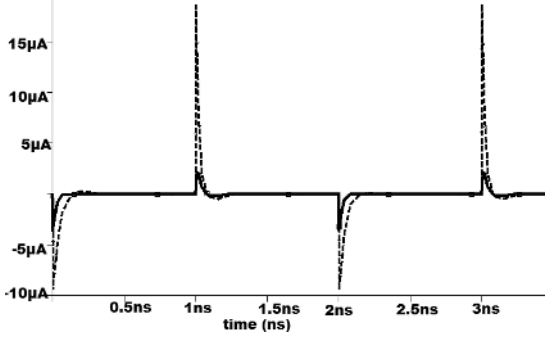
Fig. 3. (a) Output of the proposed body-biased subthreshold bootstrapped CMOS driver ($V_{in} = 1$ V). (b) Output of the proposed body-biased subthreshold bootstrapped CMOS driver ($V_{in} = 0.2$ V).




(a)




(b)




(c)

Fig. 4. (a) Node voltages of the proposed body-biased subthreshold bootstrapped CMOS driver ($V_{\text{in}} = 1\,\text{V}$). (b) Node voltages of the proposed body-biased subthreshold bootstrapped CMOS driver ($V_{\text{in}} = 0.2\,\text{V}$). (c) Transient simulation of current from power.

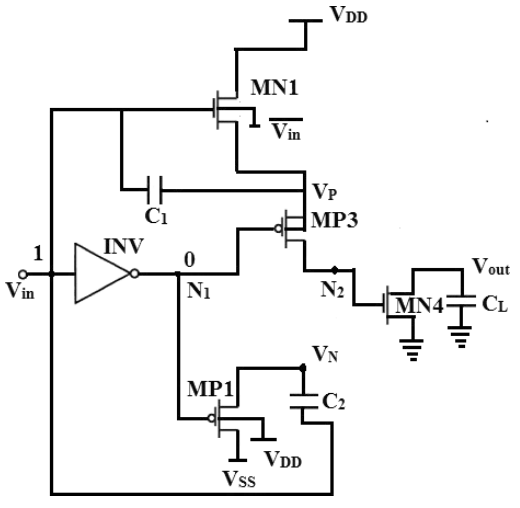



Fig. 5. Equivalent CMOS driver circuit when the input is high.

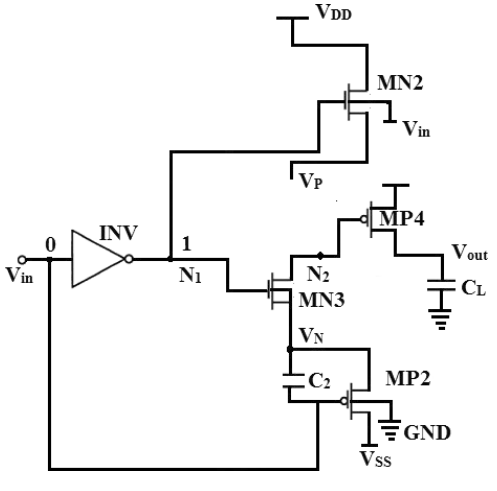



Fig. 6. Equivalent CMOS driver circuit when the input is low.

power for a $V_{\text{in}}$ of 0.6 V. Figures 5 and 6 show the equivalent circuit diagram of the proposed bootstrapped driver when the input is high and low, respectively. The equivalent circuit shows the transistors. The transistors in off state are removed.

## 4. Results and Discussions

This section gives the results of our proposed approach. The simulations for the proposed Bootstrapped CMOS driver were carried out by HSPICE tool. In the

simulations, predictive technology model[17] (PTM) of 22 nm was employed. The width-to-length ratio of NMOS and PMOS transistors are taken as 2:1. The width of PMOS is taken double the width of NMOS based on the mobility. The proposed bootstrapped CMOS driver was compared with the conventional bootstrapped CMOS driver and other bootstrapped drivers.

### 4.1. *Delay analysis*

#### 4.1.1. *Delay due to voltage scaling*

Rising delay and falling delay of the proposed Bootstrapped CMOS driver with conventional Bootstrapped CMOS driver and other bootstrapped drivers at 22 nm technology node are shown in Figs. 7 and 8, respectively.

The Proposed Body-biased bootstrapped CMOS driver has lower rising delay compared to the conventional bootstrapped CMOS driver and the other bootstrapped CMOS drivers. This is due to the higher ON current from the forward body biasing of the transistors during the pull-up state. The falling delay of the proposed CMOS driver is lower due to the proper body biasing of the transistors in pull-down state. At 22 nm technology node, rising delay and falling delay of the proposed driver is lower than the conventional CMOS bootstrapped driver[11] and other bootstrapped drivers. Figure 9 shows the propagation delay due to voltage scaling. The propagation delay increases for scaling of the voltage. The propagation delay is lower for the Proposed bootstrapped CMOS driver compared to the conventional bootstrapped CMOS driver and the other bootstrapped CMOS drivers. This is due to the voltage at $V_P$ (Fig. 4) during low transition. At high transition, the voltage at $V_P$ is added with the charges from the transistor MN1 and also boosting of charges from bootstrap capacitor $C_1$. The voltage at node $N_2$ is boosted to $2V_{DD}$. At high transition, the voltage at node $V_N$ becomes '0' due to the drain and body of MP1 that is

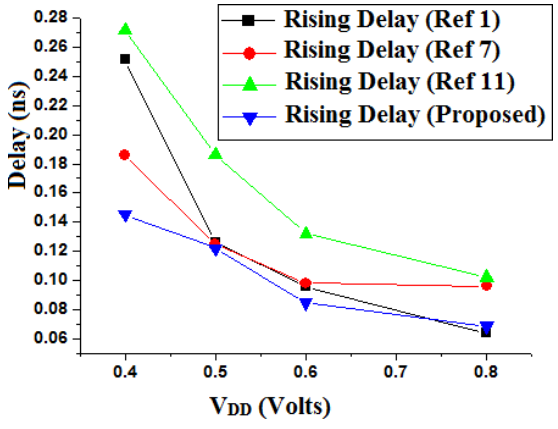



Fig. 7. Comparison of rising delay at 22 nm technology node due to voltage scaling.

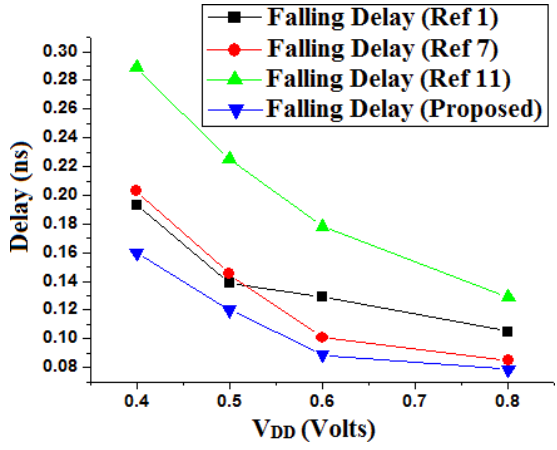



Fig. 8. Comparison of falling delay at 22 nm technology node due to voltage scaling.

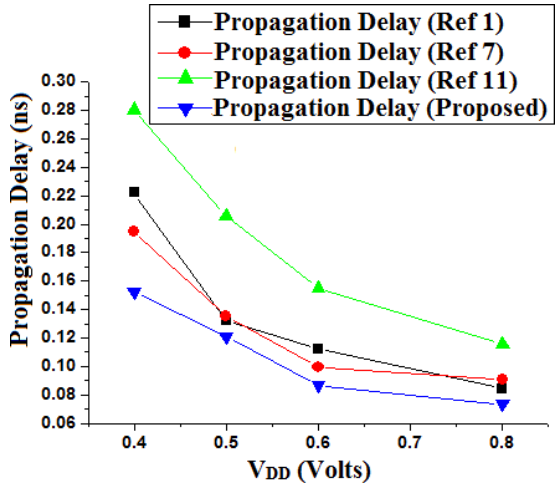



Fig. 9. Comparison of propagation delay due to voltage scaling.

connected to $V_{SS}$ and $V_{DD}$. The capacitor $C_2$ gets charged for high transition. At low transition, the transistor MP2 is ON, the capacitor $C_2$ starts discharging towards the gate of transistor MP2. The node voltage at $V_N$ equals to $-V_{DD}$ as shown in Fig. 4. At low voltage, the proposed bootstrapped CMOS driver will operate faster.

4.1.2. *Delay due to load scaling at super-threshold region*

The delay of an inverter is directly proportional to load and inversely proportional to supply voltage. Figures 10 and 11 show the rising delay and falling delay respectively

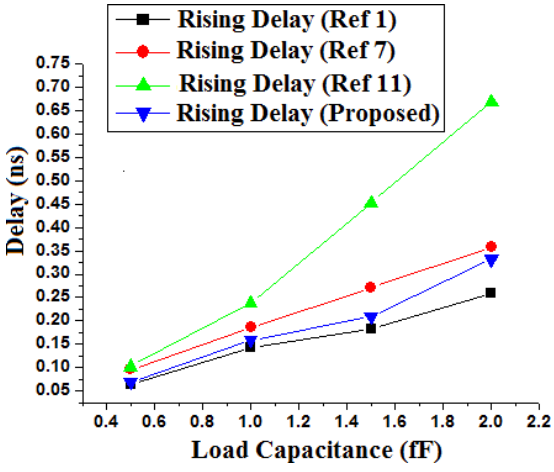



Fig. 10. Rising delay for super-threshold region due to load scaling.

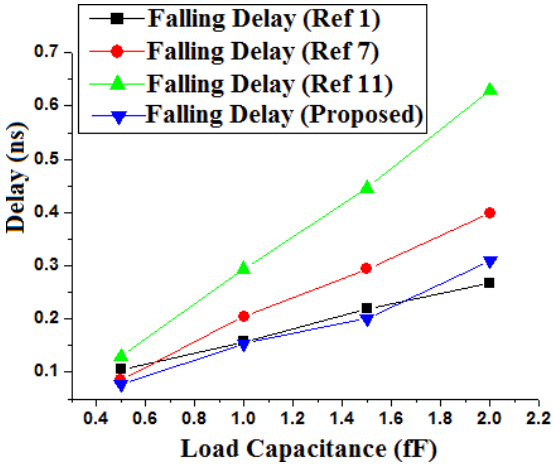



Fig. 11. Falling delay for super-threshold region due to load scaling.

at 22 nm technology node at ($V_{DD} = 0.8$ V) super-threshold region for the variation of load capacitance. As the load capacitance increases, the rising delay and the falling delay of the bootstrapped CMOS driver increases. The rising delay and falling delay for the proposed bootstrapped CMOS driver at super-threshold region is comparatively lower than the conventional bootstrapped CMOS driver and other bootstrapped CMOS drivers.

The rising delay is more compared to the CMOS driver for large RC load.[1] Figure 12 shows the comparison of the propagation delay of the proposed bootstrapped CMOS driver with conventional CMOS driver and other drivers.

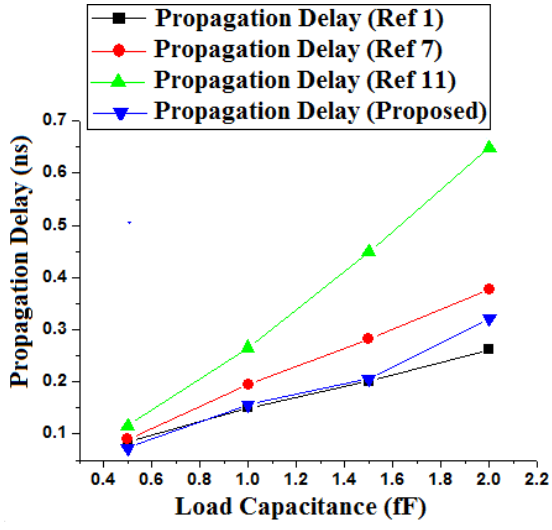



Fig. 12. Propagation delay for super-threshold region due to load scaling.

The performance of proposed bootstrapped driver is better than the conventional driver in terms of delay.

#### 4.1.3. *Delay due to load scaling at subthreshold region*

Figures 13 and 14 shows the rising delay and falling delay, respectively at 22 nm technology node at ($V_{DD} = 0.5$ V) subthreshold region for the variation of load capacitance.

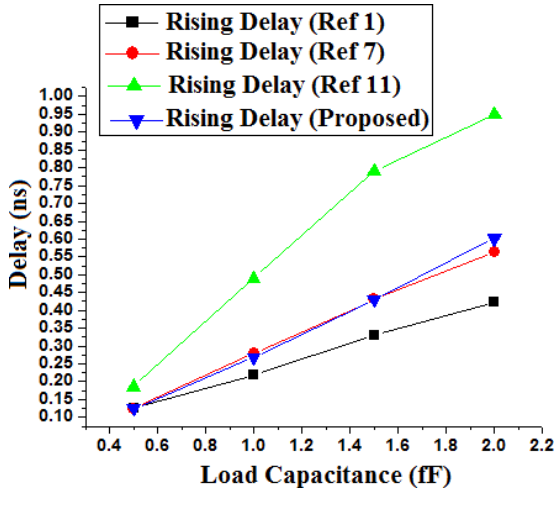



Fig. 13. Rising delay for subthreshold region due to load scaling.

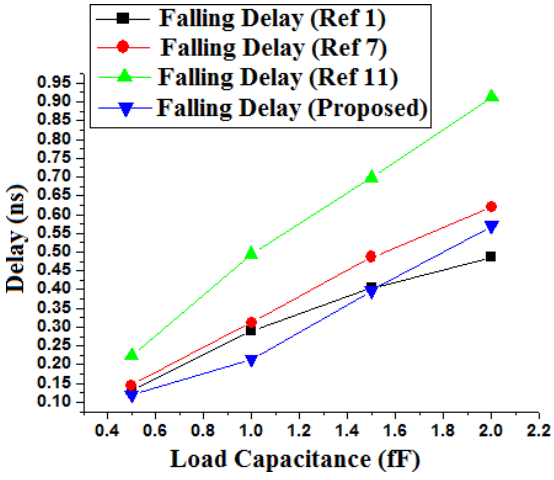



Fig. 14. Falling delay for subthreshold region due to load scaling.

Figure 15 shows the propagation delay for subthreshold region for load scaling. The rising delay and falling delay for the proposed bootstrapped CMOS driver at subthreshold region is also lower than the conventional bootstrapped CMOS driver and more than the enhanced bootstrapped driver for RC load[1] for higher loading conditions. The propagation delay is lower for the proposed bootstrapped driver compared to the conventional bootstrapped driver for higher load capacitance. The CMOS driver should have the capability to drive higher loading conditions at lower

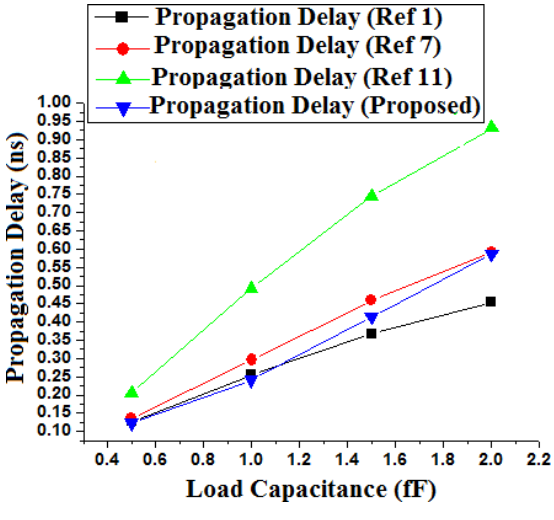



Fig. 15. Propagation delay for subthreshold region due to load scaling.

operating conditions. The proposed bootstrapped driver is more suitable to drive large loads with high speed at subthreshold region of operation.

### 4.2. *Power dissipation analysis*

Reducing the supply voltage and load reduces the power dissipation. Low-power operation is essential for battery operated devices. Here, the power dissipation is analyzed by scaling the voltages and load at 22 nm technology node. Figure 16 shows the power dissipation due to scaling of voltages for low-power operation. The proposed bootstrapped CMOS driver has lower power dissipation compared to the other drivers. Figures 17 and 18 shows the power dissipation at super-threshold region and subthreshold region of operation due to load scaling.

The power dissipation of proposed bootstrapped CMOS driver is lower for higher loading conditions at super-threshold region of operation. At subthreshold region of operation, the reduction of power dissipation is more for any loading conditions for the proposed bootstrapped CMOS driver. The results show that the proposed driver is more suitable for low-power applications for driving larger loads. The low-power dissipation is due to the absence of direct path to the node $N_2$ from pull-up circuit to pull-down circuit. During low transition, the pull-up circuit and pull-down circuit are completely isolated. This reduces the short circuit when the transistor is switched. Reverse biasing of transistor at pull-down path during a high-input transition also reduces the power dissipation.

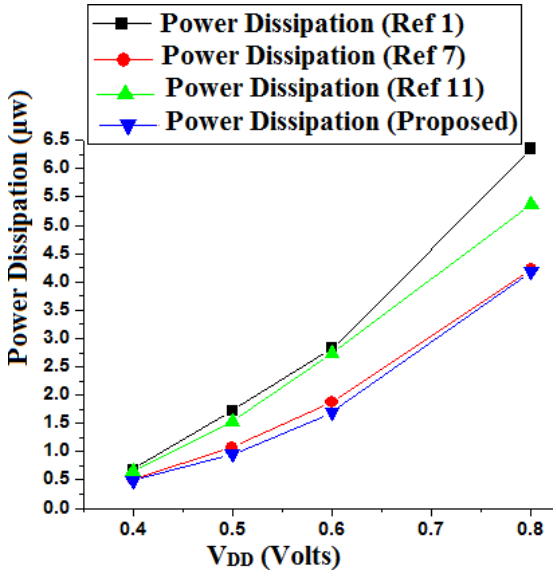



Fig. 16. Power dissipation due to voltage scaling.

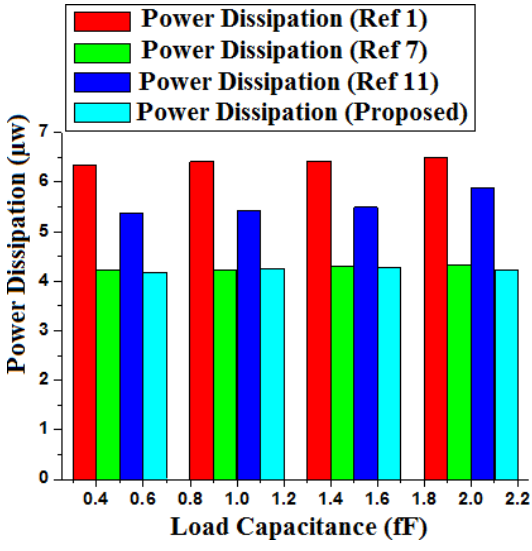



Fig. 17. Power dissipation at super-threshold region due to load scaling.

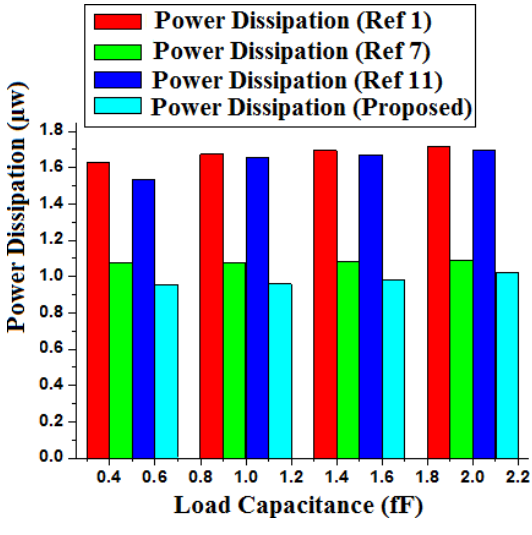



Fig. 18. Power dissipation at subthreshold region due to load scaling.

### 4.3. *Comparison of delay and power dissipation of the proposed bootstrapped CMOS driver*

The proposed body-biased bootstrapped CMOS driver was validated and compared with conventional bootstrapped driver[11] and other bootstrapped drivers using PTM[17] at 22 nm technology node.

Table 1. Comparison of proposed bootstrapped CMOS driver with other bootstrapped CMOS drivers.

| Parameter | Ref. 1 | Ref. 7 | Ref. 11 | Proposed |
|---|---|---|---|---|
| Technology node | 22 nm | 22 nm | 22 nm | 22 nm |
| Delay (ns) | 0.455 | 0.591 | 0.932 | 0.586 |
| Power dissipation ($\mu$W) | 1.712 | 1.088 | 1.695 | 1.02 |
| Power delay product (fJ) | 0.778 | 0.643 | 1.579 | 0.597 |

Table 1 shows the comparison of performance of bootstrapped CMOS drivers at subthreshold region of operation ($V_{DD} = 0.5$). The results from Table 1 show that the power delay product of the proposed body biased bootstrapped CMOS driver is lower than the other bootstrapped CMOS drivers at subthreshold region of operation for higher loading conditions. The power-delay product shows that the proposed body-biased bootstrapped CMOS driver is more suitable to drive high loads at subthreshold region.



## 5. Conclusion

A body-biased bootstrapped CMOS driver which operates better at subthreshold region has been proposed. The proposed bootstrapped CMOS driver has 37% reduction in delay and 39% reduction in power dissipation compared to the conventional bootstrapped CMOS driver. Body bias technique is applied to improve the switching speed. The power delay product is less compared to the conventional bootstrapped CMOS driver and other bootstrapped drivers. The proposed driver is also more suitable for driving larger loads at subthreshold region. The proposed driver can be used to drive interconnects with higher fan-out.

## References

1. H.-J. Kim, J. Kim and B. S. Kong, Enhanced bootstrapped CMOS driver for large RC load and ultra-low voltage VLSI, *IEICE Electron. Exp.* **9** (2012) 1208–1213.
2. B. S. Kong and Y.-H. Jun, Power-efficient low voltage bootstrapped CMOS latched driver, *Electron. Lett.* **35** (1999) 2113–2115.
3. P. C. Chen and J. B. Kuo, Sub-1V CMOS large capacitive-load driver circuit using direct bootstrap technique for low-voltage CMOS VLSI, *Electron. Lett.* **38** (2002) 265–266.
4. Y. Ho, C. Chang and C. Su, Design of a sub threshold-supply bootstrapped CMOS inverter based on an active leakage-current reduction technique, *IEEE Trans. Circuits Syst. II* **59** (2012) 55–59.
5. J. W. Kim and B. S. Kong, Low-voltage bootstrapped CMOS drivers with efficient conditional bootstrapping, *IEEE Trans. Circuits Syst. II* **55** (2008) 556–560.
6. J. C. Garcia, J. A. Montiel-Nelson and S. Nooshabadi, A single-capacitor bootstrapped power-efficient CMOS driver, *IEEE Trans. Circuits Syst. II* **53** (2006) 877–881.
7. V. K. Sharma, Design of low leakage PVT variations aware CMOS bootstrapped driver circuit, *J. Circuits Syst. Comput.* **26** (2017) 1750137-1–1750137-19.

8. C.-Y. Lu and C.-T. Chuang, Energy efficient bootstrapped CMOS large RC-load driver circuit for ultra low-voltage VLSI, *J. Low Power Electron. Appl.* **2** (2012) 282–300.
9. P. Corsonello, M. Lanuzza and S. Perri, Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates, *Int. J. Circuit Theory Appl.* **42** (2012) 65–70.
10. L. C. Fatt, Y. K. Seng and S. S. Rofail, Sub-I V bootstrapped CMOS driver for giga scale-integration era, *Electron. Lett.* **35** (1999) 392–394.
11. J. C. Garcia, J. A. Montiel-Nelson and S. Nooshabadi, A 1.5-V full-swing bootstrapped CMOS large capacitive-load driver Circuit suitable for low-voltage CMOS VLSI, *IEEE J. Solid-State. Circuits.* **32** (1997) 119–121.
12. A. Karthikeyan and P. S. Mallick, Optimization techniques for CNT based VLSI interconnects-A review, *J. Circuits Syst. Comput.* **3** (2017) 1730002-1–1730002-15.
13. A. Karthikeyan and P. S. Mallick, High-speed and low-power repeater for VLSI interconnects, *J. Semicond.* **38** (2017) 105006-1–105006-5.
14. P. U. Sathyakam and P. S. Mallick, Towards realisation of mixed carbon nanotube bundles as VLSI interconnects: A review, *Nano Commun. Netw.* **3** (2012) 175–182.
15. A. Karthikeyan and P. S. Mallick, Transmission gate as buffer for carbon-nanotube based VLSI interconnects, *IETE J. Res.* (2017), doi: 10.1080/03772063.2017.1351316.
16. S. D. Pable, Z. H. Mohd. Hasan, S. A. Abbasi and A. R. M. Alamoud, Interconnect optimization to enhance the performance of sub threshold circuits, *Microelectron. J.* **44** (2013) 454–461.
17. ptm.asu.edu. (2008). Predictive Technology Model (PTM). [online] Available at: http://ptm.asu.edu.