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Comparison of Fuzzy and ANFIS Controllers for Asymmetrical 31-Level Cascaded Inverter with Super Imposed Carrier PWM Technique

KOLA MURALIKUMAR[1], P. PONNAMBALAM[2]
[1]Vellore Institute of Technology, Vellore, Tamil Nadu, India (e-mail: kolamuralikumar@gmail.com)
[2]Vellore Institute of Technology, Vellore, Tamil Nadu, India (e-mail: p.ponnambalam@gmail.com)
Corresponding author: P. Ponnambalam (e-mail: p.ponnambalam@gmail.com).

ABSTRACT The modified topology for an asymmetrical 31-level cascaded inverter is analyzed with less number of DC voltage sources, power diodes, and power electronic knobs. The Super Imposed Carrier Pulse Width Modulation (SIC-PWM) is proposed for a 31-level asymmetrical modified cascaded inverter topology to reduce the Total Harmonic Distortions (THD). The Fuzzy logic controller (FLC) and Adaptive Neuro-Fuzzy Inference System (ANFIS) are suggested for a 31-level asymmetrical modified cascaded inverter topology to control the root mean square (RMS) voltage. These controllers help in maintaining the output voltage constant even when there is a change in input voltage to the inverter. This study aims to compare Fuzzy logic and ANFIS controllers by applying them to the 31-level cascaded inverter. Using both the controllers the inverter is controlled and its performance is compared using a step response tool in MATLAB. The study of the proposed modified 31-level Asymmetrical cascaded inverter is carried out to evaluate the THD without and with Fuzzy logic and ANFIS controller. Using the step response tool, Settling Time, Overshoot, RMS Voltage values, Peak Time, Peak value, and Rise Time were evaluated and compared for Fuzzy and ANFIS controlled 31-level asymmetrical cascaded inverter. The THD value for without a controller is 4.97%, with the fuzzy logic controller is 4.15% and with ANFIS controller is 3.77%. In both MatLab and real-time simulation, total harmonic distortion (THD) is observed to be the almost same and is lower than 5% which is under IEEE standards. The performance of Fuzzy and ANFIS controlled 31-level asymmetrical cascaded inverter is evaluated and compared with the use of MATLAB/Simulink and the same is done with Real-Time simulation using OPAL-RT 5700.

INDEX TERMS Asymmetrical Cascaded Inverter, Super Imposed Carrier PWM technique, Total Harmonic Distortion, Adaptive Neuro-Fuzzy Inference System(ANFIS), Fuzzy logic controller(FLC).

NOMENCLATURE

MLI	Multilevel Inverter
THD	Total Harmonic Distortion
FLC	Fuzzy Logic Controller
RMS	Root Mean Square
ANFIS	Adaptive Neuro-Fuzzy Inference System
SCI-PWM	Super Imposed Pulse Width Modulation
PD-PWM	Phase shift- Pulse Width Modulation
SHEPWM	Selective Harmonic elimination
NPC	Neutral Point-Clamped
FC	Flying Capacitor
IGBT	Insulated Gate Bipolar Transistor
FBC	Full Bridge Converter
NLC	Nearest Level Control
FFT	Fast Fourier Transformation
HIL	Hardware in Loop
RT	Real-Time Simulation
Vdc	DC Voltage source
f_s	Switching frequency
V_0	Output Voltage
V_{n_rms}	n^{th} Harmonic for RMS voltage
V_{fund_rms}	Fundamental frequency for RMS voltage
e	error
ce	change in error

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I. INTRODUCTION

A multi-level inverter is an important role in medium voltage and high-power applications. The idea behind multilevel inverters is that having more than two levels in the output offer additional advantages such as increased output voltage range [1]. This multi-level inverter can synthesize higher DC voltages by using a series-connected semiconductor device. Various multilevel inverter topologies were introduced in 1980, including diode-clamped technology and neutral point-clamped (NPC) [2]. In the 1990s, new topologies such as NPC, cascaded H-bridge, and flying-capacitor(FC) multi-level inverter was introduced [3].

The conventional multi-level inverter topologies such as the FC inverter and NPC uses a single common source, whereas multiple isolated DC sources are used in cascaded inverter topology [4]. In diode clamp technology, one DC source is used, but the clamped diode requirement is exceptionally high. In FC topology, capacitors are placed as an alternative of diode-clamping [5]. Consequently, the total size of the inverter increases in both the cases [4]. The cascaded multi-level inverter topology is chosen for its modular environment, and being flexible to add additional modules [6]. Using the same circuit components the no. of voltage levels could be increased by appropriately selecting the DC voltage sources [1]. If all DC sources' value is equal, then it is called symmetrical. If the DC sources are unequal then it is referred to as asymmetrical cascaded inverter topology [7].

The THD is comparatively more for a traditional two-level voltage converter due to the issues in voltages, and it decreases the life-cycle of the electrical installation and automation [8]. Utilizing a filtering circuit could solve this issue but this raises the complexity of the circuit and the overall cost. As compared with other multi-level inverters, the proposed cascaded inverter will be able to alleviate the complex issues created by the filtering circuit hence this cascaded inverter generates an improved output voltage with less THD thus reducing the need for heavy filters [9]. In high power applications, like variable frequency drives, electric vehicles, HVDC, FACT, active power filters, and hybridization of renewable energy sources, multilevel inverter played an important role. It is mainly effective for medium voltage motor drive system-based applications, due to their less switch voltage stress. The suggested multilevel inverters are suitable for renewable energy and industrial applications.

Several topologies for cascaded multi-level inverters with several control methods have been proposed recently [10]. The different circuit configurations of symmetric cascaded multi-level inverters are described in [11]. In [12] the presented topology is asymmetric inverter type, in which the number of bidirectional power switches constraint is more resulting in more number of IGBTs, which raises the cost of the inverter. The [13] proposed a novel circuit topology with fewer switches and different algorithms, but this circuit has a larger no of voltage sources, which is a disadvantage. These complexities can be reduced by making the best use of semiconductor devices. Uneven dc voltage magnitude of sources can be used to minimize switch count [11]. [14], [15] presented several inverters with higher voltage-levels to decreases the number of power switches. A full-bridge converter (FBC) converts the DC phase output of these inverters to the AC step. In [16], a three-phase with three single phases system is defined, as well as several novel topologies for reducing the number of components in both single-phase and three-phase systems.

The appropriate switching frequency and no of levels for these inverters were investigated in [17]. To minimize harmonics, this inverter is powered by a level-shifted PD-PWM technique, as well as an LC filter. [18] proposed a new single-phase cascaded topology in which the pulses for the switches are produced using a SHEPWM. A basic unit with 11 levels is given, as well as instructions for cascading two basic units to attain the 71 levels at the output. The [19] proposes a 31-level asymmetric cascaded multilevel inverter For renewable energy applications. The output of multi-level inverter under dynamic load disturbances and steady-state transient was investigated by these authors. The [20] suggests using the nearest level control PD-PWM method and PWM (NLC-PWM) to control eleven unidirectional switches and a single switched capacitor unit to synthesize a 9-level output voltage waveform. The [21] suggests a three-source 15-level topology with 4 dc voltage sources and 12 switches for a total of 25 levels at the output. These researchers tested various loading conditions as well as dynamic variations in load and modulation indexes.

In [22], the authors proposed the single-source-driven quadruple boost multilevel inverter topology (QB-MLI) with lesser order of resources over the other switched capacitor. This controller is used to balancing the two capacitors voltage with the associated control logic. The [23] focuses on a new family of step-up multilevel inverter topologies with switched capacitor integration with dual input voltage sources using passive elements. In [24], proposed the 5-Level boost inverter topology, It consists of eight switches, one SC unit, and one input voltage source. To maintain the capacitor voltage, a conventional carrier-based sinusoidal modulation technique is used.

In [25], a high boosting ratio inverter is introduced in this article based on using the switched capacitor multilevel inverter (SCMLI). A fuzzy logic optimized reduced sensor is proposed to achieve the MPPT control for the fuel cell. The proposed inverter stage is based on switched capacitor cells with self-balanced capacitor voltages. The [26] proposed multiple-voltage-vector model predictive control (MPC) algorithm with reduced complexity and fixed switching frequency for T-type three-phase three-level inverters which are compared in terms of the steady-state behavior, dynamic response, and neutral point voltage balancing performance. The [27] proposed an adaptive neuro-fuzzy model (ANFIS) to the multilevel inverter (MLI) for a grid-connected photovoltaic (PV) system. ANFIS gives the control voltage according to the different inputs. The ANN-based SHEPWM was designed to obtain inverter output voltage which has

a bipolar waveform with quarter-wave symmetry in [28]. Different harmonic orders are analyzed for load current and ripple of the dc-link voltage.

From the above-specified literature review, it can be found that the modified cascaded inverter topology for 31-level asymmetrical inverter using SICPWM techniques without the controller and with fuzzy and ANFIS controller are found to be lacking in the literature. This topology can reduce the voltage stress on each power device due to the utilization of multiple levels on the DC bus. It is important when a high DC side voltage is imposed by an application. Even at low switching frequencies, smaller distortion in the multilevel inverter AC side waveform can be achieved (with stepped modulation technique). Hence, in this paper, the proposed super-imposed PWM method can be used to reduce the system complexity and reduce the total harmonic distortion. On the other hand, to control the RMS output voltage of the system, fuzzy logic and ANFIS controller are used. These control techniques are flexible and allow modification in the rules. Even inaccurate, distorted, and error input information is also accepted by the system.

The major contribution of these paper is summarized here: 1. The paper proposes a super-imposed carrier PWM technique for 31-level asymmetrical modified cascaded inverter topology to reduce the Total Harmonic Distortions (THD). 2. The Fuzzy logic controller (FLC) and Adaptive Neuro-Fuzzy Inference System (ANFIS) is suggested for a 31-level asymmetrical modified cascaded inverter topology to control the root mean square (RMS) voltage. These controllers help to control and maintaining the output RMS voltage constant even when there is a change in input voltage to the inverter. even when R-Load varies, the RMS output voltage remains constant. 3. This study aims to compare Fuzzy logic and ANFIS controllers by applying them to the 31-level cascaded inverter to find the step response values (Time, Overshoot, RMS Voltage values, Peak Time, Peak value, and Rise Time).

The modified cascaded inverter topology for 31-level Asymmetrical configuration with modes of operation and switching pattern is detailed in section 2. Section 3 proposes the super-imposed carrier PWM technique. The Fuzzy logic controller and ANFIS controller integrated into the multilevel inverter are discussed in section 4. Section 5 represents the results and discussions. The conclusion is described in section 6.

II. MODIFIED-CASCADED INVERTER TOPOLOGY

The fundamental circuit diagram of the symmetrical and asymmetrical cascaded inverter topology of the system is illustrated in Fig. 1. In this configuration, H-bridge and modular structure are integrated. The no. of DC source voltage as well as switches vary appropriately to obtain the multilevel outputs in modular design, whereas the H-Bridge remains identical. By enhancing the DC source voltage and switches in the modular design, the output voltage levels can be raised. The Asymmetrical Cascaded Inverter for a 31-level is analyzed. In this configuration, the Super Imposed Carrier PWM method is used to generate triggering pulses for the inverter circuit. This PWM method provides self-balancing for the multi-level inverter. The switching frequency is $f_s = 2kHz$.

The 31-level asymmetric cascaded multilevel inverter is suggested in the present study. Several advantages have resulted from the reduced number of circuit components in the suggested topology. These advantages include few DC sources with low THD, a fewer number of switches, and the generation of the higher number of output voltage levels. The suggested multilevel inverters are suitable for renewable energy and industrial applications.

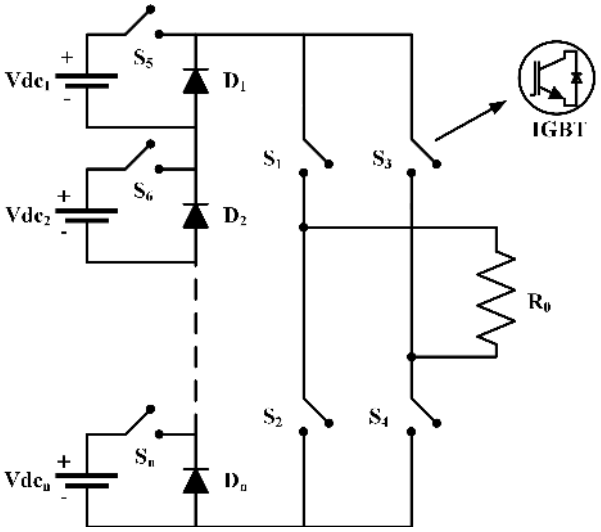

FIGURE 1. The fundamental circuit diagram of symmetrical and asymmetrical cascaded inverter.

A. 31-LEVEL ASYMMETRICAL CASCADED MULTI-LEVEL INVERTER

As demonstrated in Fig.1, a simple block of modified cascaded inverter topology comprises of the number of DC source voltage [29]. If the amplitude of the DC source voltage is not equal, then the inverter is referred to as the Asymmetrical cascaded inverter [11]. It can easily increase the output voltage levels by enhancing the dc voltage levels and the number of switches in modular design [30]. It can easily increase the output voltage levels by boosting the dc voltage levels and the number of switches in modular construction [31]. The DC input voltage sources were chosen based on a linear series with a factor of two or three. The modified topology is utilized for producing more voltage levels, without increasing the quantity of DC voltage sources and switches.

The dc input voltage source can be stated by 'n 'and Vdc as $2^{(\mathrm{n}-1)}\mathrm{Vdc}$.

Since 'n'DC sources are used in Fig. 1, the magnitude value of DC sources, output voltage levels, and maximum voltage can be determined using the equations below.

In the symmetric configuration, the magnitude value of DC sources is as follows.

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$$Vdc_1 = Vdc, Vdc_2 = 2Vdc, Vdc_3 = 4Vdc \\ \ldots Vdc_n = 2^{(n-1)}Vdc \quad (1)$$

The overall voltage magnitude can be calculated as follows:

$$V_{0,\max} = (2^n - 1)\, V_{dc} \quad (2)$$

Another technique for determining the maximum reference voltage based on the DC source used is

$$V_{0,\max} = (N - 1)V_{dc} \quad (3)$$

Where,

$$N = (2^n) \quad (4)$$

The following formula is used to measure the output voltage-level of an asymmetric configuration. The output voltage-level number is

$$L = \left(2^{n+1} - 1\right) \quad (5)$$

Equation (5) verified that the proposed topology of the asymmetric condition can achieve a greater number of voltage levels.

where, n=4 is the number of DC voltage sources on each leg, then the number of switches, sources shall be calculated using equation (5) respectively:

$$L = \left(2^{4+1} - 1\right) = 31 levels \quad (6)$$

The 31-level Asymmetrical cascaded inverter is as shown in Fig.2. The Number of switches and output levels related to level modules is tabulated in Table 1.

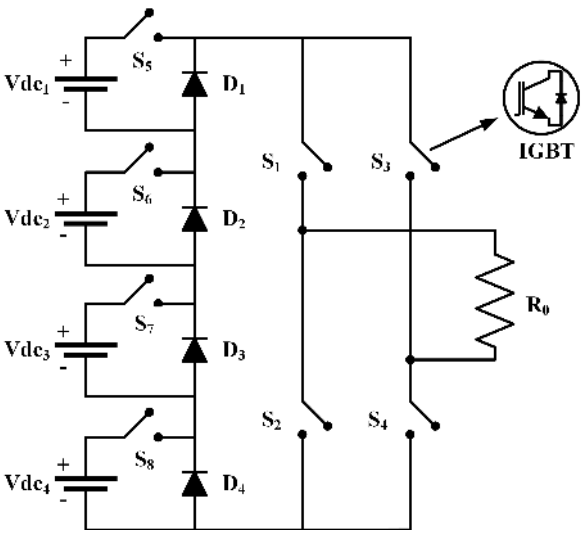

FIGURE 2. Thirty-one-level Asymmetrical cascaded inverter.

TABLE 1. Number of switches and output levels related to level modules

Cascaded level modules	Dc Sources	No. of Switches	No. of Levels
Level Module 1	1Vdc	5	3
Level Module 2	2Vdc	6	7
Level Module 3	4Vdc	7	15
Level Module 4	8Vdc	8	31
Level Module 5	16Vdc	9	63
Level Module 6	32Vdc	10	127
.	.	.	.
Level Module n	$2^{(n-1)}Vdc$	$n+4$	$2^{(n+1)}-1$

B. MODES OF OPERATIONS

From the Fig. 1, four input source voltage Vdc_1, Vdc_2, Vdc_3 and vdc_4 is considered for the 31-level cascaded inverter. For each source, the input voltage is $Vdc_1 = V; Vdc_2 = 2V; Vdc_3 = 4V; Vdc_4 = 8V$. The arrangement of the asymmetrical inverter has a +ve group and a -ve group. The +ve group is taking care of delivering positive signal waves beyond load capacity. The amount of gain voltage Vdc rises with the rise in the number of switches. The Switching pattern for the 31-level cascaded inverter is tabulated in Table 2. The modes of operation for 31-level Asymmetrical topology for all positive levels including zero levels are as shown in Fig. 3. The operating modes of the 31-level cascaded inverter are tabulated in Table 3.

III. SUPER IMPOSED CARRIER PULSE WIDTH MODULATION (SIC-PWM)

The switching pattern is particularly important for any multilevel inverter to obtain an efficient output. The harmonic components of the topology are decided by the modulation index of the PWM Scheme, so the harmonics of the inverters are determined by the switching pattern. Super Imposed Carrier PWM technique is used in this topology.

The block diagram of executed Super Imposed Carrier PWM is visualized in Fig. 4. The carrier wave is super imposed with a reference sinewave signal and compared by using a comparator, then the aggregated signal is generated. The aggregated signal is also called the super-imposed PWM technique. The DC signals are given to the generated super-imposed sinusoidal signal for generating the desired number of levels. From the desired voltage levels, the output voltage is obtained. In this, the sinusoidal waveform is superimposed with a carrier triangular wave. Fig 5(a) shows the sinusoidal waveform and Fig 5(b) shows the carrier wave signal. The amplitude of the carrier wave is 10% of the sinusoidal wave. The superimposed waveform is compared with 30 different signals. At every stage of comparison, the superimposed signal and dc signal generates the pulses. By adding all stage pulses at every comparison point, the comprehensive signal

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TABLE 2. Switching pattern for 31-level cascaded inverter

Switching Levels	Switches								Voltage Sources				
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Vdc_1	Vdc_2	Vdc_3	Vdc_4	Output
Level-1	1	0	0	1	1	1	1	1	1	1	1	1	+15Vdc
Level-2	1	0	0	1	0	1	1	1	0	1	1	1	+14Vdc
Level-3	1	0	0	1	1	0	1	1	1	0	1	1	+13Vdc
Level-4	1	0	0	1	0	0	1	1	0	0	1	1	+12Vdc
Level-5	1	0	0	1	1	1	0	1	1	1	0	1	+11Vdc
Level-6	1	0	0	1	0	1	0	1	0	1	0	1	+10Vdc
Level-7	1	0	0	1	1	0	0	1	1	0	0	1	+9Vdc
Level-8	1	0	0	1	0	0	0	1	0	0	0	1	+8Vdc
Level-9	1	0	0	1	1	1	1	0	1	1	1	0	+7Vdc
Level-10	1	0	0	1	0	1	1	0	0	1	1	0	+6Vdc
Level-11	1	0	0	1	1	0	1	0	1	0	1	0	+5Vdc
Level-12	1	0	0	1	0	0	1	0	0	0	1	0	+4Vdc
Level-13	1	0	0	1	1	1	0	0	1	1	0	0	+3Vdc
Level-14	1	0	0	1	0	1	0	0	0	1	0	0	+2Vdc
Level-15	1	0	0	1	1	0	0	0	1	0	0	0	+Vdc
Level-16	1	1	0	0	0	0	0	0	0	0	0	0	0
Level-17	0	1	1	0	1	0	0	0	1	0	0	0	-Vdc
Level-18	0	1	1	0	0	1	0	0	0	1	0	0	-2Vdc
Level-19	0	1	1	0	1	1	0	0	1	1	0	0	-3Vdc
Level-20	0	1	1	0	0	0	1	0	0	0	1	0	-4Vdc
Level-21	0	1	1	0	1	0	1	0	1	0	1	0	-5Vdc
Level-22	0	1	1	0	0	1	1	0	0	1	1	0	-6Vdc
Level-23	0	1	1	0	1	1	1	0	1	1	1	0	-7Vdc
Level-24	0	1	1	0	0	0	0	1	0	0	0	1	-8Vdc
Level-25	0	1	1	0	1	0	0	1	1	0	0	1	-9Vdc
Level-26	0	1	1	0	0	1	0	1	0	1	0	1	-10Vdc
Level-27	0	1	1	0	1	1	0	1	1	1	0	1	-11Vdc
Level-28	0	1	1	0	0	0	1	1	0	0	1	1	-12Vdc
Level-29	0	1	1	0	1	0	1	1	1	0	1	1	-13Vdc
Level-30	0	1	1	0	0	1	1	1	0	1	1	1	-14Vdc
Level-31	0	1	1	0	1	1	1	1	1	1	1	1	-15Vdc

will produce which is the same as the output waveform of the multilevel inverter. Hence it can be easily predicting the inverter output waveform before conduction. From the comparison of carrier superimposed sinusoidal signal with various DC signals, each dc signal is given to the super-imposed signal to generate the required number of voltage levels. Fig. 6 shows a comparison of carrier superimposed sinusoidal signal with various DC signals. Fig. 7. shows the comprehensive signal. From the analysis of the super-imposed carrier PWM technique, the expected output voltage waveform of 31-level is as shown in Fig.8. which shows clearly how to generate switching pulses for the switches.

The no. of output level decides the necessary number of dc bias levels. N-1 dc bias signals are a necessity for an N-level output. The phase displacement technology is used for the PWM technique. Consider an N-level multilevel inverter, where N is the odd number since the zero levels are typical. In a multi-level inverter, the significant number of positive levels is given as

$$N_{pos} = \frac{N_{\text{level}} - 1}{2} \tag{7}$$

In an N-level multilevel inverter, the number of negative levels is identical to the number of positive levels which is given as

$$N_{neg} = \frac{N_{\text{level}} - 1}{2} \tag{8}$$

$$N_{pos} = N_{neg} = \frac{N_{\text{level}} - 1}{2} \tag{9}$$

Mathematical methods

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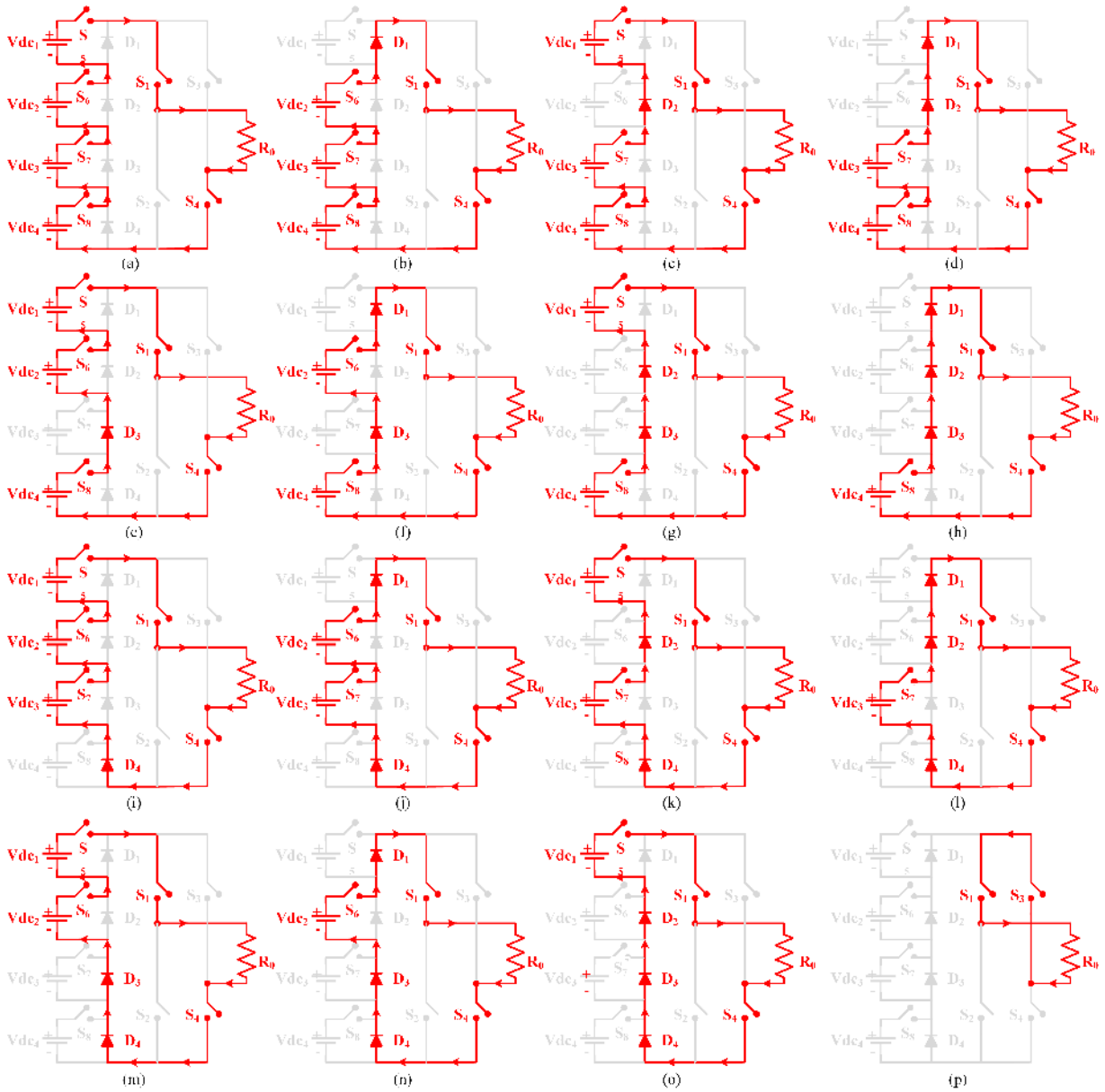

FIGURE 3. Positive modes of operation including zero level for 31-level asymmetrical cascaded inverter.

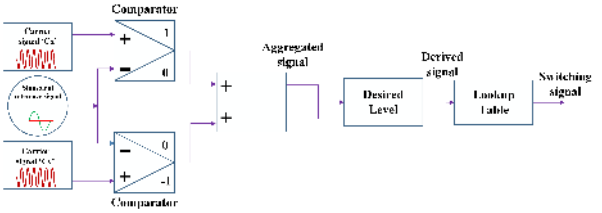

FIGURE 4. Block diagram of the proposed control scheme.

The cascaded MLI topology with a desirable amplitude and enhanced harmonic spectrum is provided with programmed PWM technique to determine the required switching angles for obtaining the output [32]. In any PWM technique, the $n+1$ equation is required to monitor the output voltage and to eradicate the nth harmonics [33], by Selective Harmonic Elimination Stepped-Waveform (SHESW) method which is more appropriate for MLI topology. Using this method with the MLI topology [34], It is possible to achieve a low THD output waveform without using a filter circuit.

THD is calculated as the proportion of the respective RMS voltages with all harmonic components (from its 2nd harmonic on) to the RMS voltage of the frequency components (the frequency response is the main frequency of the signal, i.e., Frequency will be determined whenever the signal is measured with an oscilloscope) [35]. The mathematical description of THD is shown in Equation 1 (note that voltage is often used in this equation [36]: but current can also be used):

TABLE 3. operating modes of 31-level cascaded inverter

Modes	Current Directions of Load	Active Source Voltage	Output Voltage (V_0)	
			Magnitude of V_0(Volts)	
Mode-1	Vdc_1-S_5-S_1-R_0-S_4-Vdc_4-S_8-Vdc_3-S_7-Vdc_2-S_6-Vdc_1	Vdc_1+Vdc_2+Vdc_3+Vdc_4	+15Vdc	+30
Mode-2	Vdc_2-S_6-D_1-S_1-R_0-S_4-Vdc_4-S_8-Vdc_3-S_7-Vdc_2	Vdc_2+Vdc_3+Vdc_4	+14Vdc	+28
Mode-3	Vdc_1-S_5-S_1-R_0-S_4-Vdc_4-S_8-Vdc_3-S_7-D_2-Vdc_1	Vdc_1 +Vdc_3+Vdc_4	+13Vdc	+26
Mode-4	Vdc_3-S_7-D_2-D_1-S_1-R_0-S_4-Vdc_4-S_8-Vdc_3	Vdc_3+Vdc_4	+12Vdc	+24
Mode-5	Vdc_1-S_5-S_1-R_0-S_4-Vdc_4-S_8-D_3-Vdc_2-S_6-Vdc_1	Vdc_1+Vdc_2 +Vdc_4	+11Vdc	+22
Mode-6	Vdc_2-S_6-D_1-S_1-R_0-S_4-Vdc_4-S_8-D_3- Vdc_2	Vdc_2 +Vdc_4	+10Vdc	+20
Mode-7	Vdc_1-S_5-S_1-R_0-S_4-Vdc_4-S_8-D_3-D_2-Vdc_1	Vdc_1+Vdc_4	+9Vdc	+18
Mode-8	Vdc_4-S_8-D_3-D_2-D_1-S_1-R_0-S_4-Vdc_4	Vdc4	+8Vdc	+16
Mode-9	Vdc_1-S_5-S_1-R_0-S_4-D_4-Vdc_3-S_7-Vdc_2-S_6-Vdc_1	Vdc_1+Vdc_2+Vdc_3	+7Vdc	+14
Mode-10	Vdc_2-S_6-D_1-S_1-R_0-S_4-D_4-Vdc_3-S_7-Vdc_2	Vdc_2+Vdc_3	+6Vdc	+12
Mode-11	Vdc_1-S_5-S_1-R_0-S_4-D_4-Vdc_3-S_7-D_2-Vdc_1	Vdc_1+Vdc_3	+5Vdc	+10
Mode-12	Vdc_3-S_7-D_2-D_1-S_1-R_0-S_4-D_4-Vdc_3	Vdc3	+4Vdc	+8
Mode-13	Vdc_1-S_5-S_1-R_0-S_4-D_4-D_3-Vdc_2-S_6- Vdc_1	Vdc_1+Vdc_2	+3Vdc	+6
Mode-14	Vdc_2-S_6-D_1-S_1-R_0-S_4-D_4-D_3-Vdc_2	Vdc_2	+2Vdc	+4
Mode-15	Vdc_1-S_5-S_1-R_0-S_4-D_4-D_3-D_2-Vdc_1	Vdc_1	+Vdc	+2
Mode-16	R_0-S_1- S_3- R_0	0	0	0
Mode-17	Vdc_1-S_5-S_3-R_0-S_2-D_4-D_3-D_2-Vdc_1	-Vdc_1	-Vdc	-2
Mode-18	Vdc_2-S_6-D_1-S_3-R_0-S_2-D_4-D_3-Vdc_2	-Vdc_2	-2Vdc	-4
Mode-19	Vdc_1-S_5-S_3-R_0-S_2-D_4-D_3-Vdc_2-S_6- Vdc_1	-Vdc_1-Vdc_2	-3Vdc	-6
Mode-20	Vdc_3-S_7-D_2-D_1-S_3-R_0-S_2-D_4-Vdc_3	-Vdc_3	-4Vdc	-8
Mode-21	Vdc_1-S_5-S_3-R_0-S_2-D_4-Vdc_3-S_7- D_2- Vdc_1	-Vdc_1-Vdc_3	-5Vdc	-10
Mode-22	Vdc_2-S_6-D_1-S_3-R_0-S_2-D_4-Vdc_3-S_7-Vdc_2	-Vdc_2-Vdc_3	-6Vdc	-12
Mode-23	Vdc_1-S_5-S_3-R_0-S_2-D_4-Vdc_3-S_7-Vdc_2-S_6-Vdc_1	-Vdc_1-Vdc_2-Vdc_3	-7Vdc	-14
Mode-24	Vdc_4-S_8-D_3-D_2-D_1-S_3-R_0-S_2-Vdc_4	-Vdc_4	-8Vdc	-16
Mode-25	Vdc_1-S_5-S_3-R_0-S_2-Vdc_4-S_8-D_3-D_2-Vdc_1	-Vdc_1-Vdc_4	-9Vdc	-18
Mode-26	Vdc_2-S_6-D_1-S_3-R_0-S_2-Vdc_4-S_8-D_3- Vdc_2	-Vdc_2 -Vdc_4	-10Vdc	-20
Mode-27	Vdc_1 -S_5-S_3-R_0-S_2-Vdc_4-S_8-D_3- Vdc_2-S_6-Vdc_1	-Vdc_1-Vdc_2 -Vdc_4	-11Vdc	-22
Mode-28	Vdc_3-S_7-D_2-D_1-S_3-R_0-S_2-Vdc_4-S_8-Vdc_3	-Vdc_3-Vdc_4	-12Vdc	-24
Mode-29	Vdc_1-S_5-S_3-R_0-S_2-Vdc_4-S_8-Vdc_3-S_7-D_2-Vdc_1	-Vdc_1 -Vdc_3-Vdc_4	-13Vdc	-26
Mode-30	Vdc_2-S_6-D_1-S_3-R_0-S_2-Vdc_4-S_8-Vdc_3-S_7-Vdc_2	-Vdc_2-Vdc_3-Vdc_4	-14Vdc	-28
Mode-31	Vdc_1-S_5-S_3-R_0-S_2-Vdc_4-S_8-Vdc_3-S_7-Vdc_2-S_6-Vdc_1	-Vdc_1-Vdc_2-Vdc_3-Vdc_4	-15Vdc	-30

Since the magnitudes of both the harmonics are required to calculate THD, Fourier analysis can also be used to impacts resulting in THD.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n\_rms}^2}}{V_{fund\_rms}} \tag{10}$$

V_{n_rms} is the nth harmonic for RMS voltage.
V_{fund_rms} fundamental frequency for RMS voltage.

Harmonics Reduction Method and Fourier Transform

Fourier transform technique is utilized for the output voltage of the MLI, which is having symmetry in odd quarter-wave [37], [38]. The MLI Fourier series expression is expressed as (10).

The fundamental switching frequency control method is generalized if DC voltage values are equal in MLI as expressed using equations shown below.

$$V(t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi} \left(\cos(n\theta_1)\cos(n\theta_2)\right. \\ \left.\cos\left(n\theta_3\right) + - - - + \cos\left(n\theta_s\right)\sin(n\omega t)\right. \tag{11}$$

According to the equation (10), there will be no even harmonics in output voltage since the waveform is odd quarter-

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wave in symmetric. The equation is expressed as follows [39]using harmonic elimination theory to eliminate the nth harmonic:

$$(cos(n\theta_1)(cos(n\theta_1)(cosn\theta_2) + ... + (cos\theta_s) = 0 \quad (12)$$

From equation (3), the peak values of odd harmonics in the form of switching angle i.e. θ_1, θ_2 and θ_s. Usually, an equation with a switching angle $'s'$ is active to estimate the fundamental frequency value and lower order harmonic of $s-1$ is eliminated. The three switching angle transforms (11) is as shown below:

$$v(t) = \sum_{n=1,3,5...}^{\infty} \frac{4v_{dc}}{n\pi}(cos(n\theta_1))(cos(n\theta_2)) \\ (cos(n\theta_3)) + sin(n\omega t) \quad (13)$$

Transcendental Equations and Their Solutions

The third and fifth order harmonics are extracted using harmonic equations. The harmonic equation that follows is as follows [40]:

$$cos(\theta_1) + cos(\theta_2) + cos(\theta_3) = \frac{\pi V_1}{4V_{dc}} \quad (14)$$

$$cos(3\theta_1) + cos(3\theta_2) + cos(3\theta_3) = 0 \quad (15)$$

$$cos(5\theta_1) + cos(5\theta_2) + cos(5\theta_3) = 0 \quad (16)$$

equation (4) can be expressed as

$$cos(\theta_1) + cos(\theta_2) + cos(\theta_3) = m \quad (17)$$

where,

$$m = \frac{\pi V_1}{4V_{dc}} \quad (18)$$

The equations (4) and (6) are transcendental harmonics, it is used as an iterative process such as Newton-Raphson method [32]. The transcendental calculations are transformed into polynomial equations due to their characterization of the harmonic content, then the subsequent method is applied to finding the solution.

The solution is sought by converting the transcendental equations that characterize the harmonic substance into polynomial equations. The obtained groups of solutions are observed for their corresponding THD to select the set, which generates the least harmonic elimination typically due to the 11th and 13th harmonics.

IV. CONTROL METHODS FOR MULTILEVEL INVERTER

Fig. 9. depicts the Controller integrated into a Multilevel inverter. In this article Fuzzy logic and ANFIS are the two control techniques that will be required to control the output RMS voltage for the proposed modified 31-level asymmetrical cascaded inverter. The Fuzzy Logic Controller and ANFIS controller are compared with the parameters such as Settling Time, Overshoot, RMS Voltage values, Peak Time, Peak value, and Rise Time of a 31-level asymmetrical cascaded

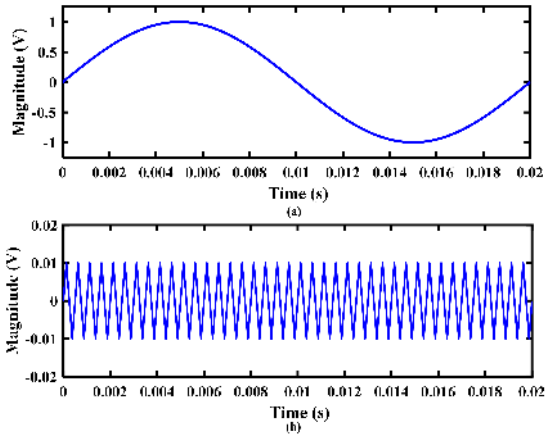

FIGURE 5. (a) Sinusoidal reference signal, (b) Carrier triangular signal.

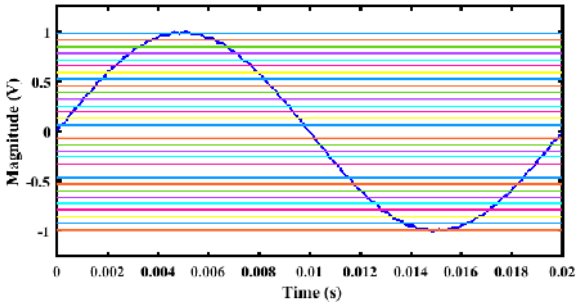

FIGURE 6. Comparison of carrier super imposed sinusoidal signal with different DC signal.

inverter. The fuzzy logic and ANFIS controller works with imprecise inputs, it does not need an accurate mathematical model and it can handle nonlinearity well. Besides, fuzzy is more robust as compared to the conventional non-linear controller. The following section gives the details of the fuzzy logic controller and ANFIS controller.

A. FUZZY-LOGIC CONTROLLER

Fuzzy logic is a reasoning system that is similar to human reasoning. This method of decision-making is close to that used by humans [41]. And it requires all transitional possible among YES or NO. It comprises of four main elements: Rules, fuzzifier, defuzzifier, intelligence [42], [43]. The fuzzy logic control diagram is as displayed in Fig. 10.

Rules: It includes all of the experts rules and the IF THEN condition [44]. The fuzzy theory offers various effective methods for designing and tuning fuzzy controllers to govern the decision-making mechanism [45]. Usually, this development reduces the number of fuzzy rules as well. The types of fuzzy rules are as follows.

Ri : If e is $\mathrm{A_i}$, ce is $\mathrm{B_i}$ then $\delta \mathrm{m_n}$ is $\mathrm{C_i}$

fuzzy subsets of their discourse universe are A_i, B_i, and C_i. Every universe of discourse is divided into 7 sections into fuzzy subsets: Positive Big (PB), Positive Medium (PM), Positive Small (PS), Zero (ZE), Negative Small (NS), Negative Medium (NM), and Negative Big (NB). Here e and

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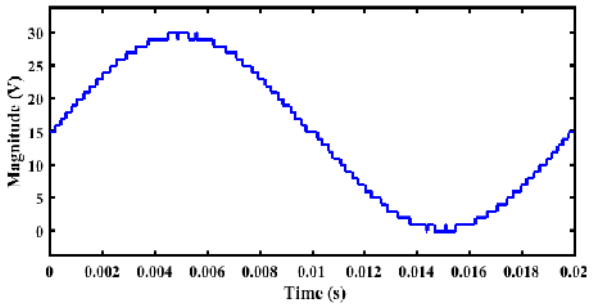

FIGURE 7. Comprehensive signal.

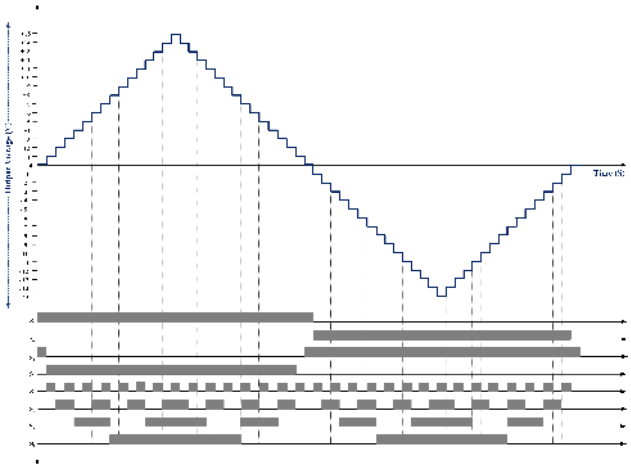

FIGURE 8. The expected output voltage waveform of 31-level.

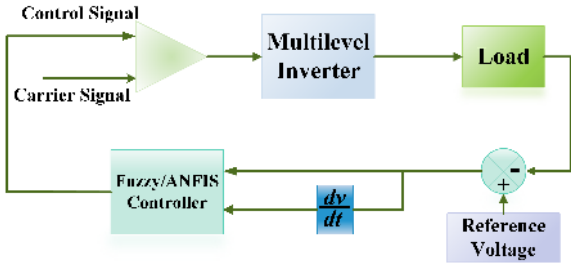

FIGURE 9. Controller integrated to Multilevel inverter.

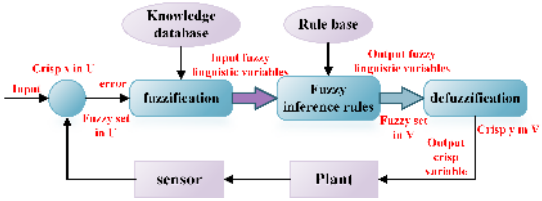

FIGURE 10. Fuzzy logic controller block diagram.

ce have normalized values of [-1,1], and m_n has a range of [-1,1]. A maximum of forty-nine rules is used for any combination of error (e) and change in error (ce). Table 4 shows how to build a rule base.

each rule has two components in the inference result. According to the rule, the specific rule of the weighting function W_i as well as the rate of membership of modulated signal C_i, can be written as

$$Z_i = \min\{\mu_e(e), \mu_{ce}(ce)\} \cdot C_i \tag{19}$$

$$= W_i C_i \tag{20}$$

Fuzzifier: The input or crisps number is converted into fuzzy sets in this process. Sensors will calculate it in crisp inputs and send it to the control system for processing.

Inference engine or intelligence: it defines the degree of similarity between fuzzy input fields. It will determine which rules will be implemented. Taking the fire rules and combining them with the control acts.

Defuzzifier: Fuzzy output is the process of transforming a fuzzy element into a crisp member or minimizing a fuzzy set to a crisp set [46].

Fuzzy logic has been used in numerous applications such as facial pattern recognition, air conditioners, washing machines, vacuum cleaners, antiskid braking systems, transmission systems, control of subway systems and unmanned helicopters, knowledge-based systems for multiobjective optimization of power systems, weather forecasting systems, models for new product pricing or project risk assessment, medical diagnosis and treatment plans, and stock trading. Fuzzy logic has been successfully used in numerous fields such as control systems engineering, image processing, power engineering, industrial automation, robotics, consumer electronics, and optimization.

B. ANFIS CONTROLLER

ANFIS design is envisioned in Fig.11. ANFIS is the combination of both neural networks and fuzzy inference systems. Thus, it offers the benefits of inference mechanism of the fuzzy system and learning ability of neural networks [47]. An excellent experience presentation and reasoning skills of fuzzy sense that possess the abilities to change over the starring position of the association to accomplish the desired output [48]. An adaptive network is based on the FIS that combines practically all the types of neural network simulations [37]. ANFIS is a hybrid soft computing model composed of a neuro-fuzzy system in which a fuzzy inference system can be trained by a neural network learning algorithm. ANFIS was being set up as both an essential part for fine-tuning the membership functions parameters of Fuzzy inference systems [44].

To obtain an efficient FIS to control the output of the inverter a proper Artificial Neural network is trained based on the input and output of the inverter. This forecast includes membership rules, if-then rules, and fuzzy logic operators [48]. Two kinds of fuzzy schemes are typically used which are Mamdani and Sugeno models. The following five essential data handling cycles in ANFIS operation comprise

TABLE 4. Rule base table

E/ce	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

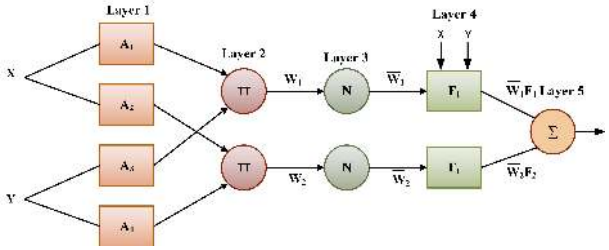

FIGURE 11. ANFIS Architecture.

a fuzzy operative application, input fuzzification, request for technique, output expansion, and defuzzification [49]. ANFIS is usually a multi-layered back-propagation system where each device performs a particular role on inbound signals(node function) [44]. In this system, the output 'z'is based on the inputs 'x'and 'y'which are the error (e) and change in error (ce) for the system. In the rule-base, there are Takagi and Sugeno type of fuzzy if-then rules.

Rule 1: IF $x = A1, y = B1$; THEN $f1 = p1x + q1y + R1$

Rule 2: IF $x = A2, y = B2$; THEN $f2 = p2x + q2y + R2$

This ANFIS controller is widely used for controlling the non-linear system. This controller is used in the Temperature water bath controller, planes, voltage instability predictor.

V. RESULTS AND DISCUSSION

The modified asymmetrical 31-level cascaded inverter using the Super Imposed Carrier Pulse width Modulation (SICPWM) technique is modeled in MATLAB/Simulink and the Real-time simulation domain. The analysis was carried out without a controller and with fuzzy logic and an ANFIS controller.

A. SIMULATION RESULTS

1) 31-level modified cascaded inverter without controller

Using the MATLAB/Simulink the modified asymmetrical 31-level cascaded inverter using the SICPWM technique is simulated.

The following are the 31-level modified asymmetrical inverter simulation parameters considered for R-load:

- **Input voltage (DC)** = 30V ($Vdc_1 = 2V; Vdc_2 = 4V; Vdc_3 = 8V; Vdc_4 = 16V$)
- **Carrier switching frequency** f_s = 2 KHZ
- **R-Load**=100 Ω

The load-wide output voltage is 29.80V (RMS voltage is 21.07V). Fig. 12 depicts the load-wide output voltage. The current through the load is 0.298A. Fig. 13 Depicts the current through the load. Fig. 14 shows the Fast Fourier Transform (FFT) study of a 31-level asymmetrical cascaded inverter. The THD value from the FFT is 4.97%.

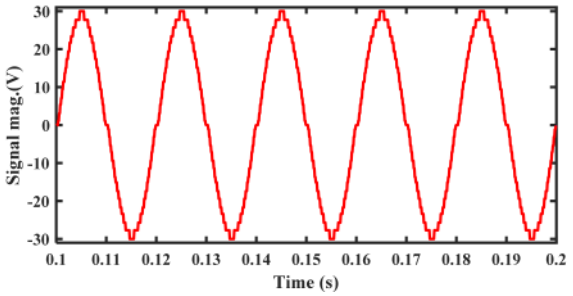

FIGURE 12. Load wide output voltage for 31-level modified asymmetrical inverter.

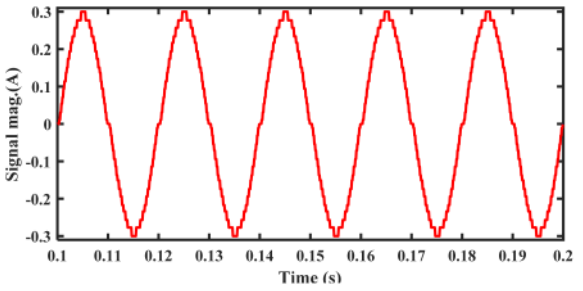

FIGURE 13. Output Current through load for 31-level modified asymmetrical inverter.

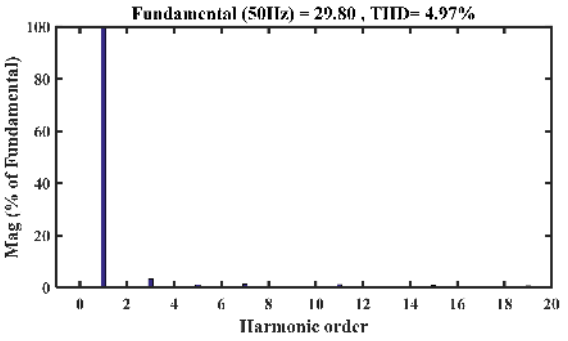

FIGURE 14. FFT Analysis for output voltage of 31-level modified asymmetrical inverter.

2) 31-level modified cascaded inverter with fuzzy controller

Fig. 15 depicts the designed fuzzy controller membership function. In this case, to create membership functions, the fuzzy logic controller is tuned by input values with a range of -35 to +35, dual inputs (e and ce), and a single output value is considered. 7-membership functions are considered from the total input and output values, a total of 49 rules are

made specifically for fuzzy controller. The designed fuzzy controller rules are as shown in Fig. 16 and the corresponding Surface plot of the fuzzy layout is visualized in Fig. 17.

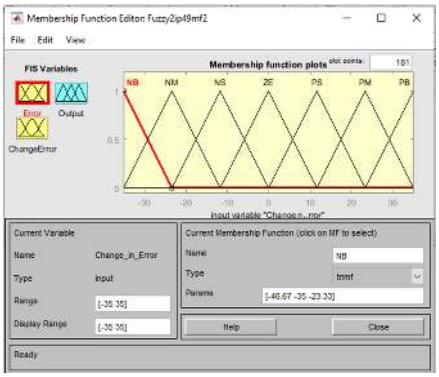

FIGURE 15. Designed fuzzy controller membership function.

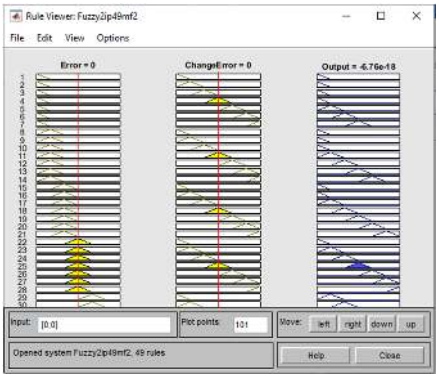

FIGURE 16. Designed fuzzy controller rules.

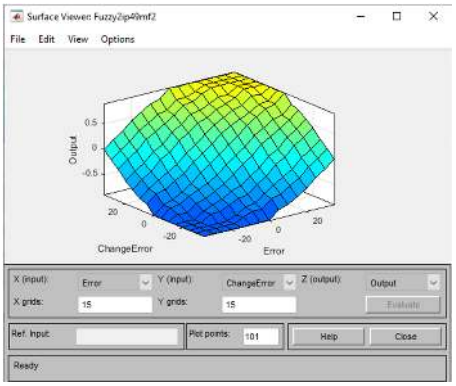

FIGURE 17. Surface plot of the fuzzy layout.

Fig. 18 depicts the reference voltage and RMS output voltage of a Fuzzy logic-based 31-level cascaded inverter. From Fig. 18, the reference voltage is held at 15V in the beginning and then increased to 22V after 1sec. The output voltage across the load for a 31-level cascaded inverter with fuzzy logic is shown in Fig. 19. It can be seen that the pulse width is smaller at the beginning (while the reference voltage is 15V) and then rises after 1 second to boost the RMS output voltage to 21.98V. The minimum reference voltage is maintained at 15 V for 1 second. The FFT analysis of a 31-level asymmetrical cascaded inverter with a Fuzzy controller is presented in Fig. 20. The THD factor from the FFT is 4.15%.

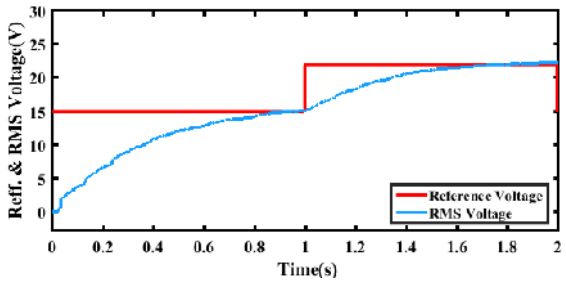

FIGURE 18. Reference and output RMS voltage for 31-level inverter with fuzzy.

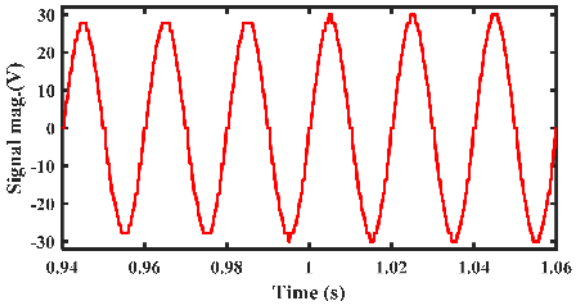

FIGURE 19. Output voltage across load with Fuzzy logic controller.

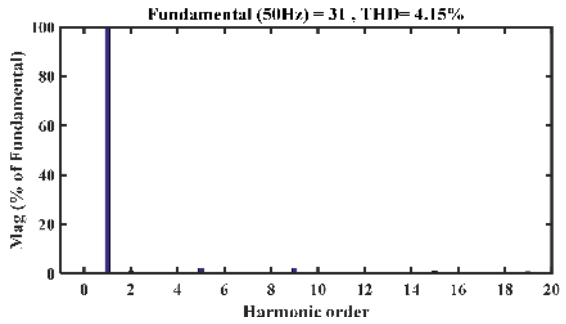

FIGURE 20. FFT analysis for 31-level inverter with fuzzy.

3) 31-level modified cascaded inverter with ANFIS controller

ANFIS training: In addition to getting ANFIS training data sets, the input voltage is varied from -35V to +35V in a step of 0.07V using the MATLAB/Simulink model of the 31-level modified cascaded inverter. Each pair of training data has its input voltage captured. The Designed ANFIS controller membership function is depicted in Fig. 21. It has a single output, dual inputs (e and ce), and For each input has

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seven membership functions. The seven input membership functions are used to generate 49 fuzzy set rules, which are shown in Fig. 22. 1000 samples of training data sets and 1000 epochs are often used during the training period. The ANFIS generates a FIS utilizing this predefined input or output data set, with Membership function parameters tuned using a hybrid optimization technique combining backpropagation and least square algorithms. The training error has been minimized, and the ANFIS output closely matches the system's actual output. Fig. 23 depicts the ANFIS training error waveform. The ANFIS structure generated in MATLAB is shown in Fig. 24. and the corresponding Surface plot of the fuzzy layout is visualized in Fig. 25.

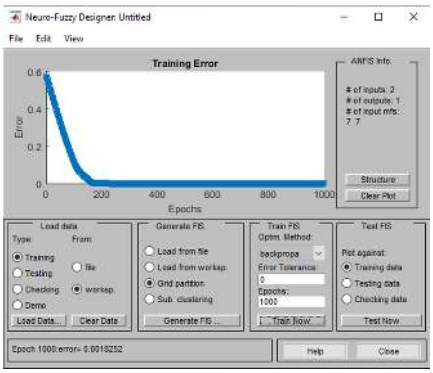

FIGURE 23. ANFIS training error

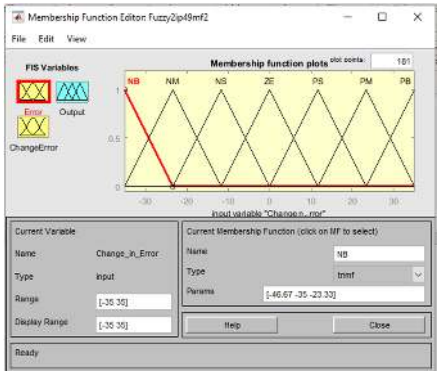

FIGURE 21. Designed ANFIS controller membership function.

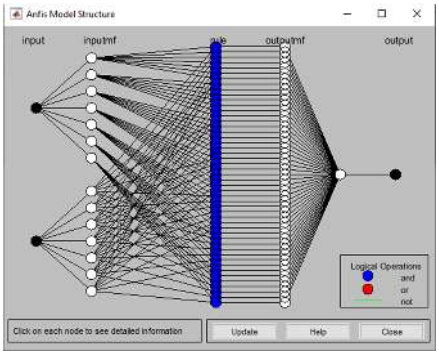

FIGURE 24. ANFIS structure generated in the MATLAB.

FIGURE 22. Designed ANFIS controller rules.

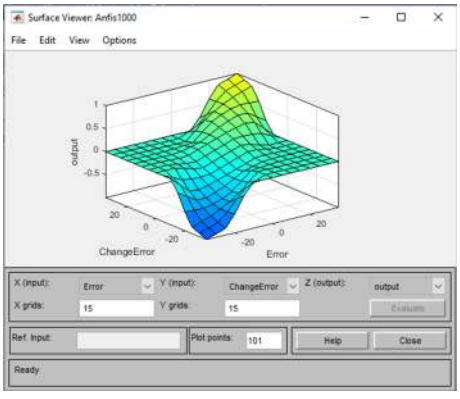

FIGURE 25. Surface view of the ANFIS controller designed.

Fig. 26 shows the reference voltage and output RMS voltage of a 31-level cascaded inverter using an ANFIS controller. From Fig. 26, the reference value is held at 15V in the beginning and then increased to 22V after 1sec. The load-wide output voltage for ANFIS controlled 31-level cascaded inverter is visualized in Fig. 27. It could be observed that the width of the pulse is smaller in beginning (while the reference voltage is 15V) and then rises after 1 second to enhance the output RMS voltage to 22.217V. The minimum reference voltage is kept constant at 15 V for 1 second. The FFT evaluation of a 31-level asymmetrical cascaded inverter with ANFIS is visualized in Fig. 28. The THD from the FFT is 3.77%.

4) Step response comparison of 31-level cascaded inverter with controllers.

For a 31-level Asymmetrical cascaded Inverter, a comparative study of step response factors such as (i) Rise Time, (ii) Settling Time, (iii) Overshoot, (iv) Peak value, (v) Peak Time, and (vi) RMS Voltage values was performed using an FL and ANFIS controller. Step response comparison is tabulated in Table 4 and the corresponding chart is represented in Fig. 29.

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TABLE 5. Step response comparison of 31-level cascaded inverter with controllers

Parameters	Asymmetrical 31-level Cascaded Inverter	
	With Fuzzy Controller	With ANFIS Controller
Rise Time	1.2435	1.0907
Settling Time	1.7026	1.4138
Settling Min	19.7991	20.1842
Settling Max	21.9817	22.217
Overshoot	0	0.0123
Peak Value	21.9817	22.217
Peak Time	1.8135	1.9869

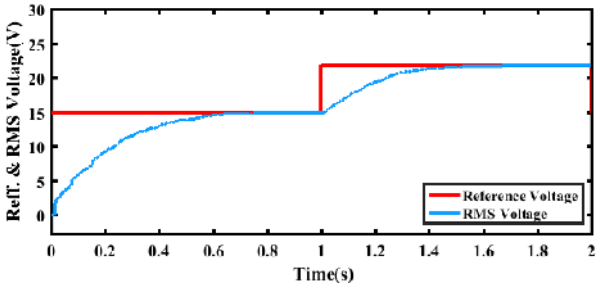

FIGURE 26. Reference and output RMS voltage of 31-level inverter with ANFIS.

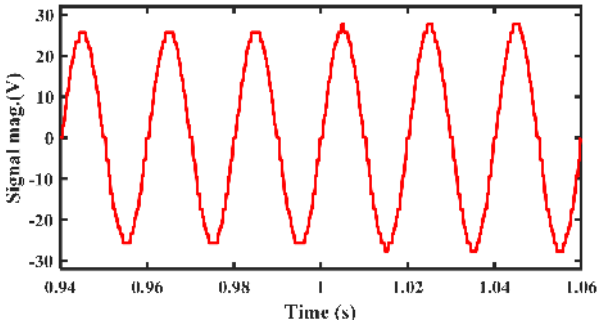

FIGURE 27. Output voltage across load with ANFIS controller.

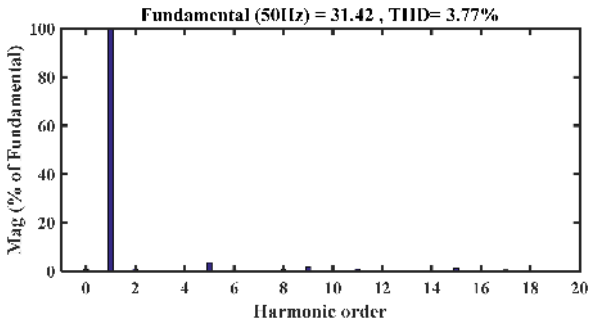

FIGURE 28. FFT analysis for 31-level inverter with ANFIS.

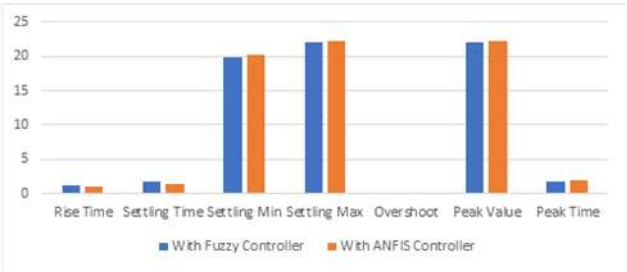

FIGURE 29. Step response comparison chart of 31-level cascaded inverter with controllers.

5) Comparison of RMS voltage and THD parameters of 31-level cascaded inverter with controllers

The RMS voltage and THD of 31-level asymmetrical cascaded inverter without the controller and with fuzzy logic and ANFIS controller is illustrated in Table 5. and corresponding charts as shown in Fig. 30 and Fig. 31. From Table 5 it can be noticed that the ANFIS gives provides better efficiency as compared to the fuzzy controller.

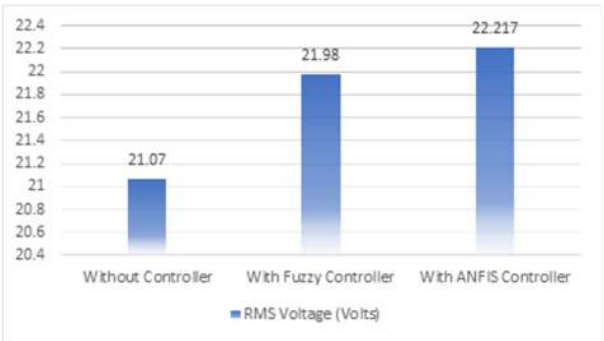

FIGURE 30. RMS output voltage Comparison of 31-level cascaded inverter with and without controllers

6) Dynamic conditions for Input Voltage and Resistive Load

The dynamic condition is carried out for different DC source voltages and variable resistive loads. The DC source voltages are taken as Vdc=30V, Vdc=60V, and Vdc=45V. For each dc source voltage, three different resistive loads: R= 100Ω,

TABLE 6. Comparison of RMS voltage and THD parameters of 31-level cascaded inverter with and without controllers

Parameter	Asymmetrical 31-Level Cascaded Inverter		
	Without Controller	With Fuzzy Controller	With ANFIS Controller
RMS Voltage	21.07	21.98	22.217
THD	4.97%	4.15%	3.77%

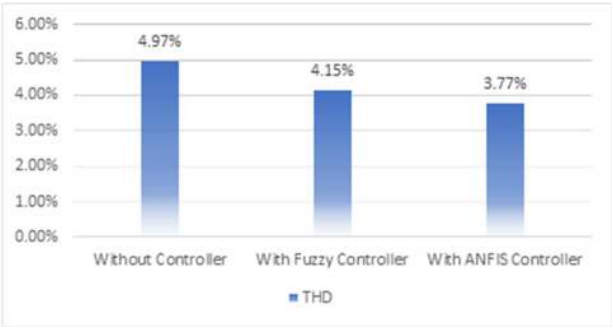

FIGURE 31. THD Comparison of 31-level cascaded inverter with and without controllers

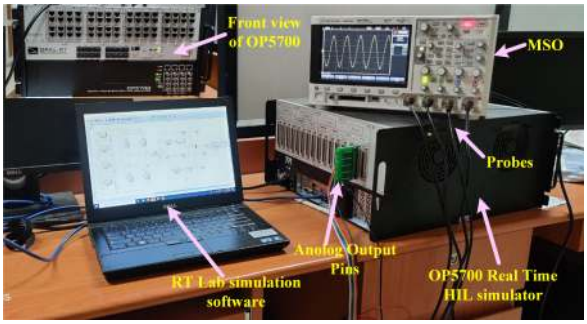

FIGURE 32. Real-time HIL setup.

R=200Ω, and R=150Ω respectively. From these conditions, the Fuzzy and ANFIS RMS output voltage is controlled and maintained constant based on the reference voltage. The resultant values for different DC source Voltage and Resistive Loads are tabulated in Table 7.

TABLE 7. Dynamic conditions at different Input Voltage and Resistive Load

Input Voltage (V)	Resistive Load (Ω)	Fuzzy RMS Output Voltage (V)	ANFIS RMS Output Voltage (V)
30	100 200 150	21.98	22.21
60	100 200 150	21.98	22.21
45	100 200 150	21.98	22.21

B. REAL TIME SIMULATION RESULTS

The Real-time simulation HIL setup is shown in Fig. 32. The modified asymmetrical 31-level cascaded multilevel inverter using the superimposed carrier pulse width modulation (SICPWM) technique without the controller and with fuzzy and ANFIS controller are built-in RT lab simulation and dumped into the OP5700 real-time HIL simulator to test the system performance.

1) 31-level modified cascaded inverter without controller

The load-wide output voltage is 29.77V (RMS voltage is 21.05V). The load-wide output voltage is given in Fig. 33. The current through the load is 0.297A. Fig. 34. Depicts the current through the load. The FFT analysis of the 31-level asymmetrical inverter is presented in Fig 35. The THD value from FFT is 5.03%.

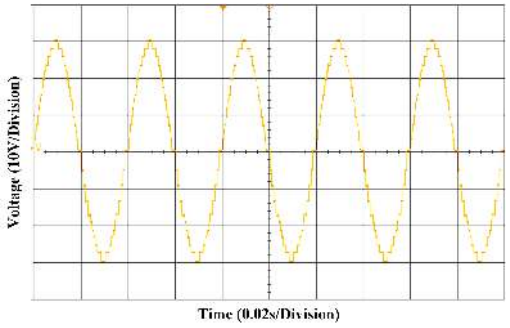

FIGURE 33. Output voltage across the load without controller.

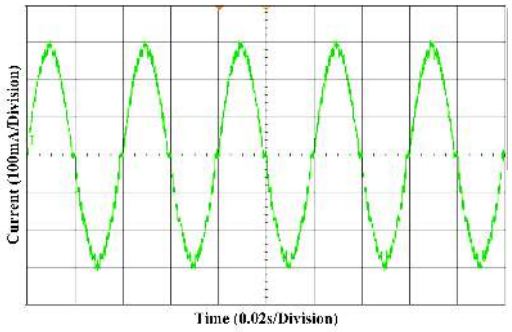

FIGURE 34. Current through load without controller.

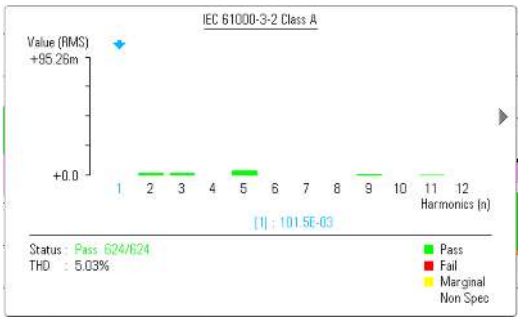

FIGURE 35. Fast Fourier transform (FFT).

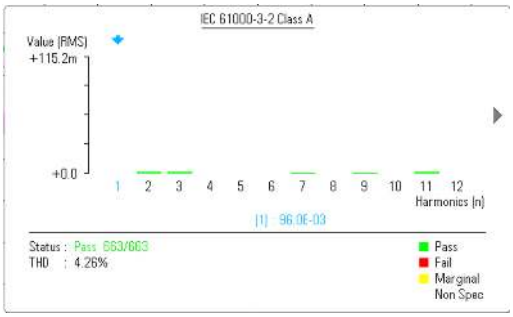

FIGURE 38. Fast Fourier transform (FFT) with Fuzzy logic controller.

2) Fuzzy controlled 31-level modified cascaded inverter

Fig. 36 shows the reference voltage and RMS voltage of a 31-level cascaded inverter using Fuzzy logic. From Fig. 36, the reference voltage is held at 15V in the beginning and then increased to 22V after 1sec. The load-wide output voltage for Fuzzy controlled 31-level cascaded inverter is shown in Fig. 37. It could be observed that the width of the pulse is smaller in the beginning (while the reference voltage is 15V) and then rises after 1 second to boost the RMS output voltage to 21.89V. The minimum reference voltage is maintained constant at 15 V for 1 second. The FFT analysis of 31-level asymmetrical cascaded inverter with FLC is illustrated in Fig. 38. The THD value from the FFT is 4.26%.

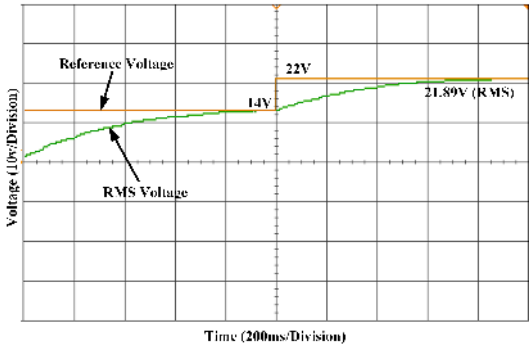

FIGURE 36. Reference and RMS output voltage with Fuzzy logic controller.

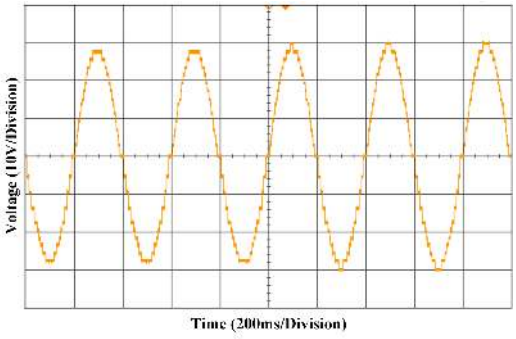

FIGURE 37. output voltage across the load with Fuzzy logic controller.

3) ANFIS controlled 31-level modified cascaded inverter

Fig. 39 shows the reference voltage and output RMS voltage of ANFIS controlled 31-level cascaded inverter. From Fig. 39, the reference voltage is held at 15V in the beginning and then increased to 22V after 1sec. The load-wide output voltage for a 31-level cascaded inverter with an ANFIS controller is shown in Fig. 40. It could be observed that the width of the pulse is smaller in the beginning (while the reference voltage is 15V) and then rises after 1 second to enhance the output RMS voltage to 21.96V. The minimum reference voltage is maintained constant at 15 V for 1 second. The FFT analysis of a 31-level asymmetrical cascaded inverter with ANFIS is illustrated in Fig. 41. The THD from the FFT is 3.98%.

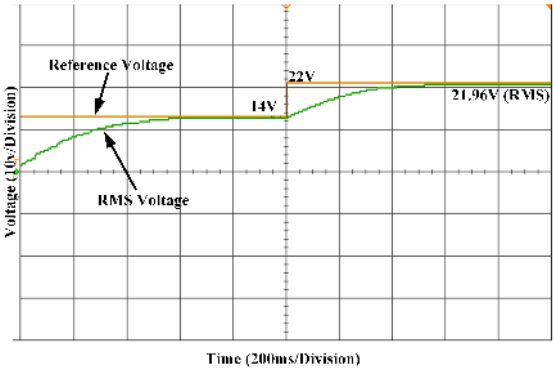

FIGURE 39. Reference and RMS output voltage with ANFIS controller.

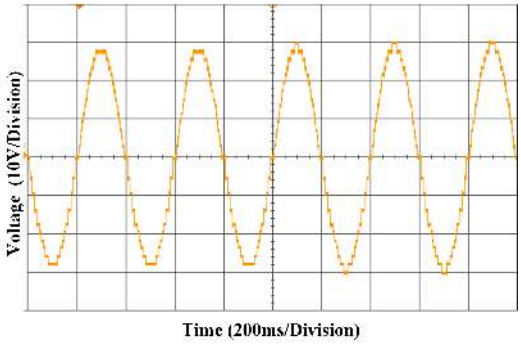

FIGURE 40. output voltage across the load with ANFIS controller.

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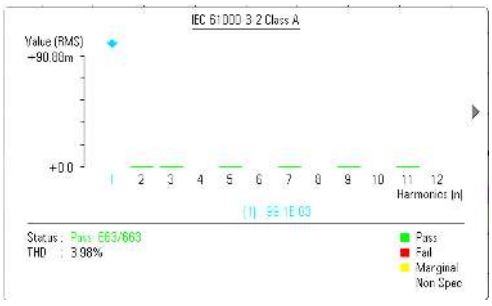

FIGURE 41. Fast Fourier transform (FFT) with ANFIS controller.

The fuzzy logic and ANFIS controller track the input values and control the converter to supply desired current output. The control process has been developed selecting the most accurate modulation index for the multilevel inverter which directly affects the output power. This closed-loop analysis improves the stability of the system without disturbing the quality of the output. These controllers are used to maintain the constant output voltage based on the reference voltage in the controller design, even when there is a change in input voltage to the inverter. The fuzzy logic and ANFIS controller works with imprecise inputs, it does not need an accurate mathematical model and it can handle nonlinearity well.

4) comparison of simulation and real-time simulation results for 31-level asymmetrical cascaded inverter

Comparison of both simulation and Real-Time simulation results with RMS voltage and THD of 31-level asymmetrical inverter without the controller and with FL and ANFIS controller is presented in the Table. 8 and corresponding charts as shown in Fig. 42 and Fig. 43. From Table 8 it could be noticed that the output RMS voltage and THD are slightly more in Real-Time simulation as compared to simulation for without and with controllers.

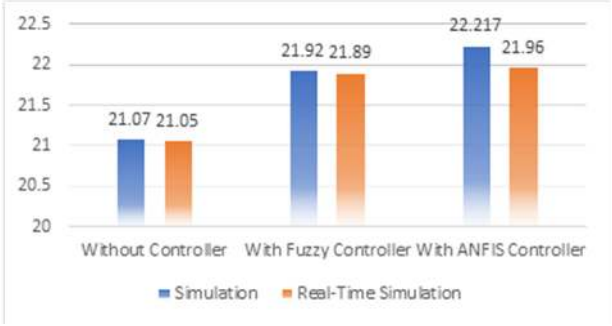

FIGURE 42. RMS output voltage comparison of simulation and Real-Time simulation.

VI. CONCLUSION

The proposed modified 31-level Asymmetrical cascaded inverter with and without Fuzzy logic and ANFIS controller is presented in this paper, demonstrating a substantial change in THD percentages and RMS voltage control. The proposed modified 31-level Asymmetrical cascaded inverter

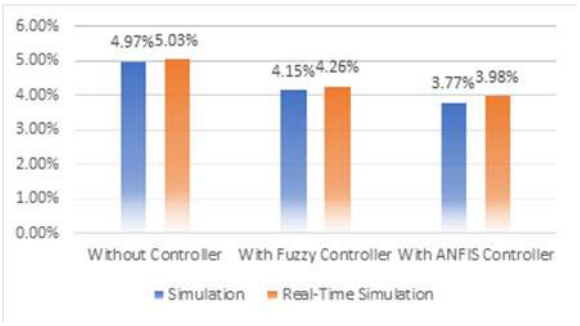

FIGURE 43. THD comparison of simulation and Real-Time simulation.

with Fuzzy logic and ANFIS controller is designed in MATLAB/SIMULINK and verified in Real-Time simulation using OPAL-RT 5700. By using Super Imposed Carrier Pulse Width Modulation (SIC-PWM) with and without the controller, the RMS output voltage is controlled and THD is decreased. The performance of step response parameter values is evaluated and compared for Fuzzy and ANFIS controlled 31-level Asymmetrical cascaded inverter. The dynamic conditions were also analyzed for different DC source voltages and variable resistive loads, the RMS output voltage is controlled and maintained constant (i.e., RMS value is 21.98V for Fuzzy and 22.21V for ANFIS). Using the analytical solution for a 31-level cascaded inverter, it has been identified that the THD value for without a controller is 4.97%, with the fuzzy logic controller is 4.15% and with ANFIS controller is 3.77%. As compared to the Fuzzy logic controller, the ANFIS controller gives better performance. i.e., the RMS Voltage is controlled and settled in less settling time.

REFERENCES

[1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135–151, 2016.

[2] W. A. Halim, S. Ganeson, M. Azri, and T. N. A. T. Azam, "Review of Multilevel Inverter Topologies and Its Applications," no. January 2016, 2018.

[3] R. A. Krishna and L. P. Suresh, "A brief review on multi level inverter topologies," *Proceedings of IEEE International Conference on Circuit, Power and Computing Technologies, ICCPCT 2016*, 2016.

[4] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies," *Renewable and Sustainable Energy Reviews*, vol. 76, no. July 2016, pp. 788–812, 2017. [Online]. Available: http://dx.doi.org/10.1016/j.rser.2017.03.066

[5] F. Dijkhuizen, "Multilevel converters : review , form , function and motivation," *Ever 2012*, p. 7, 2012.

[6] Y. Suresh, J. Venkataramanaiah, A. K. Panda, C. Dhanamjayulu, and P. Venugopal, "Investigation on cascade multilevel inverter with symmetric, asymmetric, hybrid and multi-cell configurations," *Ain Shams Engineering Journal*, vol. 8, no. 2, pp. 263–276, 2017. [Online]. Available: http://dx.doi.org/10.1016/j.asej.2016.09.006

[7] Z. Wang, K. Liao, K. Zhang, X. Huang, and Z. Kong, "An improved ripple suppression method based on flying-capacitor modular multilevel converter for high performance MV drivers," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 2571–2575, 2017.

[8] Basavaraja D.S., A. D. Kulkarni, and T. Ananthapadmanabha, "A Modular Single-phase Multistring Multilevel Inverter Topology for Distributed

TABLE 8. Comparison of simulation and real time simulation results for 31-level inverter

Parameter	Asymmetrical 31-Level Cascaded Inverter					
	Without Controller		With Fuzzy Controller		With ANFIS Controller	
	Simulation	Real-Time Simulation	Simulation	Real-Time Simulation	Simulation	Real-Time Simulation
RMS Voltage	21.07	21.05	21.92	21.89	22.217	21.96
THD	4.97%	5.03%	4.15%	4.26%	3.77%	3.98%

Energy Resources," *Procedia Technology*, vol. 21, pp. 569–574, 2015. [Online]. Available: http://dx.doi.org/10.1016/j.protcy.2015.10.057

[9] J. Sathik, M. Ali, and V. Krishnaswamy, "An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications," *Renewable and Sustainable Energy Reviews*, no. October 2016, pp. 1–21, 2017. [Online]. Available: http://dx.doi.org/10.1016/j.rser.2017.10.052

[10] N. A. Rahim, M. F. M. Elias, and W. P. Hew, "Transistor-clamped h-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," *IEEE transactions on industrial electronics*, vol. 60, no. 8, pp. 2943–2956, 2012.

[11] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3109–3118, 2011.

[12] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Conversion and Management*, vol. 50, no. 11, pp. 2761–2767, 2009. [Online]. Available: http://dx.doi.org/10.1016/j.enconman.2009.06.032

[13] S. Mekhilef and M. N. A. Kadir, "Voltage control of three-stage hybrid multilevel inverter using vector transformation," *IEEE Transactions on Power Electronics*, vol. 25, no. 10, pp. 2599–2606, 2010.

[14] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels," *IET power electronics*, vol. 7, no. 1, pp. 96–104, 2014.

[15] R. Samanbakhsh and A. Taheri, "Reduction of power electronic components in multilevel converters using new switched capacitor-diode structure," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7204–7214, 2016.

[16] R. R. Karasani, V. B. Borghate, P. M. Meshram, H. M. Suryawanshi, and S. Sabyasachi, "A three-phase hybrid cascaded modular multilevel inverter for renewable energy environment," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1070–1087, 2017.

[17] M. D. Siddique, S. Member, and M. A. Memon, "A New Multilevel Inverter Topology With Reduce Switch Count," *IEEE Access*, vol. 7, pp. 58 584–58 594, 2019.

[18] M. D. Siddique and S. Member, "A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress," *IEEE Access*, vol. 7, pp. 174 178–174 188, 2019.

[19] C. Dhanamjayulu and S. Meikandasivam, "Fuzzy controller based design of 125 level asymmetric cascaded multilevel inverter for power quality improvement," *Analog Integrated Circuits and Signal Processing*, vol. 101, no. 3, pp. 533–542, 2019. [Online]. Available: https://doi.org/10.1007/s10470-019-01468-0

[20] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count," *IEEE Access*, vol. 7, pp. 24 498–24 510, 2019.

[21] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, "Design and Hardware Implementation Considerations of Modified Multilevel Cascaded H-Bridge Inverter for Photovoltaic System," *IEEE Access*, vol. 7, pp. 16 504–16 524, 2019.

[22] A. Iqbal, M. D. Siddique, B. Prathap Reddy, and P. K. Maroti, "Quadruple Boost Multilevel Inverter (QB-MLI) Topology with Reduced Switch Count," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7372–7377, 2021.

[23] A. Iqbal, M. D. Siddique, B. Prathap Reddy, P. K. Maroti, and R. Alammari, "A New Family of Step-up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies with Dual Input Voltage Sources," *IEEE Access*, vol. 9, 2020.

[24] M. D. Siddique, B. P. Reddy, A. Iqbal, and S. Mekhilef, "Reduced switch count-based N-level boost inverter topology for higher voltage gain," *IET Power Electronics*, vol. 13, no. 15, pp. 3505–3509, 2020.

[25] M. Aly, E. M. Ahmed, H. Rezk, and E. A. Mohamed, "Marine Predators Algorithm Optimized Reduced Sensor Fuzzy-Logic Based Maximum Power Point Tracking of Fuel Cell-Battery Standalone Applications," *IEEE Access*, vol. 9, pp. 27 987–28 000, 2021.

[26] Y. Yang, H. Wen, M. Fan, L. He, M. Xie, R. Chen, M. Norambuena, and J. Rodriguez, "Multiple-Voltage-Vector Model Predictive Control with Reduced Complexity for Multilevel Inverters," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 1, pp. 105–117, 2020.

[27] P. Karuppusamy, A. M. Natarajan, and K. N. Vijeyakumar, "An adaptive neuro-fuzzy model to multilevel inverter for grid connected photovoltaic system," *Journal of Circuits, Systems and Computers*, vol. 24, no. 5, pp. 1–23, 2015.

[28] E. Deniz, O. Aydogmus, and Z. Aydogmus, "Implementation of ANN-based Selective Harmonic Elimination PWM using Hybrid Genetic Algorithm-based optimization," *Measurement: Journal of the International Measurement Confederation*, vol. 85, no. October 2017, pp. 32–42, 2016. [Online]. Available: http://dx.doi.org/10.1016/j.measurement.2016.02.012

[29] A. Mokhberdoran and A. Ajami, "Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology," vol. 29, no. 12, pp. 6712–6724, 2014.

[30] R. S. Alishah, D. Nazarpour, and S. H. Hosseini, "Novel Topologies for Symmetric , Asymmetric , and Cascade Switched-Diode Multilevel Converter With Minimum Number of Power Electronic Components," vol. 61, no. 10, pp. 5300–5310, 2014.

[31] S. S. Lee, M. Sidorov, N. Rumzi, and N. Idris, "A Symmetrical Cascaded Compact-Module Multilevel Inverter (CCM-MLI) With Pulsewidth Modulation," vol. 65, no. 6, pp. 4631–4639, 2018.

[32] T. R. Sumithira and A. Nirmal Kumar, "Elimination of harmonics in multilevel inverters connected to solar photovoltaic systems using ANFIS: An experimental case study," *Journal of Applied Research and Technology*, vol. 11, no. 1, pp. 124–132, 2013.

[33] H. Gupta, A. Yadav, and S. Maurya, "Multi carrier pwm and selective harmonic elimination technique for cascade multilevel inverter," in *2016 2nd International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)*. IEEE, 2016, pp. 98–102.

[34] B. H. Kumar and M. M. Lokhande, "Analysis of PWM techniques on multilevel cascaded H-Bridge three phase inverter," *2017 Recent Developments in Control, Automation and Power Engineering, RDCAPE 2017*, vol. 3, pp. 465–470, 2018.

[35] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies , modulation techniques and applications," *Renewable and Sustainable Energy Reviews*, vol. 76, no. January 2016, pp. 1248–1282, 2017. [Online]. Available: http://dx.doi.org/10.1016/j.rser.2017.03.121

[36] H. Abu-Rub, J. Holtz, J. Rodriguez, and Ge Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, 2010.

[37] G. Nageswara Rao, P. Sangameswara Raju, and K. Chandra Sekhar, "Harmonic elimination of cascaded H-bridge multilevel inverter based active power filter controlled by intelligent techniques," *International Journal of Electrical Power and Energy Systems*, vol. 61, pp. 56–63, 2014. [Online]. Available: http://dx.doi.org/10.1016/j.ijepes.2014.02.023

[38] D. Mohammadreza, "Analysis of different topologies of multilevel inverters," Master's thesis, 2010.
[39] A. Quedan, "Harmonics Elimination in Three Phase Cascade H- Bridge Multilevel Inverter Using Virtual Stage PWM," 2017.
[40] M. Derakhshanfar, "Analysis of different topologies of multilevel inverters," 2010.
[41] R. Palm, "Designs of Fuzzy Controllers," *Fuzzy Systems*, vol. 864, no. 98, pp. 227–272, 1998.
[42] T. Abdelkrim, N. Bouarroudj, A. Lakhdari, B. Benlahbib, A. Borni, and K. Benamrane, "Design novel fuzzy logic controller of photovoltaic conversion cascade based five levels inverter for stand-alone applications," in *2019 IEEE International Conference on Environment and Electrical Engineering and 2019 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe)*. IEEE, 2019, pp. 1–5.
[43] M. A. Hannan, Z. A. Ghani, M. M. Hoque, P. J. Ker, A. Hussain, and A. Mohamed, "Fuzzy logic inverter controller in photovoltaic applications: Issues and recommendations," *IEEE Access*, vol. 7, pp. 24 934–24 955, 2019.
[44] T. K. Mohan, "A Neuro-Fuzzy Controller for Multilevel Renewable Energy System," pp. 4120–4123, 2016.
[45] Y. Bai and D. Wang, "Fundamentals of fuzzy logic control âĂŤ fuzzy sets, fuzzy rules and defuzzifications," *Advances in Industrial Control*, no. 9781846284687, pp. 17–36, 2006.
[46] J. M. Mendel, "Introduction to Rule-Based Fuzzy Logic Systems," p. 123, 1995.
[47] P. P. Bonissone, "Adaptive Neural Fuzzy Inference Systems (ANFIS): Analysis and Applications," pp. 1–41, 2002.
[48] J.-S. Jang, "Anfis: adaptive-network-based fuzzy inference system," *IEEE transactions on systems, man, and cybernetics*, vol. 23, no. 3, pp. 665–685, 1993.
[49] I. To and F. Logic, "Chapter 3 Adaptive Neuro-Fuzzy Inference System," no. Jang 1993, pp. 33–46, 2005.

KOLA MURALIKUMAR received his Bachelor of Technology in Electrical and Electronics Engineering from JNTUH, Andhra Pradesh, India in 2006, and Master of Technology in Power Electronics and Electrical Drives from JNTUA, Andhra Pradesh, India in 2013. He is currently pursuing a Ph.D degree in power electronics with the Vellore Institute of Technology, Vellore, India. He has published five articles in international/national journals and conferences. His area of interest includes multilevel inverters, power converters, and fuzzy logic controllers.

DR. P. PONNAMBALAM is an Associate Professor with the VIT Vellore, India. Over the last 10 years, he has completed his B.E in Electrical and Electronics Engineering from Madurai Kamaraj University by 2002, he has completed his M.E in Power Electronics and Drives from Anna university Chennai by 2006, he has completed his Ph.D from Anna University Chennai by 2015, he has a good contribution towards the research in the area of Fuzzy Controllers for different multilevel inverters. He has many papers to his credit in many journals at the national and international level of repute. His area of interest is on Fuzzy Controllers for power electronic applications.