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Crisscross switched multilevel inverter using cascaded semi-half-bridge cells

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Abstract: A new cascaded multilevel inverter (MLI) is presented with the aim of utilising lesser number of switches, better modularity and reduced voltage stress. The new structure configured under symmetric and asymmetric mode, produces all odd and even voltage levels. This structure comprises semi-half-bridge cells connected in series with crisscross switches to generate any target level for synthesising the sinusoidal output voltage waveform. In extension to the proposed topology, subinverters derived from the proposed MLI are cascaded with an objective to produce more voltage levels with reduced standing voltage. Compared with the cascading H-bridge topology, the proposed MLI and the extended version uses lesser number of semi-conductor switches. The MATLAB R2013b-based simulation results along with the experimental results validate the proposed topology.

1 Introduction

The notion of multilevel power conversion is to synthesise stepped waveform from several sources to obtain an output voltage nearer to sinusoidal in shape and have the merits of operating at higher power and higher voltages with fewer series connected switches, reduced voltage stress, lesser EMI and improved modularity. Some of its major applications include industrial drives, FACTS devices, electric vehicles and renewable energy sources [1–5]. Cascaded multilevel inverter (MLI) has three benchmark classical-topologies namely cascading H-bridge inverters (CHBMLI), MLI with clamping diodes and flying capacitors [6–10]. The CHBMLI is more reliable for high-voltage applications due to isolated voltage sources and therefore free from voltage-balancing issues. However, it requires more number of components as the level increases. In diode clamped and FC inverters, the usages of more number of series connected clamping diodes and FC for higher level causes voltage-balancing problems.

In view of the above facts, many researchers expand their interest in deriving either hybrid topologies [11–13] from the benchmarked classical topologies or novel topologies [14, 15] to overcome the above issues. Besides, several novel switching mechanisms [16, 17] are also extended from three-level modulations [18] to MLI. The area of research is focused towards developing novel topologies rather than modulation strategies in order to achieve desired number of levels with minimum power components. Among several topologies, MLI derived from CHBMLI has attracted the researchers because of modular structure, operating at higher voltages and have control degree of freedom in choosing different voltage magnitudes for input sources.

Based on the selection of source voltage magnitudes, CHBMLI is further classified [19–30] into symmetric structure with equal magnitudes and asymmetric structure whose source voltage magnitudes are unequal. Compared with symmetric topology, the asymmetric topologies have the merit of utilising lesser number of power components for the same number of levels and also for higher number of levels.

Due to modularity, the symmetric structures can be easily extended to extract the required voltage levels. Two novel symmetric MLI configurations have been reported in [20, 21], one of the structures uses non-insulated DC sources with lesser number of switches and the other utilises series combination of basic cells and an H-bridge inverter. These structures increase the control circuit cost, complexity and size due to more number of bi-directional switches and gate drivers.

Two novel symmetric and asymmetric topologies have been proposed in [22] that consist of several semi-half-bridge modules with additional single DC source and an H-bridge inverter. The asymmetric topology is also derived from the same symmetric structure excluding additional single DC source. These topologies require devices with higher blocking voltage in the H-bridge side and hence more switch and gate drivers. This asymmetric structure has the capability of operating only in binary voltage ratios.

The other symmetric topology has been recommended in [23] is configured using a basic module with three DC sources, two pairs of complimentary switches and an H-bridge inverter for polarity reversal. The minimum step voltage (level 1) can be obtained by the algebraic subtraction among the voltage sources within a module. The least number of voltage level suggested by the proposed topology is seven and the higher levels can be arithmetically progressed with a factor of 6. Hence, the specific voltage levels cannot be generated by the suggested topology and its application is limited.

The other variant in MLI configuration based on hybridisation of transistor clamped topologies with Hexagon Switch Cell (HSC – H-bridge inverter with six switches) is presented in [24] in terms of symmetric and asymmetrical topologies. If the transistor clamping is on one side of HSC, then it is symmetric, otherwise it is asymmetric. The blocking voltages of clamping transistors are different and have voltage-balancing problem.

The symmetric topology suggested in [25], is suitable only for even number of 'n' isolated DC sources and the minimum number of DC sources should be 4. The other new topology identified in [26] composed of a module comprising two DC sources with two bi-directional and unidirectional devices for level generation and H-bridge inverter for polarity reversal. This topology requires more number of switches and gate drivers for increase in number of levels. A new MLI cell [27] comprising three DC sources and five devices designed to generate staircase waveform is capable of generating all levels, including odd/even just by cascading several cells. In recent years, more innovations emerging on topologies based on relocation of DC sources, introducing modular-based level generation cells and reconfiguring classical topologies tailored with innovative circuits [28–30]. In this perspective, more innovation is still required for MLI family and invites more avenues to focus the challenges to extract sinusoidal voltage/current waveforms by using lesser number of power components.

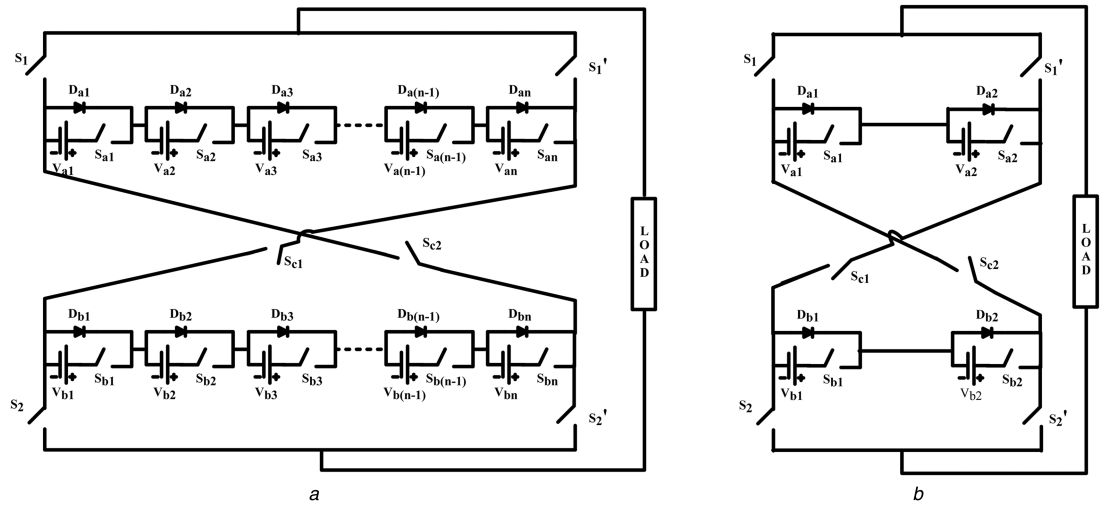


Fig. 1 *Generalised proposed topology and its configuration for nine-level inverter*
(a) Generalised proposed topology, ***(b)*** Proposed topology configured for nine level

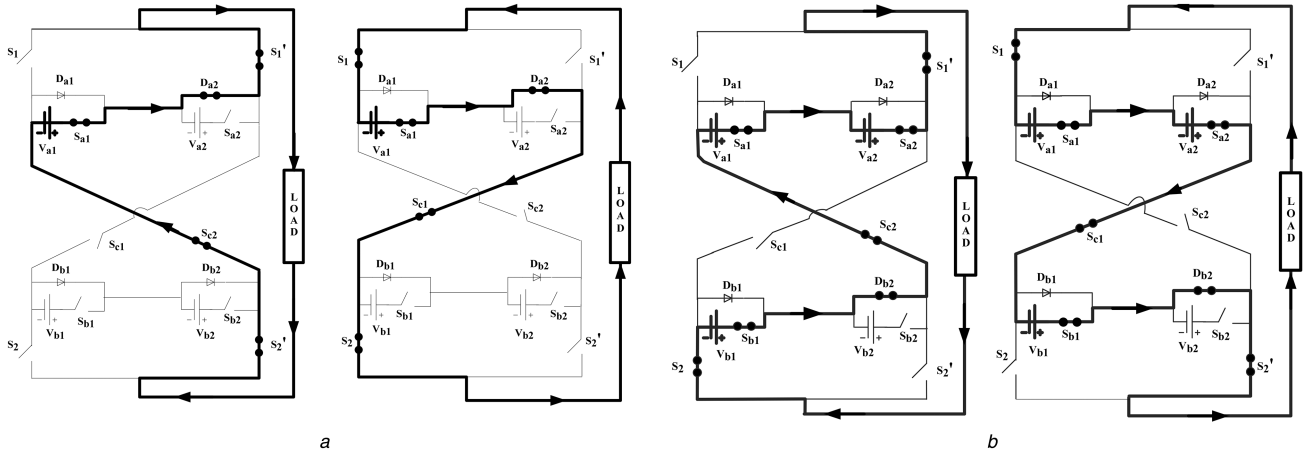


Fig. 2 *Operating mode of proposed nine level*
(a) Operating mode-level 1 ($\pm V_{a1}$), ***(b)*** Operating mode-level 3 ($\pm(V_{a1} + V_{a2} + V_{b1})$)

This paper describes the generalised structure of the proposed MLI along with multicarrier phase disposition (PD) PWM to generate any number of desired voltage levels. The proposed MLI simulation and experimental results with its extended version are presented.

2 Proposed topology

The development of new MLI topology allows sharing the voltage stress among the switches through a series connection of semi-half-bridge cells intertwined with crisscross switches. Fig. 1*a* portrays the general structure of the novel MLI topology constituted by a string of voltage sources (V_{a1}–V_{an}) and (V_{b1} – V_{bn}) connected in crisscross fashion through switches S_{c1}–S_{c2}. The switches (S_{a1}–S_{an}) and (S_{b1}–S_{bn}) connect the voltage sources in series, while the diodes (D_{a1}–D_{an}) and (D_{b1}–D_{bn}) bypass the voltage sources from the load. The switches (S_1, S_2) complementary to the switches (S'_1, S'_2) are arranged like H-bridge inverter. In the proposed topology, the required number of levels in the output voltage and the corresponding switches is given by the expression $((4 \times n) + 1)$ and $((2 \times n) + 6)$, respectively, where 'n' is the number of voltage sources per string. Voltage sharing is achieved in every conduction path due to the switching sequence and thus the blocking voltage is reduced.

Fig. 1*b* depicts the structure of nine-level inverter using four semi-half-bridge cells: two in upper and lower strings, respectively. By connecting only a few basic cells in series, this methodology can generate a minimum step voltage required for any given level. The structure of the DC-link can be obtained from a fixed DC source or from any other renewable energy sources such as solar cells, fuel cells, etc. The level 1 ($\pm V_{a1}$) and level 3 ($\pm(V_{a1} + V_{a2} + V_{b1})$) operating modes for each half-cycle with equal voltage sources for symmetrical configuration are illustrated in Figs. 2*a* and *b*. In Figs. 2*a* and *b*, the switches (S_{a1}, D_{a2}, S'_1, S'_2, S_{c2}) and (S_{a1}, D_{a2}, S_{c1}, S_2, S_1), (S_{a1}, S_{a2}, S'_1, S_2, S_{b1}, D_{b2}, S_{c2}) and (S_{a1}, S_{a2}, S_{c1}, S_{b1}, D_{b2}, S'_2, S_1) are switched to produce ($\pm V_{a1}$ and $\pm(V_{a1} + V_{a2} + V_{b1})$), respectively. The procedure follows the similar switching sequence to extract other voltage levels.

The number of switching devices in the conduction path determines the efficiency of the proposed topology. The conventional nine-level CHBMLI topology requires 16 switches and at any point of time, with half of the switches conducting, whereas in the presented topology the number of switches is always less for any level. Table 1 shows the power components comparison of the proposed and classical topologies in terms of 'm', where 'm' is the number of output levels.

The proposed MLI in asymmetrical configuration is realised by choosing the voltage ratio either in a binary ratio or factor of 2. The structure shown in Fig. 1*b* is configured to operate at 15 levels in binary ratio. The number of voltage sources and switches required is four and ten. The corresponding magnitudes of voltage sources is $V_{a1} = V_{\text{dc}}$ and $V_{a2} = V_{b1} = V_{b2} = 2\ V_{\text{dc}}$. The level $\pm(V_{a1} + V_{a2})$ is observed by switching the devices (S_{a1}, S_{a2}, S'_1, S'_2, S_{c2}) and (S_{a1}, S_{a2}, S_{c1}, S_2, S_1). The logical operation tabulated in Table 4 follows the similar pattern as used in symmetrical configuration with seven carriers and two reference signals for positive/negative pulse generation.

An extended basic sub-MLI topology in Fig. 3 from proposed MLI of Fig. 1*a* is composed of three voltage sources ($V_{a1,1}$, $V_{a2,1}$

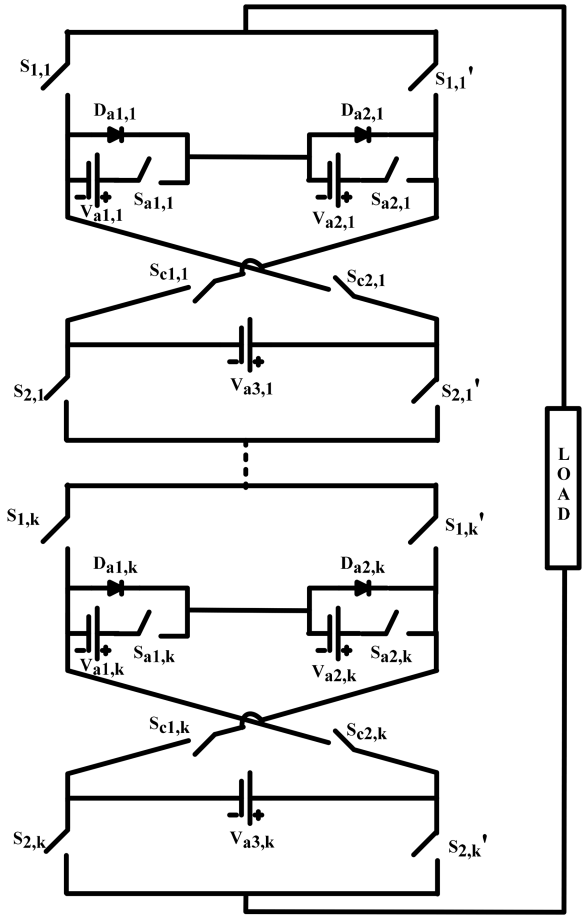


Fig. 3 *Proposed Sub MLI string (extended topology)*

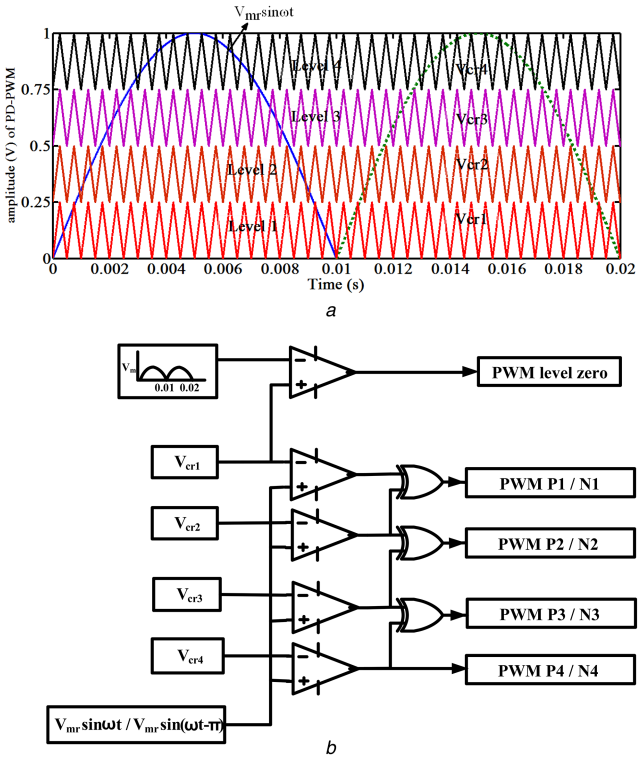


Fig. 4 *Modulation schematic for the nine-level inverter*
(a) PD-PWM scheme, ***(b)*** Analogue circuitry for base PWM generation

and $V_{a3,1}$) with eight switches. This innovative structure allows producing any possible values of minimum step voltage by using fewer number of basic subinverter cells. The main advantage of this topology is minimum number of switching devices with reduced blocking voltage for a given number of levels. For the extended topology, the relation between the DC sources (n) and the subinverters (k) required for any number of levels is shown in Table 2.

Table 1 Power components comparison – proposed topology and conventional topologies

components of MLI structure	Proposed MLI	MLI with clamping diodes/ flying capacitors	CHBMLI
semi-conductor devices: main switches	$(m+11)/2$	$2(m-1)$	$2(m-1)$
bypass diodes	$(m-1)/2$	—	—
capacitors: DC split/ flying	—	$((m-1)/2)/(m-2)$	—
DC voltage sources	$(m-1)/2$	1	$(m-1)/2$

Table 2 Relation between DC voltage sources (n) and basic units (k) in the extended inverter ($n = 3 \times k$)

Quantity	Symmetric structure	Asymmetric structure (1 : 2)
maximum output voltage	$3 \times k \times V_{dc}$	$5 \times k \times V_{dc}$
number of output voltage levels	$[(6 \times k) + 1]$	$[(10 \times k) + 1]$
number of isolated DC voltage sources	$(3 \times k)$	$(3 \times k)$
number of gate drivers-switches	$(8 \times k)$	$(8 \times k)$
standing voltages across the switches in the extended topology	$3 \times V_{dc}$	$5 \times V_{dc}$

The proposed topology illustrated in Fig. 1*b* utilises PD-PWM for producing nine-level output in symmetrical configuration due to its simplicity. It involves four triangular carriers and two reference signals (sine wave) for PWM generation and the corresponding analogue circuitry for base PWM generation for each level as portrayed in Fig. 4. Table 3 details the logical operation for PWM generation to extract various levels of output voltage. Similarly the same concept is extended for asymmetrical configuration for Fig. 2 is illustrated in Table 4.

3 Power loss analysis

The power loss [20, 26] of switching device is equal to the sum of conduction and switching losses. The other types of losses namely gate losses and off-state losses are very small and neglected. The conduction loss (P_{cond}) that occurs during on state of a switching device, while carrying current is computed by using the following equations [24, 28]:

$$P_{\text{cond},x}(t) = V_{\text{on},x}(t) \cdot I(t) \tag{1}$$

where 'x' is the semi-conductor device, $V_{on}(t)$ is the on-state voltage drop of 'x', $I(t)$ is the current flowing through 'x'. The loss during conduction on these devices is obtained by (2) and (3)

$$P_{\text{cond},G}(t) = \left[V_{\text{on},G}(t) + R_G \cdot I^{\beta}(t)\right] \cdot I(t) \tag{2}$$

$$P_{\text{cond},D}(t) = \left[V_{\text{on},D}(t) + R_D \cdot I(t)\right] \cdot I(t) \tag{3}$$

where, 'G' is IGBT (IRG4BC20UBF), 'D' is ultra-fast acting diode (BYQ28E) and 'β' is a constant depending on the specification of transistor. The conduction loss for each device over a fundamental cycle that depends on current conduction path is calculated using the following (4) and (5):

$$P_{\text{cond},G} = \frac{1}{2\pi}\int_0^{2\pi} P_{\text{cond},G}(t)\mathrm{d}\omega t \tag{4}$$

$$P_{\text{cond},D} = \frac{1}{2\pi}\int_0^{2\pi} P_{\text{cond},D}(t)\mathrm{d}\omega t \tag{5}$$

$I(t)$ is assumed to be sinusoidal. Similar procedure is followed to determine the switching loss (P_{sw}) of each semi-conductor device, which is equal to the power dissipated during turn-on (t_{on}) and turn-off (t_{off}) time and it is given in (6)

$$P_{\text{sw}} = \frac{1}{T}\sum(E_{\text{on}} + E_{\text{off}} + E_{\text{rec}}) \tag{6}$$

where, 'T' is the fundamental period, E_{on} and E_{off} are the turn-on and turn-off energy loss of IGBT. E_{rec} is the turn-off energy loss of diode and the diode turn-on loss is normally neglected due to the fast action during forward bias condition as it is <1% compared with E_{rec}. Using linear approximation of the switching voltage and current characteristics of the semi-conductor device presented in [31], the energy loss during the turn-on period is as follows:

$$E_{\text{on}} = \int_0^{t_{\text{on}}} v(t)i(t)\mathrm{d}t \tag{7}$$

Table 3 Logical mapping for each device to extract various levels for nine-level inverter

Base PWM	Output level	Logical mapping of positive level	Logical mapping of negative level
PWM level zero	zero level	S_1, S_{c2}, S'_2/S'_1, S_{c1}, S_2	S_1, S_{c2}, S'_2/S'_1, S_{c1}, S_2
PWM P1/N1	$\pm V_{a1}$	S_{a1}, S'_1, S'_2, S_{c2}	S_{a1}, S_{c1}, S_2, S_1
PWM P2/N2	$\pm(V_{a1} + V_{a2})$	S_{a1}, S_{a2}, S'_1, S'_2, S_{c2}	S_{a1}, S_{a2}, S_{c1}, S_2, S_1
PWM P3/N3	$\pm(V_{a1} + V_{a2} + V_{b1})$	S_{a1}, S_{a2}, S'_1, S_2, S_{b1}, S_{c2}	S_{a1}, S_{a2}, S_{c1}, S_{b1}, S'_2, S_1
PWM P4/N4	$\pm(V_{a1} + V_{a2} + V_{b1} + V_{b2})$	S_{a1}, S_{a2}, S'_1, S_2, S_{b1}, S_{b2}, S_{c2}	S_{a1}, S_{a2}, S_{c1}, S_{b1}, S_{b2}, S'_2, S_1

Table 4 Logical mapping for each device to extract various levels for 15-level inverter

Base PWM	Output level	Logical mapping of positive level	Logical mapping of negative level
PWM level zero	zero level	S_1, S_{c2}, S'_2/S'_1, S_{c1}, S_2	S_1, S_{c2}, S'_2/S'_1, S_{c1}, S_2
PWM P1/N1	$\pm V_{a1}$	S_{a1}, S'_1, S'_2, S_{c2}	S_{a1}, S_{c1}, S_2, S_1
PWM P2/N2	$\pm(V_{a2})$	S_{a2}, S'_1, S'_2, S_{c2}	S_{a2}, S_{c1}, S_2, S_1
PWM P3/N3	$\pm(V_{a1} + V_{a2})$	S_{a1}, S_{a2}, S'_1, S'_2, S_{c2}	S_{a1}, S_{a2}, S_{c1}, S_2, S_1
PWM P4/N4	$\pm(V_{a2} + V_{b1})$	S_{a2}, S'_1, S_2, S_{b1}, S_{c2}	S_{a2}, S_{c1}, S_{b1}, S'_2, S_1
PWM P5/N5	$\pm(V_{a1} + V_{a2} + V_{b1})$	S_{a1}, S_{a2}, S'_1, S_2, S_{b1}, S_{c2}	S_{a1}, S_{a2}, S_{c1}, S_{b1}, S'_2, S_1
PWM P6/N6	$\pm(V_{a2} + V_{b1} + V_{b2})$	S_{a2}, S'_1, S_2, S_{b1}, S_{b2}, S_{c2}	S_{a2}, S_{c1}, S_{b1}, S_{b2}, S'_2, S_1
PWM P7/N7	$\pm(V_{a1} + V_{a2} + V_{b1} + V_{b2})$	S_{a1}, S_{a2}, S'_1, S_2, S_{b1}, S_{b2}, S_{c2}	S_{a1}, S_{a2}, S_{c1}, S_{b1}, S_{b2}, S'_2, S_1

$$\begin{aligned} &= \int_0^{t_{\text{on}}} \left(\frac{V_{\text{sw}}}{t_{\text{on}}}t\right)\left(-\frac{I}{t_{\text{on}}}(t - t_{\text{on}})\right)\mathrm{d}t \\ &= \frac{1}{6}V_{\text{sw}}It_{\text{on}} \end{aligned} \tag{8}$$

$$\text{Similarly } E_{\text{off}} = \frac{1}{6}V_{\text{sw}}It_{\text{off}} \tag{9}$$

where, V_{sw} and I are the off-state voltage of semi-conductor device and the current through the semi-conductor devices, respectively. The switching loss and conduction loss of the nine-level inverter are calculated for the parameters: ($V_{a1} = V_{a2} = V_{b1} = V_{b2} = 75$ V, $R = 165\ \Omega$, $L = 20$ mH and switching frequency is 2 kHz) and it is presented as chart in Fig. 5. Fig. 5 depicts the comparison of switching and conduction loss between PWM with and without pulse swapping. The switching loss/conduction loss of each device in the voltage string is equal as seen from Fig. 5*a* or Fig. 5*b* and the scheme [30] through which the PWM is circulated extradites to balance the losses among the power cells.

4 Selection of power devices

The blocking voltages being asymmetric across the switches in the proposed MLI however facilitate a lower number of switching devices in the conduction path compared with the CHBMLI. The blocking voltage across the devices during off-state experiences different off-state voltages in accordance with the magnitude of voltage sources due to different switching states. The blocking voltage of the switches (S_{a1}–S_{an}) and (S_{b1}–S_{bn}) during off state are (V_{Sa1}–V_{San}) and (V_{Sb1}–V_{Sbn}). The forward blocking voltage of the devices in each cell is obtained by

$$V_{San} = V_{an} \tag{10}$$

$$V_{Sbn} = V_{bn} \tag{11}$$

Similarly the blocking voltage of the fast acting diodes is

$$V_{Dan} = V_{an} \tag{12}$$

$$V_{Dbn} = V_{bn} \tag{13}$$

where (V_{Dan}–V_{Dbn}) are the blocking voltage of the diodes (D_{an}–D_{bn}).

Similar procedure is followed to find the blocking voltage (V_{S1}–V'_{S1}) of the top switches (S_1–S'_1) and blocking voltage (V_{S2}–V'_{S2}) of the bottom switches (S_2–S'_2) and the relation is given by

$$V_{S1} = V'_{S1} = \sum_{j=1}^{n} V_{aj} \tag{14}$$

$$V_{S2} = V'_{S2} = \sum_{j=1}^{n} V_{bj} \tag{15}$$

The forward blocking voltages of the crisscross switches (S_{c1}–S_{c2}) are (V_{Sc1}–V_{Sc2}) and it is calculated by the following equation:

$$V_{Sc1} = V_{Sc2} = \sum_{j=1}^{n} (V_{aj} + V_{bj})\,. \tag{16}$$

The blocking voltage of the crisscross switches used for reversal of polarity has to block the full DC-link voltage. Therefore it is concluded that the proposed inverter requires power devices of different voltage rating, which is mainly dependent on the selection of voltage sources. However, the proposed inverter carries the advantage over the conventional MLI that the standing voltage of the switches switched at the high frequency is low and that the

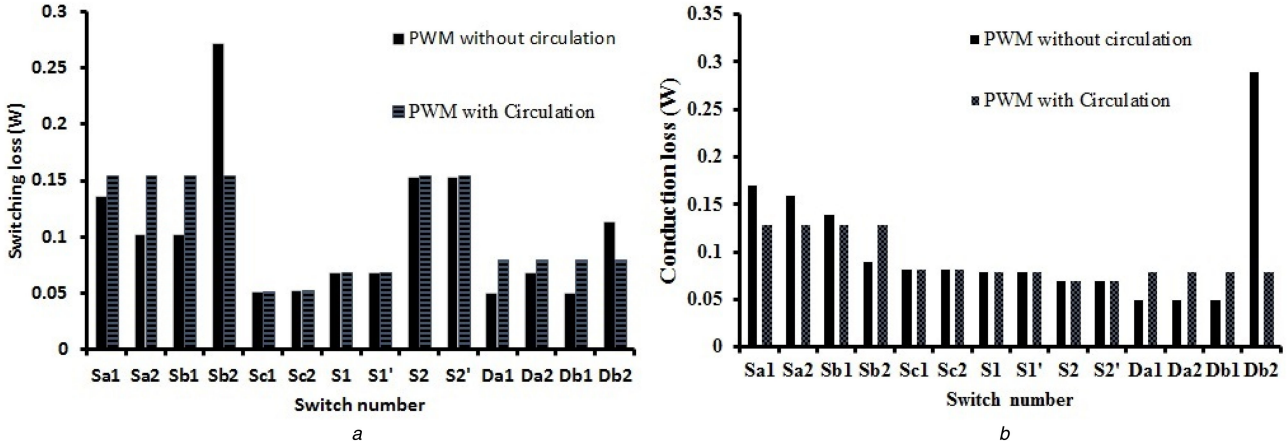


Fig. 5 *Semi-conductor losses for the nine-level inverter*
(a) Switching loss, ***(b)*** Conduction loss

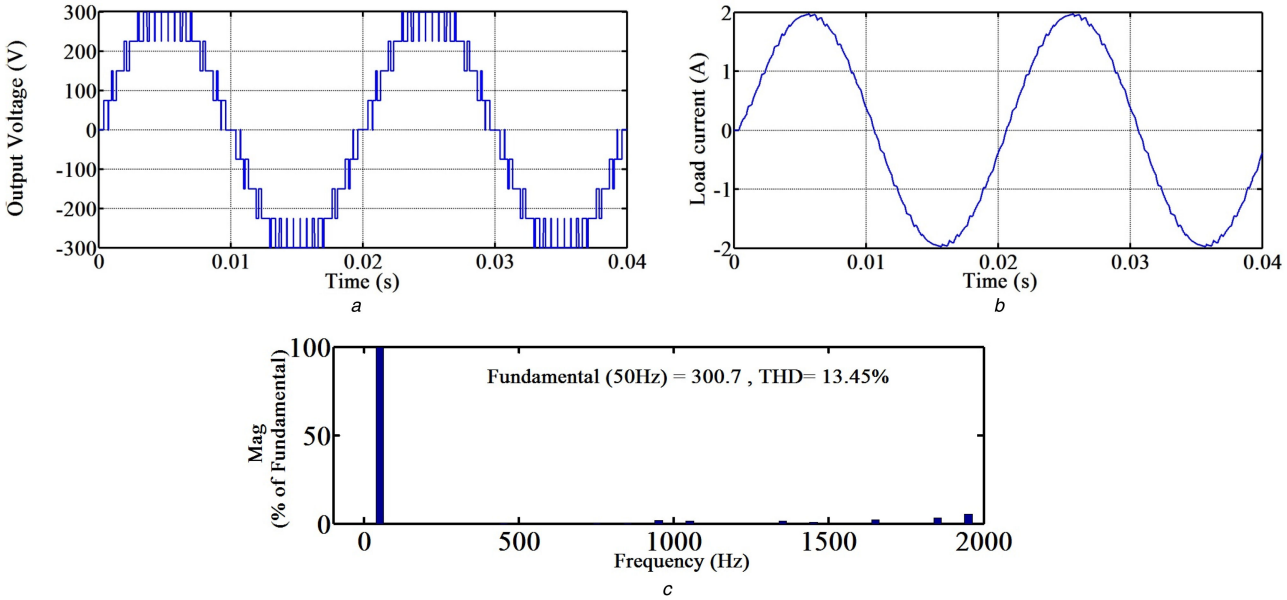


Fig. 6 *Simulation results of the proposed symmetric nine-level inverter for m_i = 1, load parameters(R = 150 Ω, L = 100 mH) and without PWM circulation*
(a) Output voltage, ***(b)*** Inductive load current waveform, ***(c)*** Output voltage spectrum

switching frequency of the switches with the high voltage stress is low.

5 Simulation results

The functionality of the proposed topologies is tested in MATLAB/SIMULINK R2013b version. The simulation parameters: ($V_{a1} = V_{a2} = V_{b1} = V_{b2} = 75$ V) under symmetrical mode ($V_{a1} = 42$ V; $V_{a2} = V_{b1} = V_{b2} = 86$ V) under asymmetrical mode for the basic topology seen in Fig. 1*b* ($V_{a1,1} = V_{a2,1} = V_{a3,1} = V_{a1,2} = V_{a2,2} = V_{a3,2} = 50$ V) for extended topology depicted in Fig. 3 under symmetrical mode and also for the same seen in Fig. 3 ($V_{a1,1} = 30$ V, $V_{a2,1} = V_{a3,1} = 60$ V, $V_{a1,2} = 30$ V, $V_{a2,2} = V_{a3,2} = 60$ V) under asymmetrical mode. Multicarrier PD-PWM method is used and the devices are switched at 2 kHz. A simulation study has been carried out with different load conditions to validate the simulated response of Fig. 1*a* under wide range of modulation indices for symmetrical case at different load conditions. Fig. 1*a* configured to obtain nine-level output is simulated for two different load conditions. For highly inductive load ($R = 150$ Ω, $L = 100$ mH), the voltage waveform along with harmonic spectrum and current waveform is depicted in Fig. 6. From Fig. 6*b*, it is evident that the load current is almost sinusoidal. The same circuit is simulated for the other load ($R = 165$ Ω, $L = 20$ mH) and the pulses are generated based on pulse swapping among the switches in the voltage string. Due to pulse swapping, the current drawn from each source remain engaged in alternate full cycles of the output waveform and balancing is accomplished in four cycles. It follows that, for equal load sharing, each source contributes for synthesising the output voltage levels alternately as shown in Fig. 7. The voltage waveform of Fig. 8*a* synthesised using PWM swapping is identical with voltage waveform of Fig. 6*a*, which is synthesised without PWM swapping and the total harmonic distortion (THD) is also equal. From Table 5, it is inferred that the power drawn from each source are equal and balanced. Another simulation case is performed for the same circuit configuration for different modulation indices (0.4 and 0.6) and the corresponding voltage THD are tabulated in Table 6. From Table 6, it is clear that, as the modulation index decreases, the number of voltage levels synthesised at the output decreases, consequently the THD increases. The proposed topology of Fig. 1*b* is simulated under asymmetrical mode with binary voltage ratio, and by using the switching sequence presented in Table 4, 15-level output voltage THD is tabulated in Table 6. Fig. 9 portrays the output voltage and its corresponding spectrum for the extended structure of proposed topology seen in Fig. 3 under symmetrical case (13-level) and asymmetrical case (21-level) with ($k = 2$), respectively.

6 Experimental results

The prototype of the proposed topology and extended topology was constructed, using IGBT (IRG4BC20UPBF) and fast acting recovery diodes (BYQ28E) with the same specifications as those

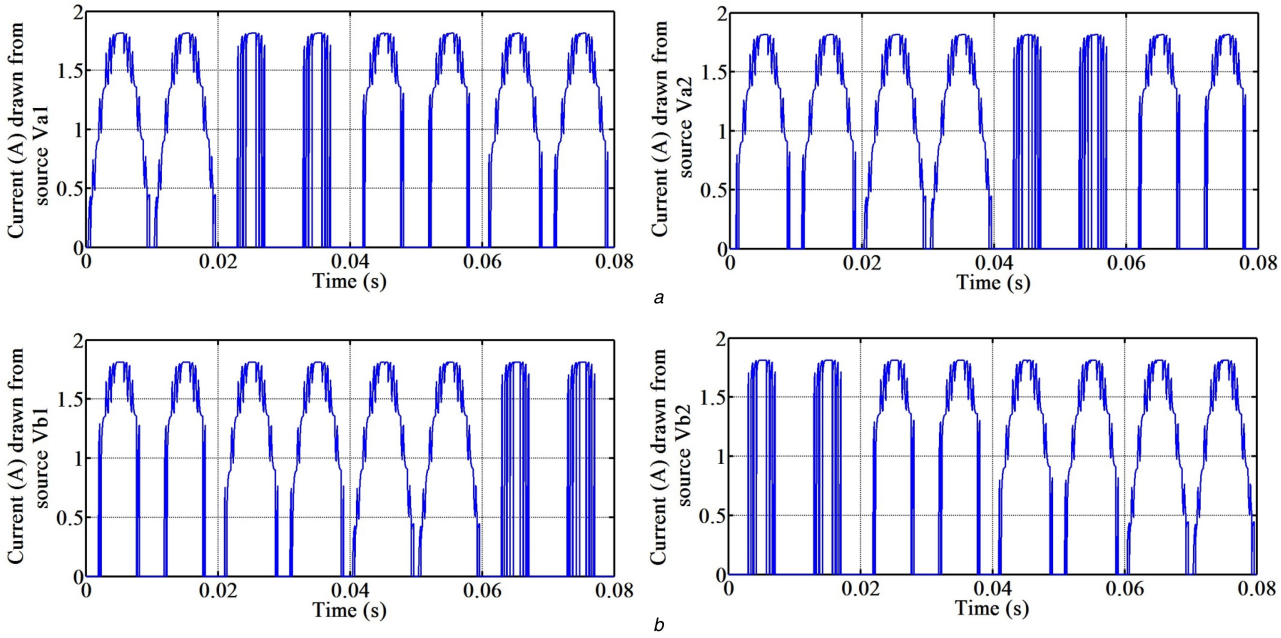


Fig. 7 *Simulation results of current drawn from each source for the proposed symmetric nine-level inverter for $m_i = 1$ and load parameters ($R = 165\ \Omega$, $L = 20$ mH) with PWM circulation*

(a) Current drawn from source (V_{a1}, V_{a2}), ***(b)*** Current drawn from source (V_{b1}, V_{b2})

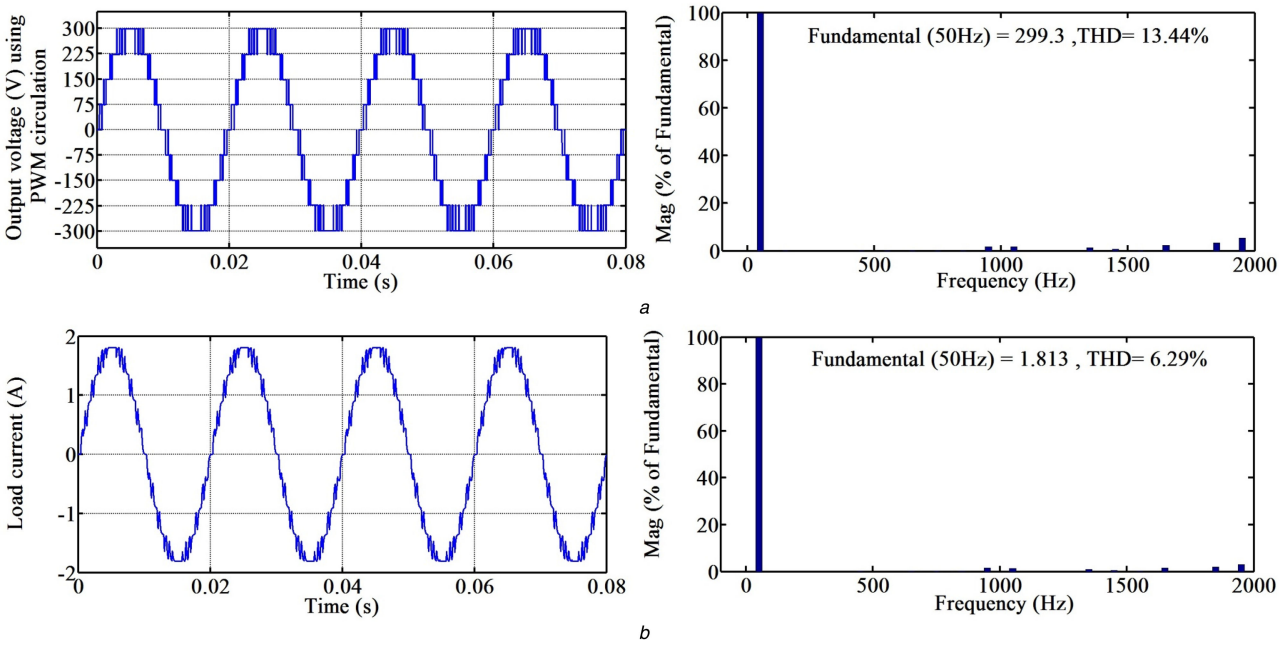


Fig. 8 *Simulation results of output voltage and current of the proposed symmetric nine-level inverter for $m_i = 1$ and load parameters ($R = 165\ \Omega$, $L = 20$ mH) with PWM circulation*

(a) Output voltage along with Harmonic spectrum, ***(b)*** Inductive load current waveform along with Harmonic spectrum

applied in simulation. The dSPACE controller DS1104 is used to generate gating pulses and the pulses are captured using Agilent MSOX3014A as portrayed in Figs. 11*a* and 13*a*. Two programmable DC power supplies available in the laboratory and the remaining isolated power supplies are constructed for configuring the different MLI structures. The voltage and current waveforms are captured using Tektronix TPS 2014 scope and Agilent DSO X 3014A scope. The experimental setup of Fig. 1*b* configured in symmetrical mode is shown in Fig. 10 and the corresponding results for different load conditions with $m_i = 1$, are depicted in Figs. 11–13. The performance of the proposed MLI configured for 15-level output is shown in Fig. 14*b* with voltage waveform. The experimental results of the extended topology under symmetric mode (13-level) and asymmetric mode (21-level) are portrayed in Figs. 14*a* and *c*. The results project the practicability of the proposed MLI structure in the MLI field.

7 Conclusions

A new MLI topology configured under symmetric and asymmetric structure is presented. The modularity of the topology is suitable to reach any desired voltage level with the advantage of lesser number of power components with reduced blocking voltage over the benchmarked conventional converters. Therefore, the control circuit complexity is reduced and the PWM scheme derived in terms of logic gates was comfortably employed. The prototype was fabricated and the hardware results of 9-level/13-level/15-level and 21-level inverter met the desired output and validated through the simulation results. The presented results project the practical viability of the proposed MLI topology in the field of renewable energy applications.

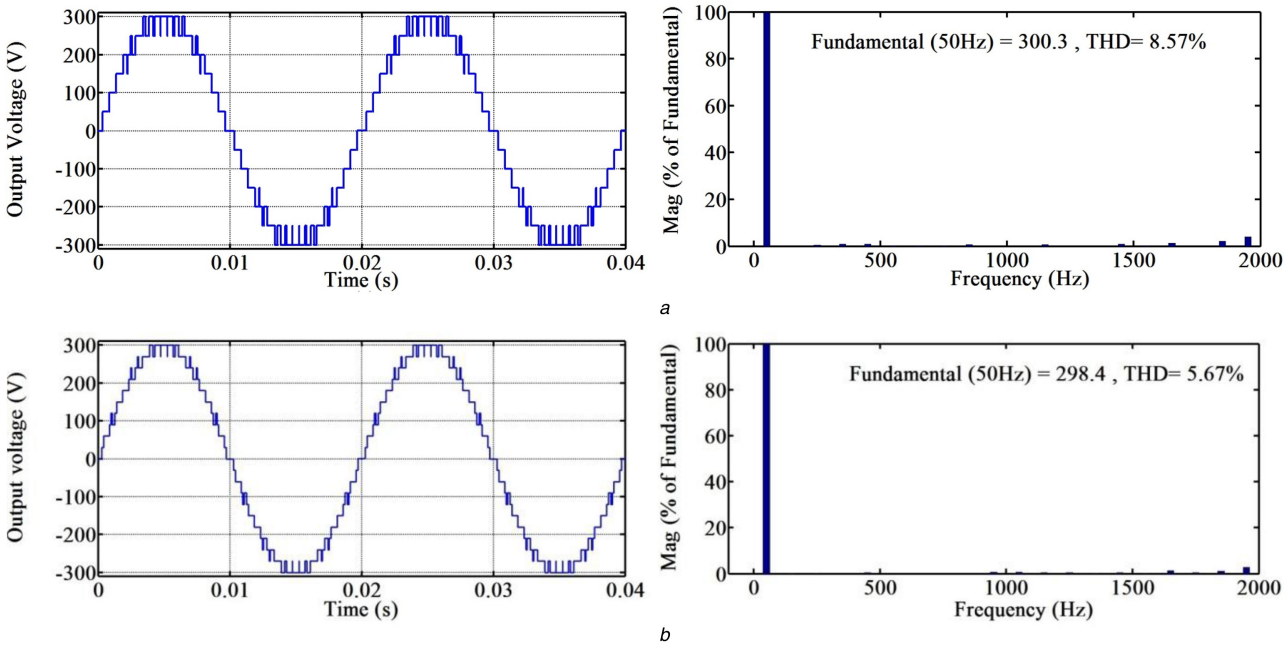


Fig. 9 *Output voltage waveform along with harmonic spectrum for the extended structure for $m_i = 1$*
(a) Symmetric 13-level inverter, ***(b)*** Asymmetric 21-level Inverter

Table 5 Power delivered by each source

Output power	Input power delivered by sources based on the PWM without circulation				Input power delivered by sources based on the PWM with circulation			
	V_{a1}	V_{a2}	V_{b1}	V_{b2}	V_{a1}	V_{a2}	V_{b1}	V_{b2}
271 W	86.02 W	80.77 W	67.77 W	40.684 W	68.81 W	68.81 W	68.81 W	68.81 W

Table 6 Proposed topology under different operating modes

MLI structure	Ratio of source voltage magnitudes	m_i	Voltage THD Magnitude (% of fundamental)	No. of voltage levels at the output, m
proposed topology	1:1	1	13.44	9
	1:1	0.6	24.21	7
	1:1	0.4	38.6	5
	1:2	1	7.8	15
extended topology	1:1	1	8.57	13
	1:2	1	5.67	21

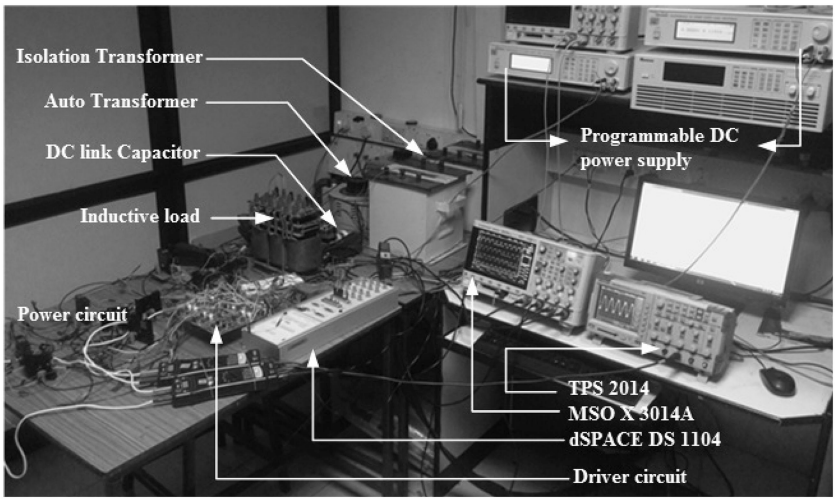
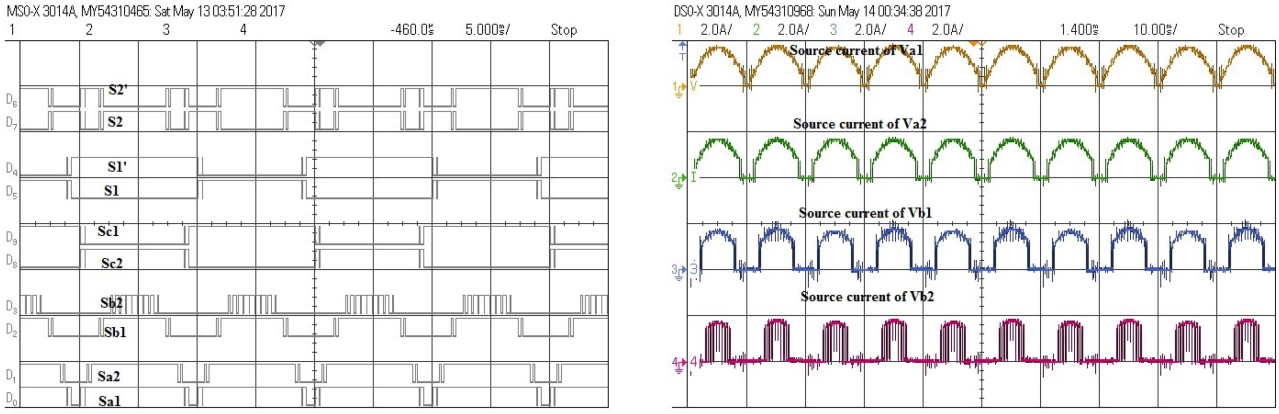


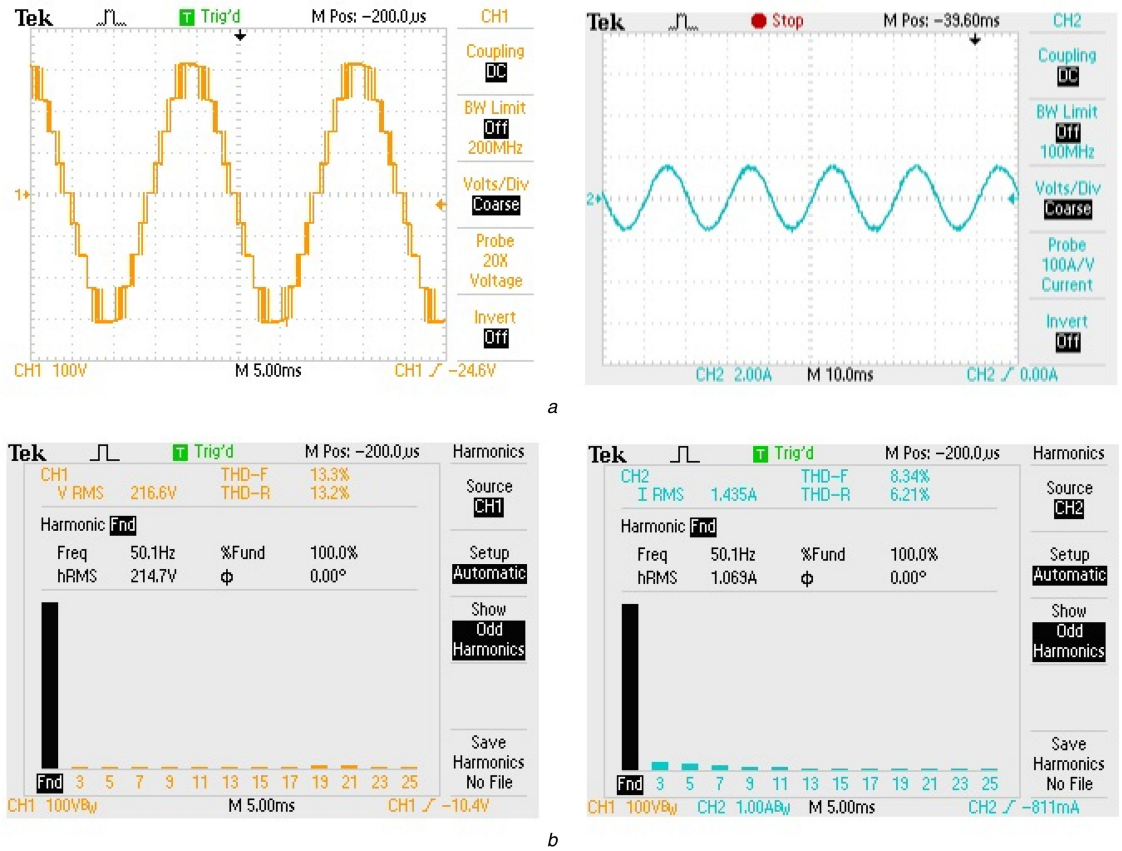
Fig. 10 *Photograph of the experimental setup*



a *b*

Fig. 11 *Gating signal and source current of the proposed symmetric nine-level inverter for $m_i = 1$, load ($R = 150\ \Omega$, $L = 100$ mH) and without PWM circulation*

(a) Gating pulses, ***(b)*** Current drawn from each source



a

b

Fig. 12 *Output voltage and load current of the proposed symmetric nine-level inverter for $m_i = 1$, inductive load ($R = 150\ \Omega$, $L = 100$ mH) and without PWM circulation*

(a) Output voltage and Inductive load current waveform, ***(b)*** Output voltage and inductive load current spectrum

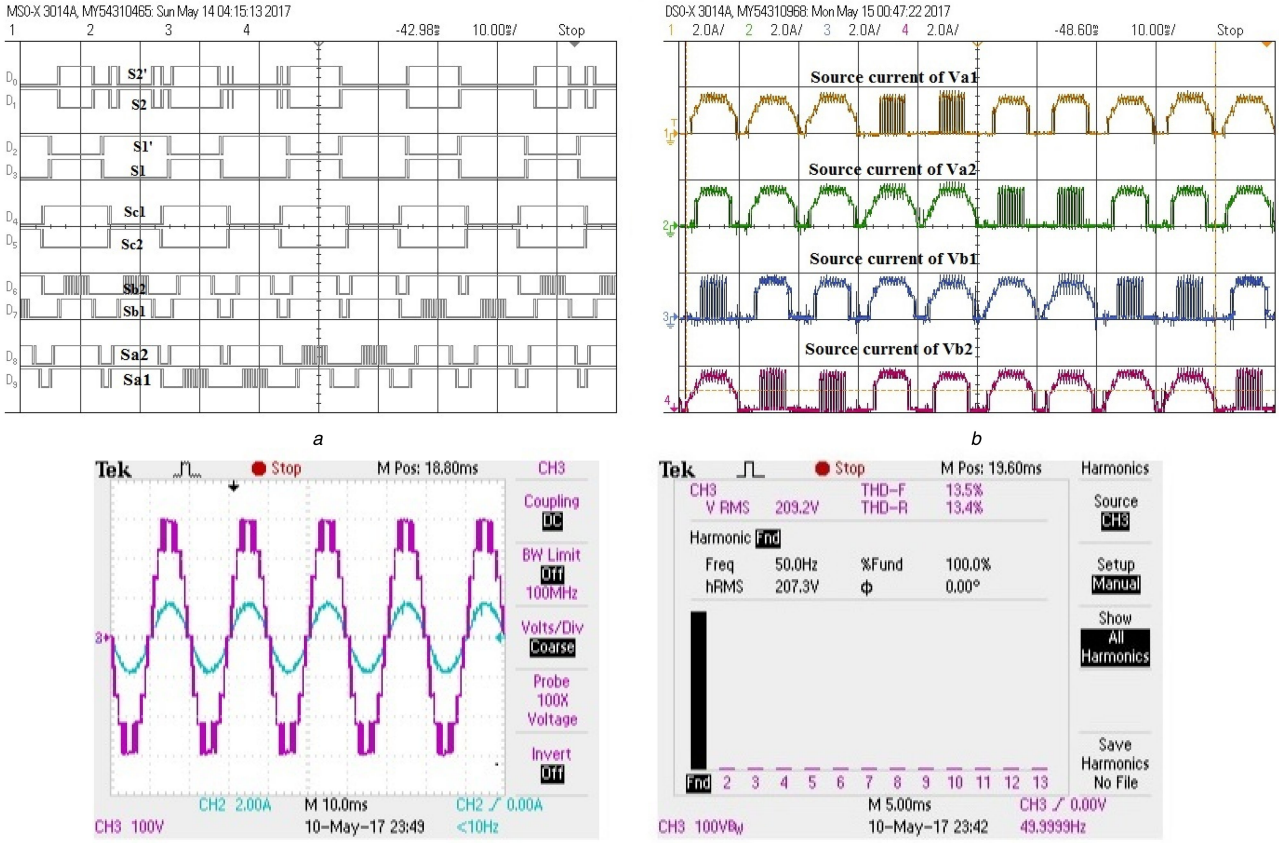


Fig. 13 *Experimental results of the proposed symmetric nine-level inverter for m_i = 1 and load parameters(R = 165 Ω, L = 20 mH) with PWM circulation*
(a) Gating pulses, ***(b)*** Current drawn from each source, ***(c)*** Output voltage and load current waveform, ***(d)*** Output voltage spectrum

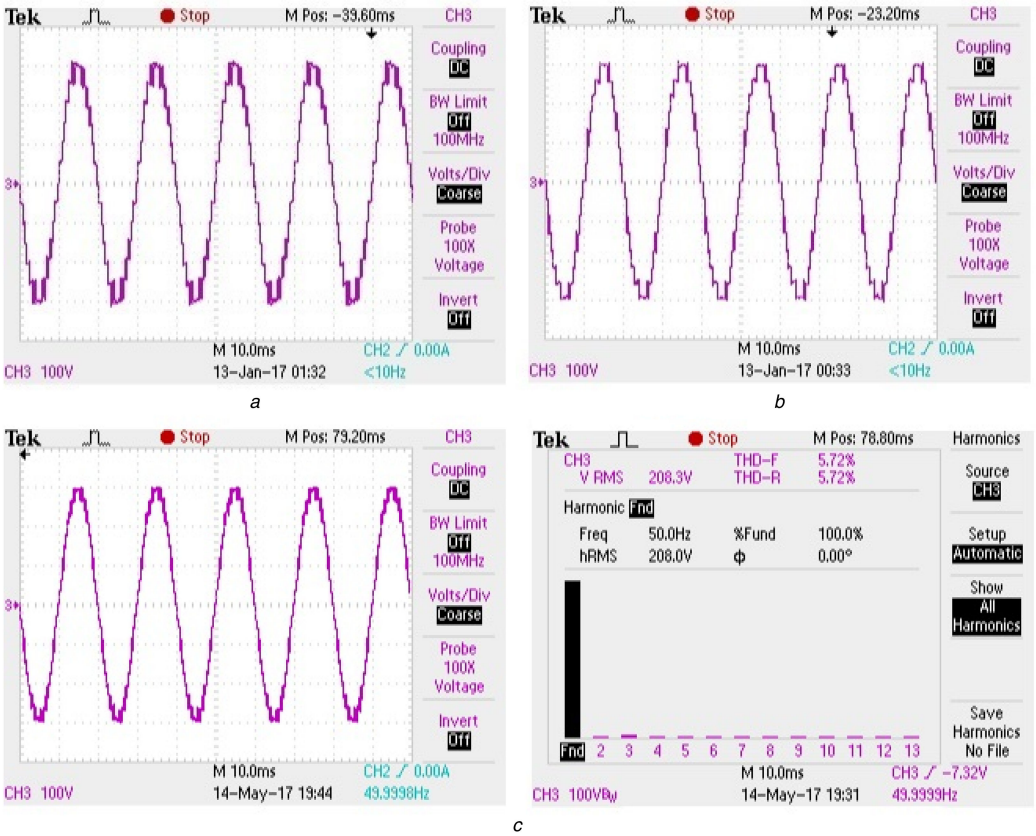


Fig. 14 *Output voltage waveform of proposed and extended topology with different source voltage ratio for m_i = 1*
(a) 13-level MLI of extended topology in symmetric mode (1:1), ***(b)*** 15-level MLI of proposed topology in asymmetric mode (1:2), ***(c)*** 21-level MLI of extended topology in asymmetric mode (1:2) with voltage spectrum

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