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Design and Implementation of 16bit SRAM Using Quantum Dot Cellular Automata

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Design and Implementation of 16bit SRAM Using Quantum Dot Cellular Automata

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Abstract—The era of CMOS technology at the nanoscale will be going to replace with an unimaginable future by the opportunity of Quantum-dot cellular automata (QCA). The largest possible scope for constructing an elegant and efficient memory design is there with QCA technology. The suggested methodology and execution of a brand-new reminiscence cell shape primarily depends on QCA with a minimum delay, area, and complications is provided to develop a static random-access memory. This paper affords the circuit diagram and its execution of a 16-bit Static RAM with a new shape in QCA. Because of having powerful pipelining structure with in the QCA, this SRAM is very fast in executing operations. With a new shape of 4-bit width design for the 16-bit SRAM has applied in QCA. The ability of resulting read/write operations often with minimal delay is possible with this kind of SRAM design. Having a smaller number of majority gates and cells, the design of 16-bit decoders and multiplexers are represented. For getting rid from the adjoining hassle of intersecting labels, the new signal distribution network has been used to implement the SRAM with 2-to-4 decoders and 4-to-1 mux's. The Quantum do CA-primarily depend on Static RAM cell turned into comparison with the Static RAM cell depended totally on CMOS. Consequences observed that the suggested Static RAM is more systematic in phrases of area, complexity, clock frequency, latency, throughput, and power in take.

1. Introduction

Digital calculation has got the new technology using quantum dots called quantum dot cellular automata. Information transmission with high speed and frequency along with low power and delay has been possible with QCA technology. Voltage source need not requires for the QCA; electron moment will give the logical values. QCA will dominates the era of CMOS technology. Rather, Complementary MOS circuit levels, the Quantum dot CA clocking is basically have been dissimilar from the information. Barriers between the dots can go for falls and raises with the help of clock that which makes the choice of forbidding and accepting the particles to jump in the middle of dots. The benefits of Quantum dot CA technology compared to Complementary MOS has the following:

1) fast operations; 2) less power dissipation; 3) large apparatus thickness. Even though the sizes of CMOS technology in future will get reduced, still they will have some kind of limitations. Because of this there will be a huge impact of molecular plans on nanoscale. One of the most interesting application of the QCA technology is Static random-access memory (SRAM). Its comparatively equivalent structure which suits to fabrication at the nanoscale. Parallel memories can also be implemented in QCA. Following with the tradeoff of the data along the lines of QCA cells, the architecture uses the proper slots in the memory cell. QCA memory clocking relies under the saving of different sections and complications are the things which are resulted by the architecture; for combining the circuits with the breadth of 1 bit, the resulted memory cells from the architecture be utilized. Those designs efforts inculcate area truncation and series memories to reduce clock cycle

latency in reading. Since the hybrid architecture design is conditional, so that to preserve different kinds of information as an information container for device breadth is 1 bit and is highly impossible. The utmost observation has been attentively given to the memory, the consequences till now were invigorating but the most of the work required based on the simple design of the ultimate suggested network. Based on the researches found, which were introduced in the year 1994, they use to condemn following close by adjoining planar cable intersections. The dumbness in that kind of wiring was observed from that time only, most particularly that consists of low elation power linking the zero position and the highest elated position which reduces opposition of constructional differences, heating problems, and capacitances. The best way to overcome that problem is to use newly established label intersections those which need not resembles the same problems. In this paper, for getting rid out of the planar hassle of intersecting labels, the new signal distribution network has been used to implement the SRAM with 2-to-4 decoders and 4-to-1 mux's. The SDN gives the solutions to the biggest problems which were addressed earlier according to the past studies are as such of wire crossing by depending completely on closest neighbor interchanges, which will improve the elation energy of the device, thermal behavior and stay strong for the constructional problems.

The area and delay of the Quantum dot CA-primarily depended Static RAM cell turned into comparison with the Static RAM cell based totally on CMOS. Consequences gives that the suggested Static RAM is more systematic in phrases of area, complexity, clock frequency, latency and power in take. Both in the read and write operations for 16-bit Static RAM cell considered with the less area designed by the QCA. It was possible by the help of 4-bit width to save data as a 4-bit data packet in the Static RAM. Primarily this paper has three things to focus: 1) less timing; 2) area and 3) low power consumption. With the help of our studies, executed designs circuits through QCA Designer and consequences for particles utilized in QCA Designer. Overflow for this script is planned accordingly. Second part consists of analysis of networks and dots, polarization, magnetization and clock techniques of quantum dot cellular automata. Design for 4-to-16 decoder and 16-to-1 for the 512bit static RAM memory cells are explained in third part. The suggested quantum dots 2-to-4 decoder and 4-to-1 mux along with memory cell to design a 16-bit Static RAM is represented fourth part. Fifth part gives the simulation results of proposed 16-bit Static RAM. comparison table for results obtained from QCA based 16-bit SRAM cell to the CMOS based 16-bit SRAM memory cell is discussed in section VI. Sixth part consists of the epilogue.

2. Back drop of quantum dot cells

2.1. Analysis

Four quantum dots are get placed at its corners with a square shaped in a QCA cell. In each and every cell there are two electrons in which they try to tunnel between the two quantum dots, but in return as a result they are not supposed to tunnel from the quantum dots. Because of strong columbic attractions those two electrons are placed in opposite corners to face the largest distance among themselves. The placing of electron on the right-hand side crossed diagonal shows binary 1 and on the other side shows binary 0. There are four types of QCA implementation: 1) metal-island; 2) semiconductor; 3) molecular; and 4) magnetic. First fabrication technology which was developed to explain about the concept of QCA was metal-island. It was not even that much good when compared with present technology to compete in the terms of speed and practicality, as its structural properties are not suitable for scalable designs. That was a method which was proposed to build accordingly the quantum dots using aluminum islands. The performed experiments were dealt with metal islands as big as 1 µm in dimension. Metal-island devices must be kept at very low temperatures for quantum effects to be observable, since they are comparatively large sized islands. Very highly advanced Semiconductor fabrication processes are used to design both QCA and CMOS designs equally powerful. Cell polarization is fixed as charge position, and quantum-dot interactions depends on electrostatic coupling. Mass production of devices has not entered in to a scenario in which they can generate devices with less area. QCA solid state execution can be possible only through Serial lithographic methods. A method which was not executed till the moment to be implemented, has the

chance of constructing apparatus of individual atoms. The anticipated improvements of that methodology have: 1) symmetrical design of dot cell; 2) powerful fluctuating capacity; 3) large apparatus thickness 4) maintaining normal heat; and 5) Mass production devices can be achieved by the help of self-assembly. Study of interaction between magnetic nanoparticles is normally referred as magnetic QCA which is also called as MQCA. Polarization vector in all other executions is similar to the alluring direction of these tiny substances. The term quantum gives the meaning of quantal mechatronic behavior of magnetization interchanges which are never belongs to the elemental jumping phenomenon. The constructed devices in this way will operate at room temperature. The clock frequency which was used to get simulation results for semiconductor QCA is 1GHz and for the molecular method which was going to be implement soon in the future will uses the frequency of 1THz to get the simulation results. The high encouraging executions suggested in this writing depends on tiny magnetics and on atoms. Figure 1 shows the QCA layout of three input majority gates with inputs A, B and C which is useful to build many AND gates, decoders, mux's as a basic building block. Figure 2 Shows that the QCA layout of the inverter cell. Atomic structure with lots of central zones are physically implemented by the QCA cell; electrostatic repulsion along with the charge configuration inside a molecule gives the logical state and invokes device–device interaction. High frequencies (terahertz) and exceptional compactness are anticipated by the molecular implementation.
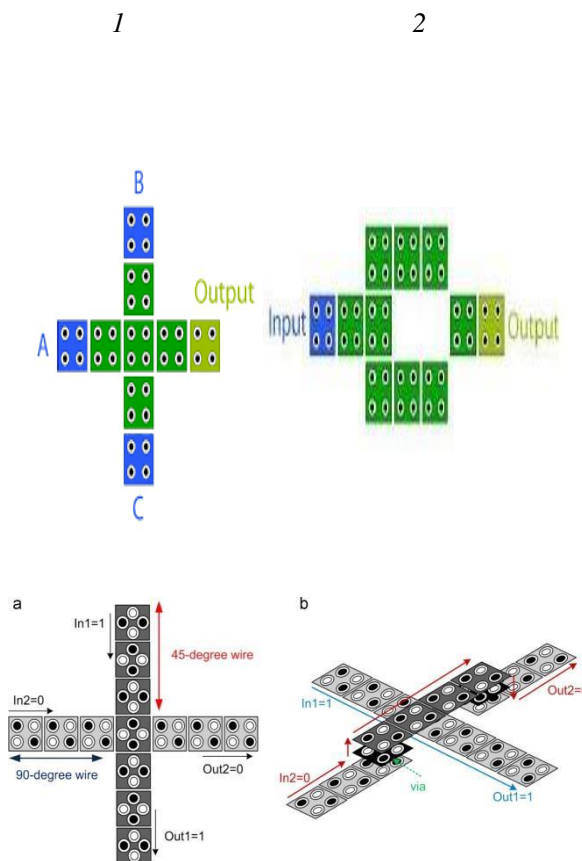
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Figure 1. 1. Majority gate, 2. Inverter gate, a. coplanar, b. multilayer wire crossings.

The desired output for molecular scale QCA was observed int his paper with in the presence of SRAM. The positioning of electrifying particles permits preserving and forwarding of details to molecular scale cellular dots. Logic 0 and logic 1 cables and not gates are the simplest circuits in the QCA technology, whose binary value is forwarded by columbic repulsion. The basic gate of the quantum dot CA is called as majority gate which is developed using 5 small cell shapes and its functionality is equals to (A X B) + (B X C) + (C X A). By the help of majority gates, we can

develop AND and OR gates with many numbers of inputs to them to implement. The other typical thing in QCA is crossing wires, they are of two types and so called as multilayer crossing wires. Cellular dots consist of different shapes those are helpful to execute all the internal connections. One of them is planar label intersections, and another thing is multiple layered intersections which are clearly observed in Figure a and Figure b. `

2.2 Cellular dot clock techniques:
Quantum dot cells has different stages of clocks: 1) switching stage; 2) holding stage; 3) releasing stage; and 4) relaxation stage (Figure 2). Initially in the switching period, the cells are not polarized and their potential obstructions are less. In that case, while in the switch phase computation will takes place after QCA cells got polarized and barriers became high. Obstructions are placed higher in the span of hold. QCA cells will get unpolarized and barriers become high at the period of release. Barriers remain low and the cells remain unpolarized during the phase of relax. The zero stage begins to interrelate by the higher stage only by time of clocking field is turned ON. Null states and active states will get strong coupling between them, only when the interchanges between the low power stages takes place. Molecular QCA cell switching behavior in a clock period is 1ps and clock frequency is hundred megahertz. Even then we can achieve more than this up to ~1 GHz. we are familiar with that the minute cell particles have the frequency of 1 THz; the problems come from molecular circuit fabrication and through the speed of the drive circuits will not arrives with this approach.
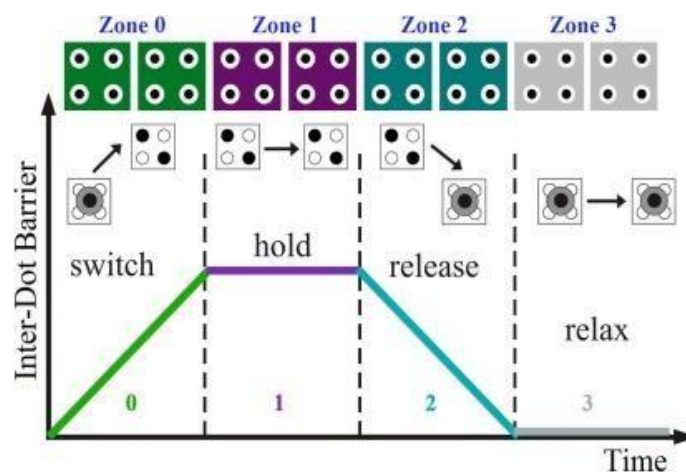

Figure 2. Clock stages of quantum dots

3 QCA DESIGN OF A DECODER AND MUX
This section presents the design of 4 x 16 decoder and 16 x 1 mux which are basic building blocks to the 16×32bit SRAM structure and their layouts in QCA.

3.1 4-to-16 decoder in QCA
Eight two input AND gates are been used in the stage to design the 4-to-16 decoder with four inputs interlinked to the wires of A, B, C, D. To get the proper accessing of output for 4-to-16 decoder uses eight two input AND gates again in the second stage. Figure 3 shows the schematic layout and its execution in QCA which gives the 16 outputs by using 4×4 two-input AND gate network. By the time EN pin is inactive (EN=0), all outputs are observed to be null. But when EN is active (EN = 1), the outputs show in connections to inputs A, B, C, and D. The designed 4-to-16 decoder consists of 1874 cells covering an area of 2.94 µm2 (1418.00 nm×2076 nm). The throughput is $Tr = O/Tb$, where O is the outputs, Tb is the period of a Bennett stage given by $Tb = 2Lb/M$, L b is the initial latency, and M the number of stages of the circuit. For example, to calculate the SDN network throughput of 4-to-16 decoder can be seen below, which have 16 outputs, four stages, and $9 \times 10{-}12$ s initial latency. In the proposed SDN block of 4-to-16 decoder structure, the molecular QCA throughput is Tr

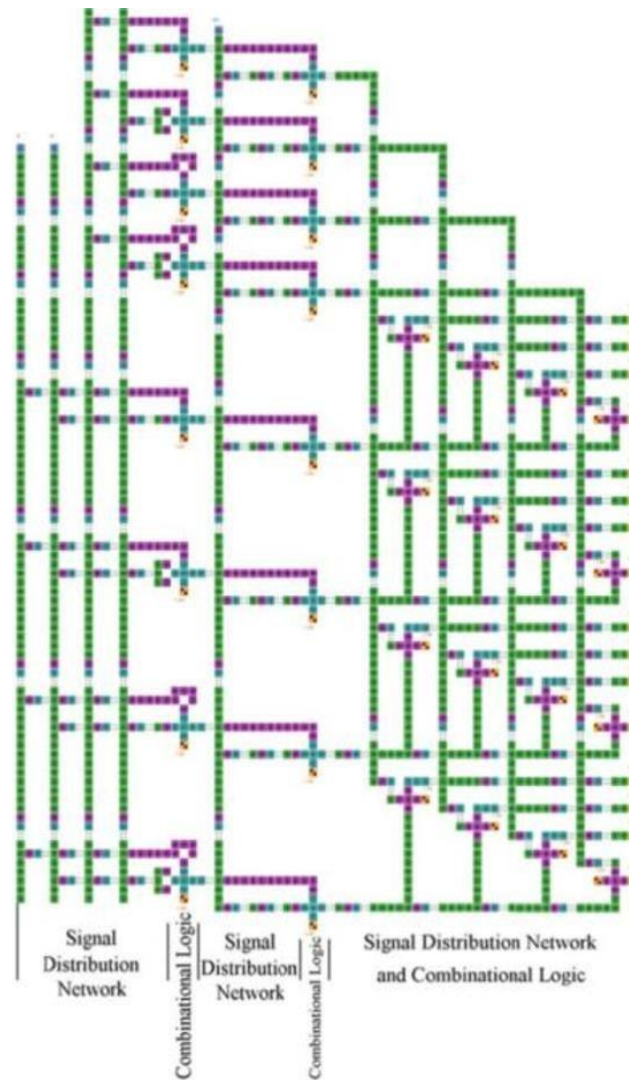= O ·M/2Lb = 16×4/2× 9×10−12 s ≈ 35 Gbit/s and Tr =35/8≈4 GB/s.

Figure 3. QCA layout of 4 x 16 decoder

3.2 16 X 1 MUX in QCA

The necessary design for 512-bit Static RAM i.e.,16 x 1 multiplexer design and execution has been discussed in this section. Twenty-four three input majority gates are required to construct the two input AND and OR gates in the first stage, AND and OR gates in the second stage are developed by the help of 12 three-input majority gates, nine three-input majority gates are required enough to implement the two-input AND and OR gates in the third and fourth stages. Thus in that way overall 16-to-1 multiplexer (MUX) is developed with the inputs of Input 1..,...,Input 16, and the selecting pins are P, Q, R, S. Figure 4 shows execution of suggested 16 x 1 multiplexer in cellular automata. The suggested 16 x 1 multiplexer utilized 3873 cells with the consumed area of 6.19 µm2 (2650 nm × 2322 nm).
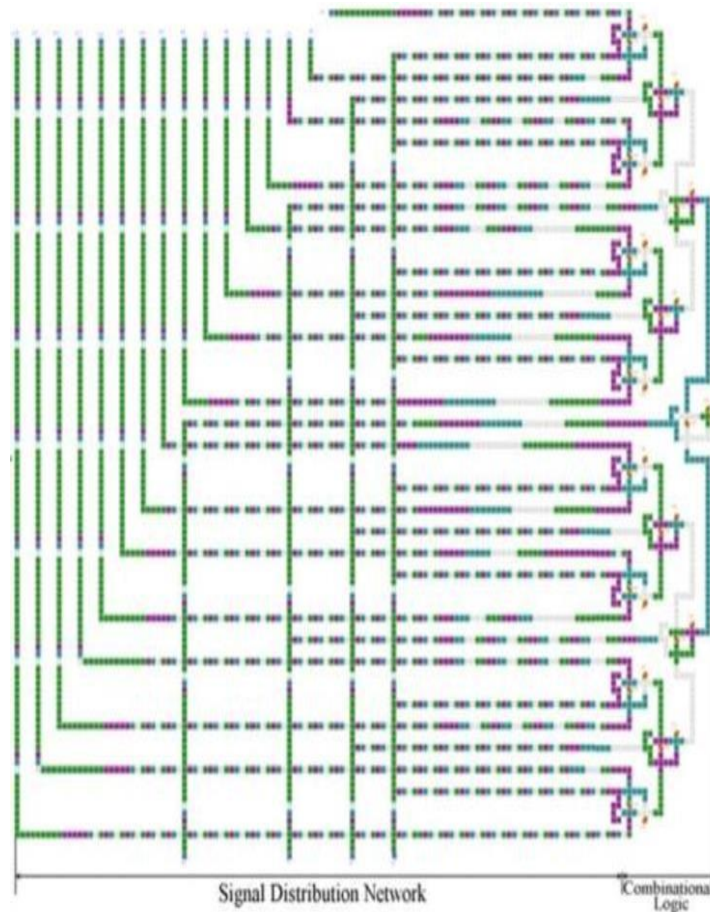
Figure 4. QCA layout of 16 x 1 mux

4 DESIGN OF 16 BIT STATIC RAM

The proposed methodology of this paper is that designing a 16-bit SRAM using 2 x 4 decoder and a 4 x 1 mux which was developed with the help of 2 x 1 mux. A 4-bit memory cell is cascaded in between those two proposed 2 x 4 decoder and 4 x 1 mux in QCA technology.

4.1 2 X 4 DECODER in QCA

Four two input AND gates are used in the design of first stage of the 2-to-4 decoder and those inputs are interlinked to the input wires A, B. For accessing the outputs, again four two-input AND gates are used by the 2-to-4decoder in the second stage. 2 x 2 two-input AND gate network are used to get the outputs. Figure 5 represents the diagrammatic structure and its execution. By the time ENABLE pin is in OFF state (ENABLE=0), all outputs are observed to be null. But when ENABLE is ON (ENABLE = 1), the results show in connections to input pins A, B. The suggested 2-to-4 decoder consists of 361 cells having consumed an area of 0.44 μm2.
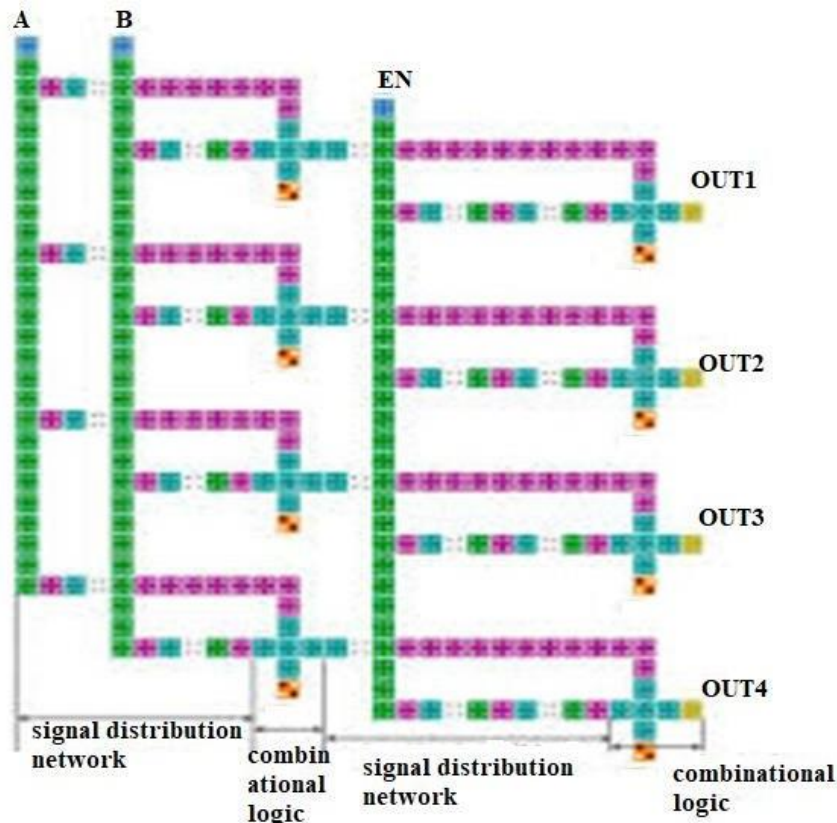
Figure 5. QCA layout of 2 x 4 decoder

4.2   4 X 1 MUX in QCA

The necessary design for 16-bit SRAM i.e.,4-to-1 multiplexer (MUX) design and execution has been discussed in this section. Six three input majority gates are required to construct the two input AND and OR gates in the first stage, AND and OR gates in the second stage are developed by the help of 3 three-input majority gates, four three-input majority gates are required enough to implement the two-input AND and OR gates in the third and fourth stages. Thus in that way overall 4-to-1 multiplexer (MUX) is developed with the inputs of Input1,,Input4, along with them the selecting pins are P, Q. Figure 6 gives execution of suggested 4 x 1 multiplexer in cellular automata. The developed 4-to-1 multiplexers with 152 cells having consumed the area of 0.31 μm2.
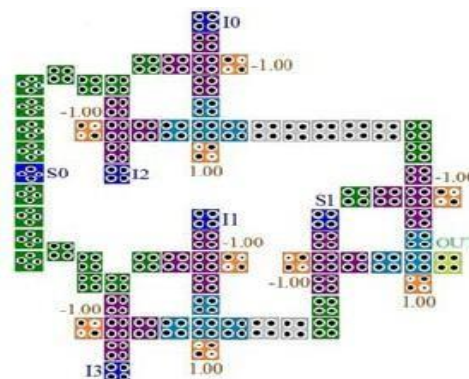

Figure 6. QCA layout of 4 x 1 mux

5 Memory cell

SRAM has its own mark of basic and important role in the memory technology. They have an equivalent place compared to microcontrollers and microprocessors as they are as faster, strong, and simply developed in usual logical procedure. Since the density, speed of the SRAM cells became improved, so that the requirement for microprocessor has fallen down even though they have well-versed scaling and transistor geometries. The two main challenges to face reduction in peak to peak voltages to avoid the thermo smashing to the transistor circuit and raises in discharge via transistor logic. This paragraph represents execution of a memory cell by quantum dot cells. In the suggested shape (Figure 7), By the time ENABLE=1, result is activated, while ENABLE = 0, then the result = NULL. When READ/WRITE = 1, the write stage is activated and the D value is stored in the memory device. When READ/WRITE =0, the read state is activated then the retained bit is stored in the result part. Memory cell stages explained in the Table I. From Figure 7, we can observe that the memory cell has four-phase of clock to operate the memory loop such that the design can be prevented from the crossing of coplanar which provides the standard structure of QCA cells. The most important part of QCA which makes it to put check to the CMOS technology is pipelining. Dot cells has thickness which have extensively higher than that of CMOS technology. The suggested memory cell consists of 52 cells having consumed the place of 0.054 µm2 (261.33 nm ×199.87 nm).

Figure 7. QCA layout of a memory cell

Table 1. memory cell operation

Mode	R/W	EN	D	Memory Loop	Output
Read	0	0	X	Unchanged	0
Read	0	1	X	Unchanged	Stored Value
Write	1	X	0	0(next cycle)	Don't Care
Write	1	X	1	1(next cycle)	Don't Care

By cascading all the three of 2 x 4 decoder, 4 x 1 mux and a memory cell, we can achieve the proposed methodology that is 16-bit SRAM. Through the suggested design of 4 x 4 RAM, we can analyze the functionality and capability. Four suggested RAM cells are required to execute the desired structure. Each row of QCA memory cell can be utilized by addressing them through the decoder circuit. By the help of all these designs, a 2D addressable array is developed as shown in Figure 8. Right hand side bottom is for serial OR array generates the outputs to get the results from each cell, whereas vertical decoder lines are used to denote vertical columns. To get the output from

all the four memory cells OR should be get activated. The value stored in selected cell is equal to the output of the complete RAM structure. By the help of increasing the size of the address words or width of bit size along with increasing number of memory cells by scaling i.e., adding rows, we can enlarge this design to larger size. This leads to increase in delay. With the help of interference of clocking phases and coplanar based cross over the suggested layouts of the 16bit SRAM with one layer was implemented.
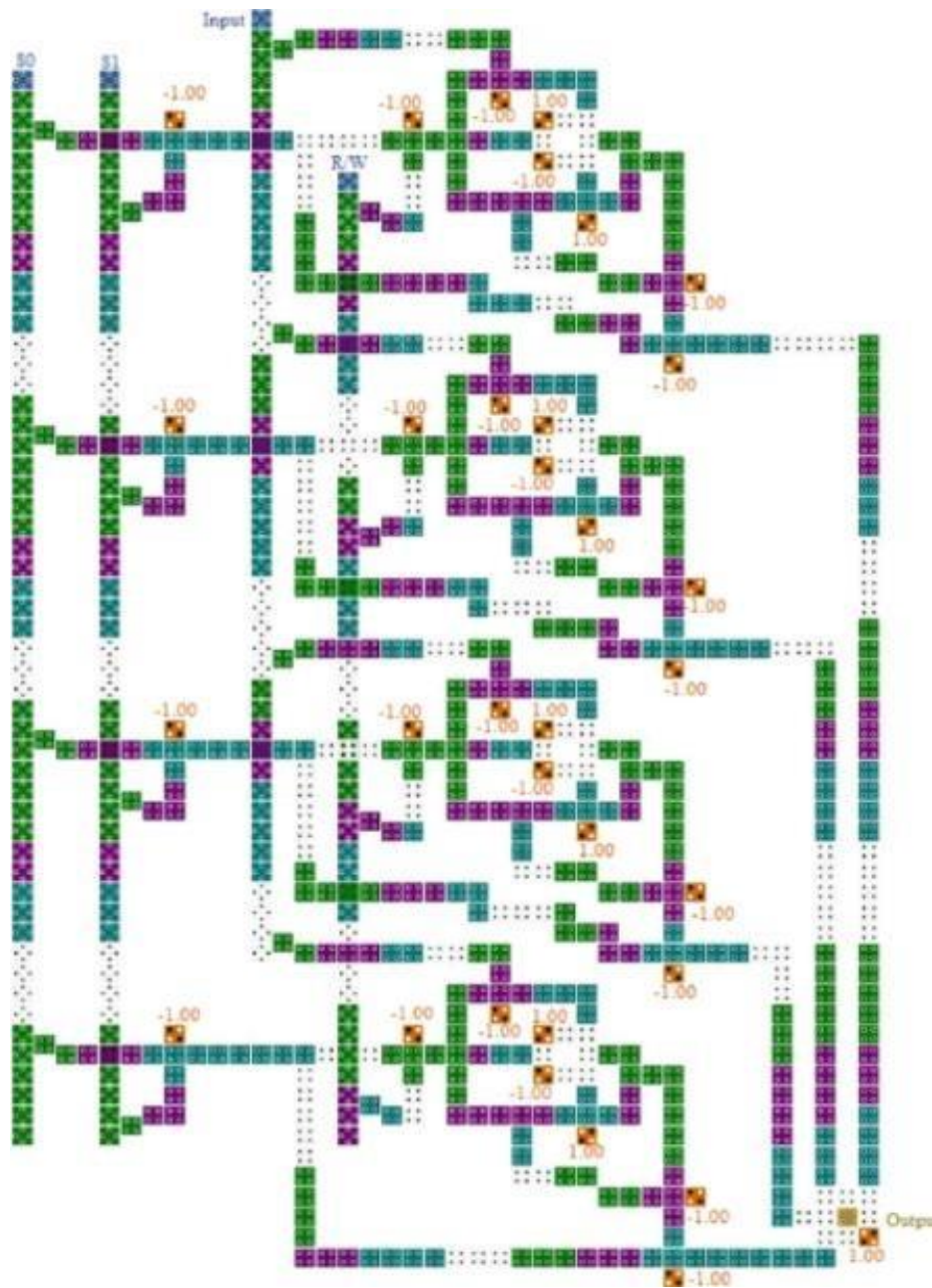

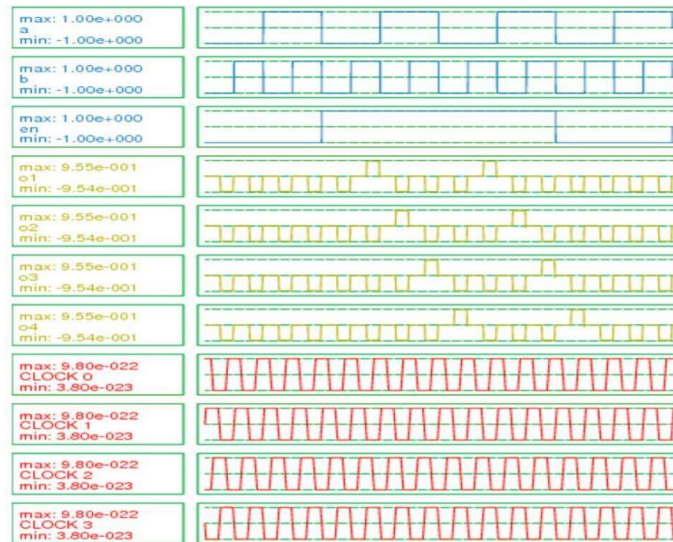**Figure 8.** QCA layout of 4x4 SRAM cell

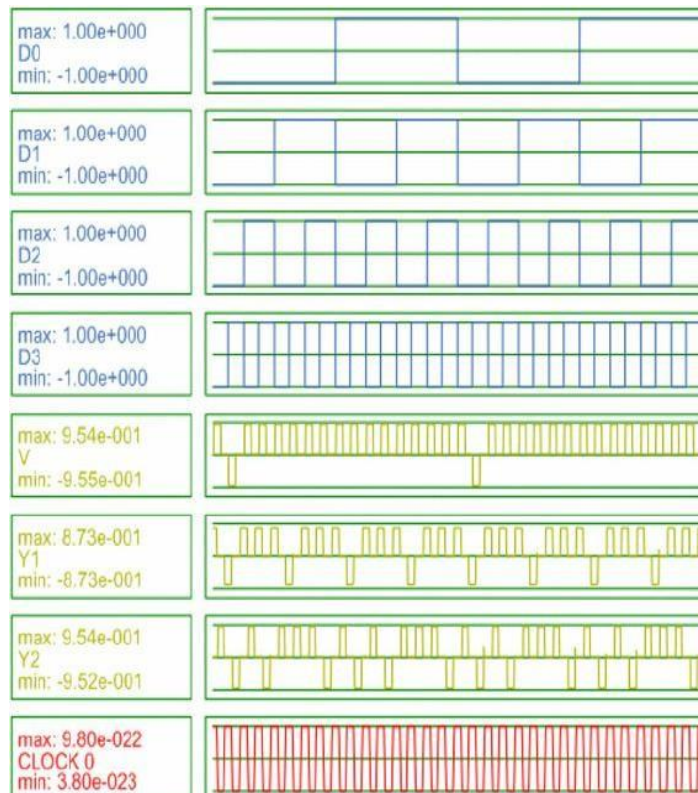## *6* Simulation results

Figure 9. 2-to-4 decoder using QCAD

Figure 10. 4 x 1 mux using QCAD
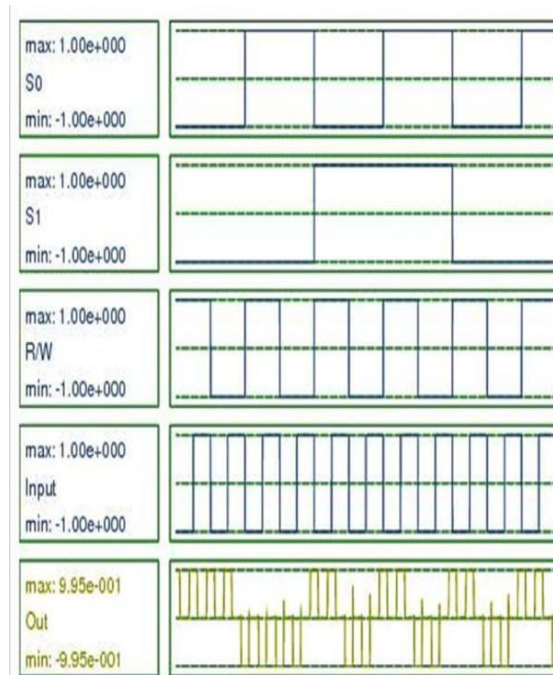
Figure 11. 4 x 4 SRAM cell

Table 2. COMPARISION TABLE

TYPE	AREA	CELL COUNT	CLOCK CYCLE DELAY	POWER
QCA BASED **2-TO-4** DECODER	0.44um^2	361	11	0.71uw
QCA BASED **4-TO-1** MUX	0.31um^2	152	9	3.07uw
QCA BASED **16** BIT SRAM	1.65um^2	860	14.5	11.13uw
CMOS BASED **16** BIT SRAM	4.987um^2	A 6T SRAM CELL	1ns	18.08uw

7 CONCLUSION

The design and execution with simulation of 16-bit SRAM using QCA technology was clearly explained in this paper. The suggested design and simulation of a brand-new reminiscence cell structure primarily based on QCA with the proper programmable logic and interconnections. For getting rid out of the planar hassle of intersecting labels, the new signal distribution network has been used to implement the 16-bit SRAM with 2-to-4 decoders and 4-to-1 mux's. The SRAM suggested here in this paper is a special design compared to the earlier studies. It is remarkably developed, since that Static RAM have a 4-bit breadth. In contrast with past researches, because of having powerful pipelining structure with in the QCA, this SRAM is very fast in executing operations. Lots of applications are there by considering the suggested Static RAM. The diagrams can be executed with the help of the QCA Designer equipment and executed by the QCAD. The simulated consequences represent the suggested Static RAM shows a work as a much efficient device. After comparing the results of suggested Quantum dot CA depended Static RAM in this literature with CMOS based Static RAM it was clear that area, clock cycle delay, and power dissipation obtained in the QCA based SRAM are highly improved. But in phrases of power consumption (in the molecular QCA) and clock cycle delay (in the semiconductor QCA) were deprecated, which can be observed because of the usage of SDN network. This SDN problem with some kind of latency and power consumption will be improved in later efforts by the help of taking possible procedures in intersection adjoining labelling of quantum dot cells circuits.

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