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Design and Implementation of Seventeen Level Inverter With Reduced Components

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ABSTRACT The multilevel inverters (MLI) are resourceful in producing a voltage waveform with superior-quality staircase counterfeit sinusoidal and depressed harmonic distortion (THD). Several conventional topologies are proposed to realize the MLI however, the limitations of these topologies may involve more DC sources and power-switching devices, and less THD, which in turn, increases the cost and size of the inverter. These drawbacks can be eliminated with the proposed hybrid Cascaded H-Bridge Multilevel Inverter with reduced components topology. As compared with the established MLI topologies the recommended topology having a reduced number of DC sources, power-switching devices, component count level factor, lesser TSV, more efficient, lesser THD, and cost-effective. The proposed MLI is a blend of a single-phase T-Type inverter and an H-Bridge module made of sub switches. This article incorporates the design and simulation of the multilevel inverter with staircase PWM technique. Further, the 9-level and 17-level MLI is examined with different combinational loads. The proposed inverter is stable during nonlinear loads, and it is well suited for FACTS and renewable energy grid-connected applications. An operational guideline has been explained with correct figures and tables. The Output voltage wave is realized in numerical simulation. Finally, the experimental demonstrations were performed by implementing a hardware prototype setup for both linear and nonlinear loads using the dSPACE controller laboratory.

INDEX TERMS Hybrid cascaded H-bridge multilevel inverter with reduced components, pulse width modulation (PWM), total harmonics distortion (THD).

I. INTRODUCTION

Present in many industrial applications has bid higher power appliances in the last couple of years. A couple of medium voltage service appliance requires high-power and medium voltage level; it is challenging directly connect only one power electronic switch to the medium power grid. To overcoming this, the multilevel inverters (MLIs) were developed in 1975 as a substitute in medium voltage high-power circumstances [1]. MLIs are turning into a well-known option to two-level inverters in the view of their several advantages, such as lesser harmonic distortion, simplified filters, better wave capability taking after a sinusoidal output, and reduced voltage stress dv/dt up on the switches, because of excellent power quality, MLIs are broadly used in all disciplines of electrical engineering, for example, renewable energy conversion, high voltage DC transmission, distributed generation (DG) system, modern drive applications, uninterruptible power supplies, and so on [2]. MLI's incorporate with power semiconductor components and various DC links to build up staircase waveform tends towards sinusoidal. Mainly three traditional multilevel inverter topologies have existed: they are neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs). Out of these, because of modular

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topology CHB-MLI having high voltage and power levels also more reliable, it requires more power semiconductor switches [3], hence switching losses increase and increasing the size, and overall cost of the circuit. In the view of these demerits, considerable MLIs were originated with the particularized objective of minimizing the quantity of power electronic devices, such topologies are called as reduced device count MLIs [4]. The topology in [5] suggested a basic structure with eight unidirectional and one bidirectional switch to produce 15 levels, authors in [6] proposed the symmetric configuration to produce higher levels but it requires more capacitors and the design suffers from higher standing voltages across the devices. The circuit in [7] is a nine-level inverter with twelve switches; three different frames are cascaded in [9] to get the desired nine-level output with ten switches, authors in [10] developed an S^3CM with twelve switches, two capacitors, and one DC source to synthesize nine levels. A modified S^3CM was proposed in [11] to produce nine levels with seven switches and two capacitors; however, it needs two DC voltage sources. To overcome the demerits in [10] and [11] a compact switched capacitor multilevel inverter was proposed in [12]. A Square T-Type topology was proposed in [13] to produce seventeen levels with four DC power sources. A modified ST-type topology known as K-type structure in [14] uses two additional switches to deliver thirteen-levels and reduces the DC sources to two by changing two capacitors. T-Type inverter topology without H-Bridge was proposed in [15] to achieve different higher levels at various load conditions with ten power switches, including two bidirectional switches. A generalized symmetric cascaded topology to reduce the total standing voltage was presented in [16] it uses a new h-type topology for both symmetric and asymmetric configuration. A higher-level inverter topology suitable for both high and low switching frequencies was proposed in [17]. Besides this [22]–[25] have been presented the reduced MLI topologies to minimize the devices count and stress voltage of the power switches.

This article highlights the reestablish framework of hybrid CHB-MLI topology with the prime objective of a minimized number of switches and increased output levels. Hence, the introduced design is named 'Hybrid Cascaded H-Bridge Multilevel Inverter with Reduced Components'. The remnant of the work is systematized: the proposed 9 level and seventeen levels Hybrid CHB-MLI topology are enlightened in Section II, in Section III calculated the power losses of the proposed multilevel inverter, homogeneity of parameters between the proposed MLI and standardized topologies are summarized in Section IV, Simulation, and test-based prototype results of proposed topology were executed in Section V, and at the end, conclusions are made in Section VI.

II. PROPOSED HYBRID CASCADED H-BRIDGE MULTILEVEL INVERTER

A. BASIC 9 LEVEL INVERTER TOPOLOGY

In this section, various issues related to Cascaded H-Bridge MLIs are addressed and the proposed hybrid Cascaded H-Bridge Multilevel Inverter with reduced components is presented by improvisation of CHB-MLI [8] for the valuation of quality output voltage with lower THD, reduced number of switches, and minimized the dv/dt stress on switches. The structure of the proposed 9 level inverters is incorporated with two DC sources V_1, V_2, and six unidirectional switches from S_1 to S_6 along with bidirectional switch S_a and two Capacitors C_1, C_2 which are connected in a blend of single-phase T-Type inverter and a module of H-Bridge made of sub switches are depicted in FIGURE 1. The specific arrangement reduces the additional DC source requirement also simplifies the number of switches needed. For a superior comprehension of working and the functioning of the introduced topology, various working modes have been represented along with conducting power electronic devices and path of load current I_0 as depicted in FIGURE 2.

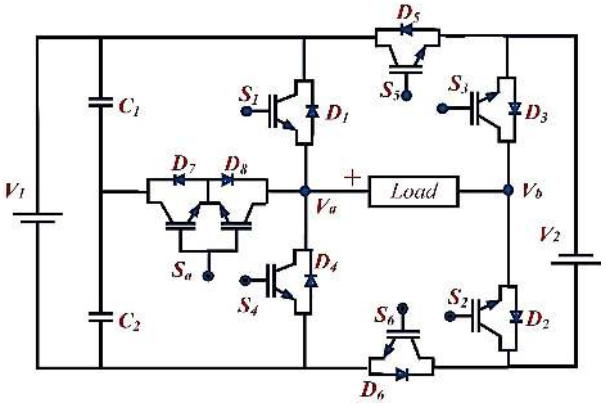

FIGURE 1. Proposed hybrid cascaded H-Bridge multilevel inverter topology.

1) OPERATING MODES

In this portion, the proposed inverter operation is explained through the various modes of output voltage levels produced in a steady-state. In this, the DC source voltage (V_{DC}) is equally shared by the two DC link capacitors C_1 and C_2 with equal magnitudes, i.e., $V_{C1} = V_{C2} = V_{DC}/2$.

Mode 1: Capacitor, C_2 acts as a voltage source, and bidirectional switch S_a, Switches S_2, S_6 are in conduction state hence the path of load current (I_0) is through C_2- S_a- D_8-load-D_2-S_6-C_2, the output voltage level is + $V_{DC}/2$, i.e. +100V.

Mode 2: Operation voltage source V_2 and switches S_6, S_4, S_3 are in conduction state; hence the path of load current I_0 is through V_2-S_6-D_4-load-S_3-V_2, the output voltage level is + $V_{DC,}$ i.e. +200V.

Mode 3: Voltage source V_2, capacitor C_2 acts as voltage sources, and bidirectional switch S_a, switches S_6, S_3 are in conduction state hence the path of load current I_0 is through V_2-S_6-C_2-S_a-D_8-load–S_3-V_2, the output voltage level is +3 $V_{DC}/2$, i.e. +300 volts.

Mode 4: Voltage source V_2, capacitors C_1, and C_2 acts as voltage sources, and switches S_6, S_1, S_3 are in conduction state hence the path of load current I_0 is through

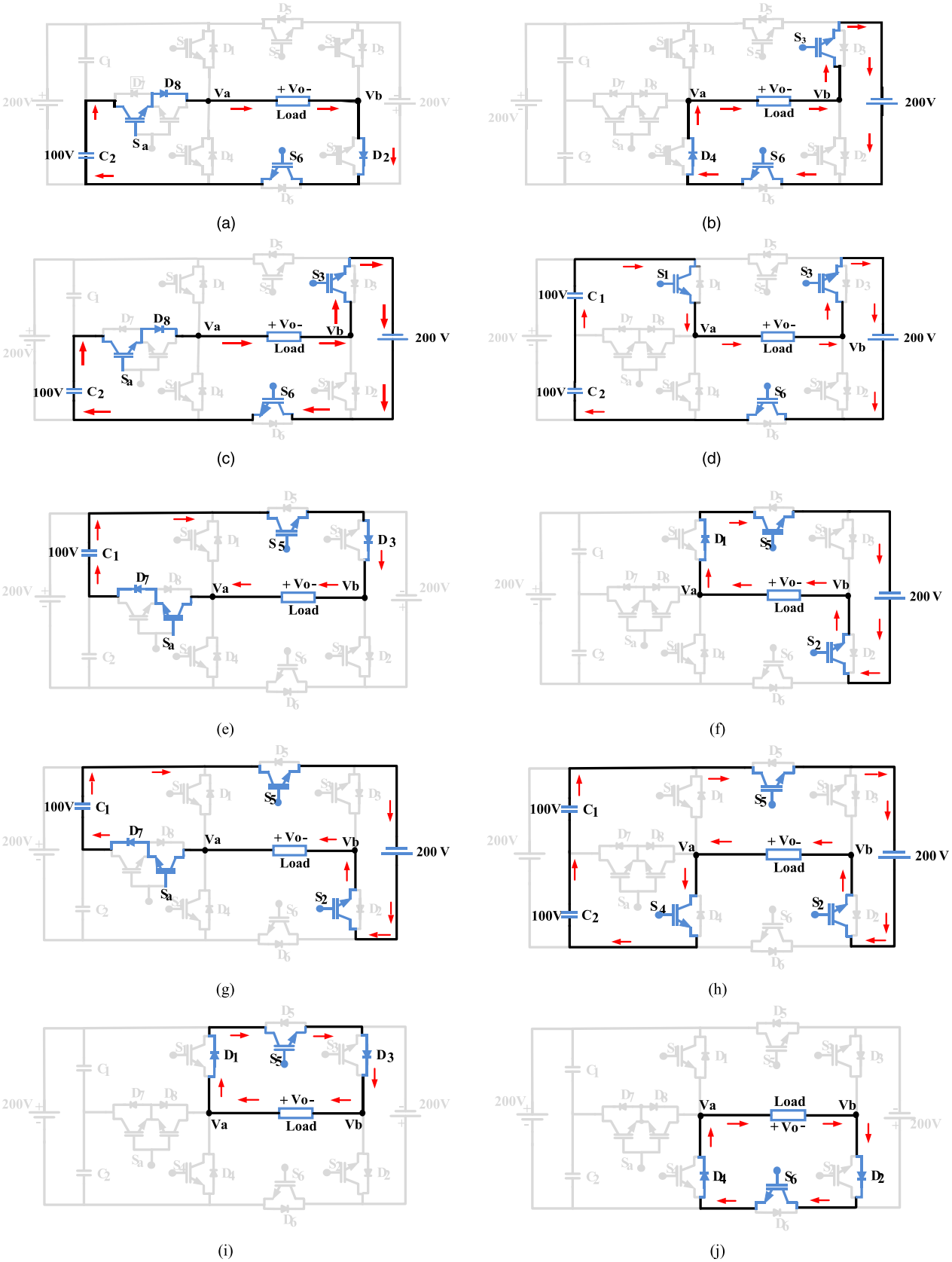

FIGURE 2. Operating modes (a) Mode-1, (b) Mode-2, (c) Mode-3, (d) Mode-4, (e) Mode-5, (f) Mode-6, (g) Mode-7, (h) Mode-8, (i) Mode-9, (j) Mode-10.

V_2-S_6-C_2-C_1- S_1-load–S_3-V_2, the output voltage level is $+2V_{DC}$, i.e. +400V.

Mode 5: Capacitor, C_1 acts as voltage sources and bidirectional switch S_A, switches S_5, S_3 are in conduction state hence the path of load current I_0 is through C_1-S_5-D_3-load-S_a- D_7-C_1, the output voltage level is $(-V_{DC}/2)$, i.e. (−100V).

Mode 6: Voltage source V_2 and switches S_2, S_1, S_5 are in conduction state hence the path of load current I_0 is through V_2-S_2-load-D_1-S_5-V_2, the output voltage level is $(-V_{DC})$, i.e. (−200V)

Mode 7: Voltage source V_2, capacitor C_1 acts as voltage sources, and bidirectional switch S_a, switches S_2, S_5 are in conduction state hence the path of load current I_0 is through V_2-S_2-load-S_a-D_7-C_1-S_5-V_2, the output voltage level is $(-3\ V_{DC}/2)$, i.e. (−300V).

Mode 8: Voltage source V_2, capacitors C_1 and C_2 act as voltage sources and, switches S_2, S_4, S_5 are in conduction state hence the path of load current Io is through V_2-S_2-load-S_4-C_2-C_1-S_5-V_2, the output voltage level is $(-2\ V_{DC})$, i.e. (− 400V).

Mode 0: Switches S_2, S_6, S_4 are in the conduction state, and the output voltage level is 0 volts during positive zero-crossing and switches S_5, S_3, S_1 are in the conduction state, and the output voltage level is 0 V during negative zero-crossing, and the expected 9 level waveform of the proposed topology is shown in FIGURE 3.

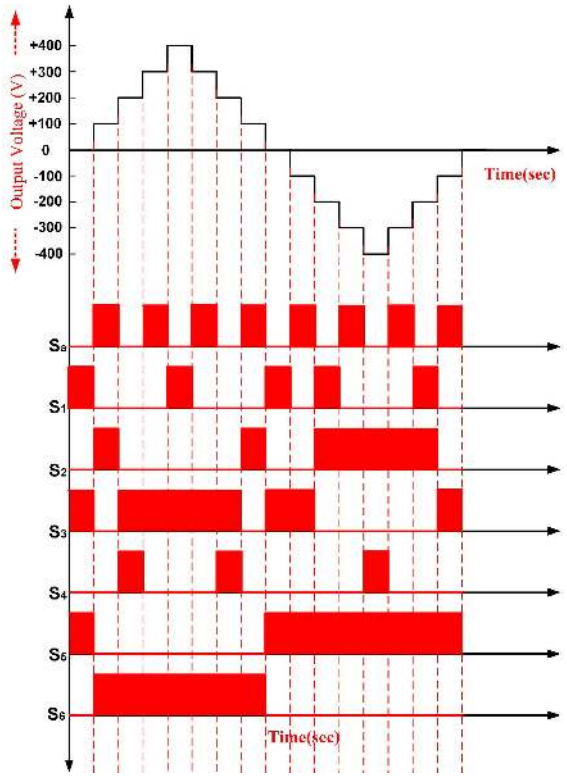

FIGURE 3. Expected 9 level waveform of the proposed topology proposed.

The operation of the proposed nine-level inverters is easily visualized from the information present in the switching table. If the switch is in the "1" state at that point, it is viewed as that switch is directing. Likewise, if the switch is in a "0" state at that point, it is viewed as that switch is not directing. TABLE 1 represents the switching states according to which the voltage is produced. The operation of the proposed 9 level inverters is divided into nine modes based on the inverter output. This structure is made of two equal DC sources V_1 & V_2 owing a magnitude of 200V each and capacitors C_1 and C_2 100 V each. Therefore, 400V is the peak output voltage; hence the inverter is asymmetrical.

TABLE 1. Switching states of 9 level inverter.

Switching Levels	S_a	S_1	S_2	S_3	S_4	S_5	S_6	Output voltage (V_{ab})
L_1	0	1	0	1	0	0	1	+400
L_2	1	0	0	1	0	0	1	+300
L_3	0	0	0	1	1	0	1	+200
L_4	1	0	1	0	0	0	1	+100
L_5	0	0	1	0	1	0	1	0+
	0	1	0	1	0	1	0	0-
L_6	1	0	0	1	0	1	0	-100
L_7	0	1	1	0	0	1	0	-200
L_8	1	0	1	0	0	1	0	-300
L_9	0	0	1	0	1	1	0	-400

For the asymmetric source configuration in the proposed topology, the generalized mathematical expressions are let the input DC sources are V_{DC1} and V_{DC2}, the voltages across capacitors C_1 and C_2 are V_{C1} and V_{C2} which is half of the input DC voltage V_{DC2}.

$$V_{DC1} = V_{DC2} \tag{1}$$

$$V_{DC2} = V_{C1} + V_{C2} \tag{2}$$

$$V_{C1} = V_{C2} = 0.5V_{DC2} \tag{3}$$

The expressions for the number of DC sources n, number of output levels N_{Lev}, the required number of power switches N_S, necessary number of diodes N_d, number of DC-link capacitors required N_{cap}, peak voltage $(VDC)_{max}$ are

$$n = \frac{(N_{Lev} - 1)}{4} \tag{4}$$

$$N_S = \frac{7(N_{Lev} - 1)}{8} \tag{5}$$

$$N_d = N_{lev} - 1 \tag{6}$$

$$N_{cap} = \frac{(N_{Lev} - 1)}{4} \tag{7}$$

$$(V_{DC})_{max} = V_{DC} \sum_{k=1}^{n} k = nV_{DC} \tag{8}$$

In this aspect to generate 9 level output Inverter requires 2 DC sources, 7 power switches IGBTs, 8 diodes, and 2 DC-link capacitors, the magnitude of peak DC voltage is 400 V.

TABLE 2. Operating modes of proposed 17 level inverter.

Modes	*Path of load current I_0*	*Output voltage (V_{ab})*
Mode-1	$V_{2a} - S_{6a} - C_{2a} - C_{1a} - S_{1a} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_{2b} - S_{6b} - C_{2b} - C_{1b} - S_{1b} - V_{ab} - V_{ba} - S_{3a} - V_{2a}$	+ 400
Mode-2	$V_{2a} - S_{6a} - C_{2a} - S_{Aa} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_{2b} - S_{6b} - C_{2b} - C_{1b} - S_{1b} - V_{ab} - V_{ba} - S_{3a} - V_{2a}$	+ 350
Mode-3	$V_{2a} - S_{6a} - D_{4a} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_{2b} - S_{6b} - C_{2b} - C_{1b} - S_{1b} - V_{ab} - V_{ba} - S_{3a} - V_{2a}$	+ 300
Mode-4	$C_{2a} - S_{Aa} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_{2b} - S_{6b} - C_{2b} - C_{1b} - S_{1b} - V_{ab} - V_{ba} - D_{2a} - S_{6a} - C_{2a}$	+ 250
Mode-5	$V_{2b} - S_{6b} - C_{2b} - C_{1b} - S_{1b} - V_{ab} - V_{ba} - D_{2a} - S_{6a} - D_{4a} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_{2b}$	+ 200
Mode-6	$C_{2b} - S_{Ab} - V_{ab} - V_{ba} - D_{2a} - S_{6a} - D_{4a} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_2 - S_{6b} - C_{2b}$	+ 150
Mode-7	$V_{2b} - S_{6b} - D_{4b} - V_{ab} - V_{ba} - D_{2a} - S_{6a} - D_{4a} - V_{aa}$ – Load - $V_{bb} - S_{3b} - V_{2b}$	+ 100
Mode-8	$C_{2b} - S_{Ab} - V_{ab} - V_{ba} - D_{2a} - S_{6a} - D_{4a} - V_{aa}$ – Load - $V_{bb} - D_{2b} - S_{6b} - C_{2b}$	+ 50
Mode-9	V_{aa} – Load - $V_{bb} - D_{2b} - S_{6b} - D_{4b} - V_{ab} - V_{ba} - D_{2a} - S_{6a} - D_{4a} - V_{a1}$	0
Mode-10	$C_{1a} - S_{5a} - D_{3a} - V_{ba} - V_{ab} - S_{4b} - D_{6b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{Aa} - C_{1a}$	- 50
Mode-11	$C_{2a} - C_{1a} - S_{5a} - D_{3a} - V_{ba} - V_{ab} - S_{4b} - D_{6b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{4a} - C_{2a}$	- 100
Mode-12	$V_{2a} - S_{2a} - V_{ba} - V_{ab} - S_{4b} - D_{6b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{Aa} - C_{1a} - S_{5a} - V_{2a}$	-150
Mode-13	$V_{2a} - S_{2a} - V_{ba} - V_{ab} - S_{4b} - D_{6b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{4a} - C_{2a} - C_{1a} - S_{5a} - V_{2a}$	-200
Mode-14	$V_{2a} - S_{2a} - V_{ba} - V_{ab} - S_{Ab} - C_{2b} - D_{6b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{4a} - C_{2a} - C_{1a} - S_{5a} - V_{2a}$	-250
Mode-15	$V_{2a} - S_{2a} - V_{ba} - V_{ab} - D_{1b} - C_{1b} - C_{2b} - D_{6b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{4a} - C_{2a} - C_{1a} - S_{5a} - V_{2a}$	-300
Mode-16	$V_{2a} - S_{2a} - V_{ba} - V_{ab} - S_{Ab} - C_{1b} - S_{5b} - V_{2b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{4a} - C_{2a} - C_{1a} - S_{5a} - V_{2a}$	-350
Mode-17	$V_{2a} - S_{2a} - V_{ba} - V_{ab} - S_{4b} - C_{2b} - C_{1b} - S_{5b} - V_{2b} - S_{2b} - V_{bb}$ - Load - $V_{aa} - S_{4a} - C_{2a} - C_{1a} - S_{5a} - V_{2a}$	-400

TABLE 3. Switching states of proposed 17 level inverter.

Levels	S_{Aa}	S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}	S_{Ab}	S_{1b}	S_{2b}	S_{3b}	S_{4b}	S_{5b}	S_{6b}	*Output voltage (V_{ab})*
L_1		Y		Y			Y		Y		Y			Y	+ 400
L_2	Y			Y			Y		Y		Y			Y	+ 350
L_3				Y	Y		Y		Y		Y			Y	+ 300
L_4	Y		Y				Y		Y		Y			Y	+ 250
L_5			Y		Y		Y		Y		Y			Y	+ 200
L_6			Y		Y		Y	Y			Y			Y	+ 150
L_7			Y		Y		Y				Y	Y		Y	+ 100
L_8			Y		Y		Y	Y		Y				Y	+ 50
L_9			Y		Y		Y			Y		Y		Y	0
L_{10}		Y		Y		Y				Y		Y		Y	- 50
L_{11}				Y	Y	Y				Y		Y		Y	- 100
L_{12}	Y		Y			Y				Y		Y		Y	-150
L_{13}			Y		Y	Y				Y		Y		Y	-200
L_{14}			Y		Y	Y		Y		Y				Y	-250
L_{15}			Y		Y	Y			Y	Y				Y	-300
L_{16}			Y		Y	Y		Y		Y			Y		-350
L_{17}			Y		Y	Y				Y		Y	Y		-400

Y= ON state of the switches

B. SEVENTEEN LEVEL INVERTER TOPOLOGIES

The proposed 17-level MLI is designed with two developed 9 level units in cascaded without additional circuit components. This topology consists of two unit's 'A' and 'B' having bidirectional and twelve switches with four DC sources and four capacitors as shown in FIGURE 4. The power quality issues like THD, fewer switches, dv/dt stress are minimized with this developed multilevel inverter.

1) OPERATING MODES

In this portion, the proposed inverter operation is explained through the various modes of output voltage levels produced in a steady-state. Multiple modes of operation are described in TABLE 2, and the expected 17 level waveform of the proposed topology is shown in FIGURE 5. The function of the proposed 17 level inverters is easily visualized from the switching table's information. If the switch is in "Y" state at that point, it is viewed as that switch is directing, otherwise, it is considered as that switch is not directing. TABLE 3 represents switching states according to which the voltage is produced.

III. POWER LOSS CALCULATION

The crucial power loss of switches in MLIs are conduction and switching losses [19] conduction losses are more effective in low switching frequency, whereas the switching loss

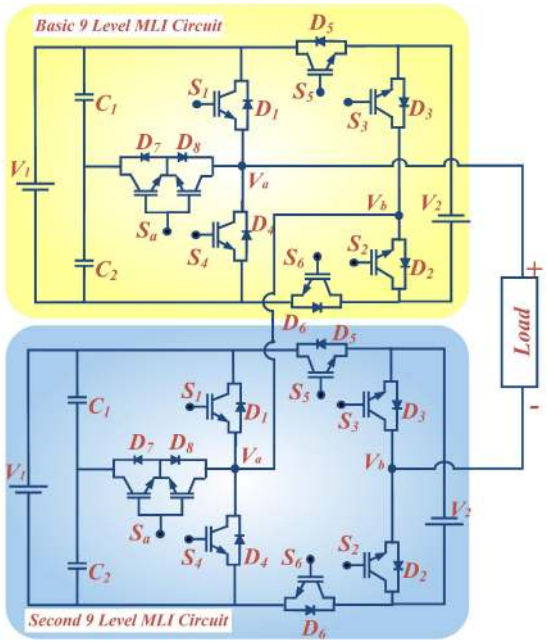

FIGURE 4. Seventeen level cascaded H-Bridge multilevel inverter topology.

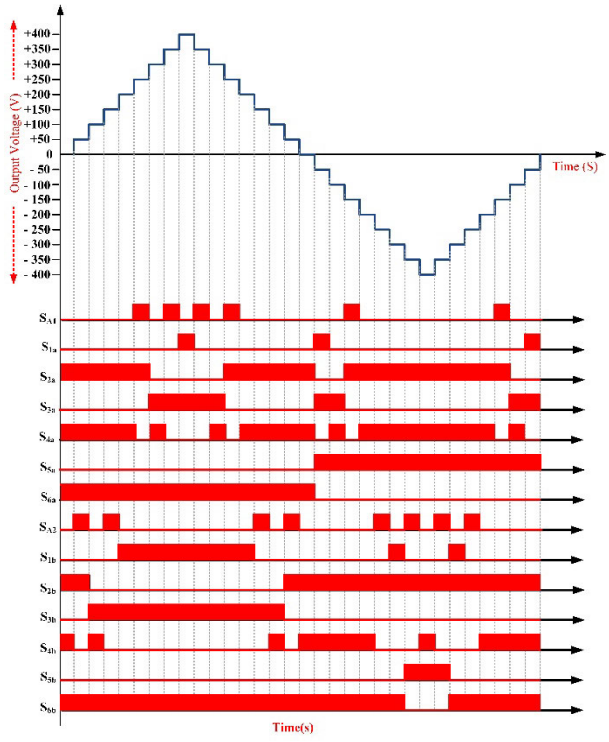

FIGURE 5. Expected 17 level waveform of the proposed topology proposed.

is dominating in high switching frequencies. Conduction loss of IGBT with antiparallel diode is for the on-state condition of resistance and voltages of both transistors and diode. Let V_S is on-state voltage, R_S is the resistance of the transistor, and V_d is on-state voltage, R_d is the diode's resistance. The conduction losses of diode P_{CD} and transistor P_{CS} are determined as follows [21]

$$P_{CD}(t) = V_d i(t) + R_d i^2(t) \tag{9}$$

$$P_{CS}(t) = V_S i(t) + [R_S i^{\beta}(t)] i(t) \tag{10}$$

where β is a constant calculated from characteristics of a power switch. Assuming there are $N_{S,ON}$ switches, and $N_{d,ON}$ diodes, are conduction at the time of instant 't' then the multilevel average conduction power losses are

$$P_{CU} = \frac{1}{\pi}\int_0^{\pi} \left[N_{S,ON}(t)P_{CS}(t) + N_{d,ON}(t)P_{CD}(t)\right] dt$$

$$P_{CU} = \frac{1}{\pi}\int_0^{\pi} \left[\begin{array}{l} N_{S,ON}(t)\left\{V_S i(t) + R_S i^{\beta}(t)\right\} \\ +N_{d,ON}(t)\left\{V_d i(t) + R_d i(t)\right\} \end{array}\right] i(t)dt \tag{11}$$

In the proposed topology there is a bi-directional switch Sa, and it conducts at the time of instant 't' then the average conduction losses are

$$P_{CB} = \frac{1}{\pi}\int_0^{\pi} \left[V_S(t) + V_d(t) + R_S i^{\beta}(t) + R_d i(t)\right] i(t)dt \tag{12}$$

Consider the output current is sinusoidal then

$$\mathrm{i(t)} = \mathrm{i_m sin(t)} \tag{13}$$

The simplified average conduction losses of a bi-directional switch can be calculated from (12) and (13)

$$P_{CB} = \frac{2}{\pi} i_m \left[V_S(t) + V_d(t)\right] + \frac{R_d i_m^2}{2} + \frac{R_s i_m^{\beta+1}}{2}\int_0^{\pi} \sin^{\beta+1}(t)dt \tag{14}$$

Therefore, total conduction losses Pc of the proposed topology is got as

$$\mathrm{P_C = P_{CU} + P_{CB}} \tag{15}$$

The switching losses occur, based on the energy losses, especially during on-state and off-state of the switches. For a switching period of a switch, there is a linear variation in voltage and current are related as follows [18]

$$P_{SW,on} = \frac{1}{T}\int_0^{t_{ON}} V(t)i(t)dt = \frac{1}{T}\int_0^{t_{ON}} \left(\frac{V_{SW}}{t_{ON}}t\right)\left(-\frac{I}{t_{ON}}(t - t_{ON})\right)dt$$

$$P_{SW,ON} = \frac{1}{6T}\left[V_{SW} I t_{ON}\right] \tag{16}$$

$$P_{SW,OFF} = \frac{1}{T}\int_0^{t_{OFF}} V(t)i(t)dt$$

TABLE 4. Variance of variant MLI topologies with regards number of output levels N_{Lev}.

Components required	CHB	NPC	FC	[10]	[13]	[9]	[11]	Proposed
Switches (N_s)	$2(N_{Lev}-1)$	$2(N_{Lev}-1)$	$2(N_{Lev}-1)$	$(N_{Lev}+3)$	$(N_{Lev}+2)$	$(N_{Lev}+1)$	$(N_{Lev}-1)$	$7(N_{Lev}-1)/8$
Diodes (N_d)	$2(N_{Lev}-1)$	$2(N_{Lev}-1)$	$2(N_{Lev}-1)$	$(N_{Lev}+3)$	$(N_{Lev}+2)$	$(N_{Lev}+1)$	$(N_{Lev}-1)$	$(N_{Lev}-1)$
Dc link capacitors (N_{cap})	0	$(N_{Lev}-1)$	$(N_{Lev}-1)$	$(N_{Lev}-1)/4$	$(N_{Lev}-1)/4$	$(N_{Lev}-1)/4$	$(N_{Lev}-1)/4$	$(N_{Lev}-1)/4$
Dc sources (n)	$(N_{Lev}-1)/2$	$(N_{Lev}-1)/8$	$(N_{Lev}-1)/8$	$(N_{Lev}-1)/8$	$(N_{Lev}-1)/8$	$(N_{Lev}-1)/8$	$(N_{Lev}-1)/4$	$(N_{Lev}-1)/4$
Driver board circuits (N_{dk})	$2(N_{Lev}-1)$	$2(N_{Lev}-1)$	$2(N_{Lev}-1)$	$(N_{Lev}+3)$	$(N_{Lev}+2)$	$(N_{Lev}+1)$	$(N_{Lev}-2)$	$7(N_{Lev}-1)/8$

TABLE 5. Variance of variant 9 level MLI topologies.

Components required		CHB	NPC	FC	[7]	[9]	[10]	[11]	[12]	[13]	[22]	[26]	[28]	Proposed
N_s		16	16	16	12	10	12	8	11	9	8	10	10	7
N_d		16	16	16	12	10	12	8	11	11	8	10	10	8
N_{cap}		0	8	8	4	2	2	2	2	0	2	0	2	2
n		4	1	1	2	1	1	2	1	4	1	4	1	2
N_{dk}		16	16	16	12	10	12	7	11	9	8	10	10	7
Fcc		5.77	6.33	6.33	4.22	3.66	4.33	3	4	3.66	3.11	3.77	3.66	2.88
TSV		16	16	16	1	-	-	9	11	11	10	16	24	5
THD		-	-	-	-	19.4	-	9.30	-	-	-	8.0	-	8.7
CF/N_{Lev}	**α=0.5**	6.666	7.22	7.22	5.27	-	-	3.5	4.611	4.278	3.55	4.66	5	3.166
	α=1.5	8.44	9	9	6.5	-	-	4.833	5.833	5.5	4.66	6.44	7.66	3.722

$$= \frac{1}{T}\int_{0}^{t_{OFF}} \left(\frac{V_{SW}}{t_{OFF}}t\right)\left(-\frac{I}{t_{OFF}}(t-t_{OFF})\right)dt$$

$$P_{SW,OFF} = \frac{1}{6T}\left[V_{SW}It_{OFF}\right] \tag{17}$$

where T is a total period and $P_{(SW,ON)}$, $P_{(SW,OFF)}$ are on-state, and off-state switching losses of the switch, t_{ON}, t_{OFF} are the ON-state and OFF-state periods of the switch respectively and V_{SW} is the peak voltage of the switch. Hence, total-switching losses P_{SW} of multilevel inverter is expressed as

$$P_{SW} = P_{SW,ON} + P_{SW,OFF} \tag{18}$$

Thus, the total power losses P_L of a multilevel inverter is the sum of conduction and switching losses; it can be expressed as

$$P_L = P_C + P_{SW} \tag{19}$$

Further, the efficiency η of the proposed MLI can be calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out}+P_L} \tag{20}$$

The output power can be got as follows;

$$P_{out} = V_{rms} \times I_{rms} \tag{21}$$

IV. COMPARISON STUDY

The asymmetrical configuration of the presented inverter topology is compared with the asymmetrical structure of Cascaded H-bridge (CHB) multilevel inverter, Neutral point clamped (NPC) multilevel inverter, flying capacitors (FC) multilevel inverter, and some other similar multilevel inverter topologies. The number of various components required regarding output voltage levels for correspondent topologies considered is calculated from the equations in TABLE 4 and tabulated in TABLE 5, and the components count per level factor F_{CCL} is calculated from (22).

$$F_{CCL} = \frac{N_S + N_d + N_{cap} + N_{dk} + n}{N_{Lev}} \tag{22}$$

The total standing voltage (TSV) is an essential factor for the selection of switches. TSV is the addition of the maximum blocking voltage across each semiconductor device.

The voltage stress of the switches in different units is given as:

$$V_{Sbi} = V_i \quad i = 1, 2 \ldots\ldots n$$
$$V_{Suni} = 2V_i \quad i = 1, 2 \ldots\ldots n$$

where n is the number of complimentary switches.

The voltage stress across each unilateral (uni) and bilateral (bi) switch can be calculated based on the circuitry.

Therefore, the generalized relation for the TSV calculation is

$$TSV = 2[VS1 + VS3 + VS5 + \ldots\ldots VS(2n+1)] \tag{23}$$

TABLE 6. Variance of variant 17 level MLI topologies.

Components required		CHB	NPC	FC	[3]	[9]	[10]	[11]	[13]	[23]	[26]	[29]	Proposed
N_s		32	32	32	10	20	24	16	14	10	20	10	14
N_d		32	32	32	10	20	24	16	20	10	20	12	16
N_{cap}		0	16	16	4	4	4	4	4	0	0	0	4
n		8	2	2	2	2	2	4	8	4	8	2	4
N_{dk}		32	32	32	20	20	24	14	14	10	20	10	14
Fcc		6.11	6.70	6.70	3.88	3.88	4.48	3.17	3.52	2	4	2	3.05
TSV		32	32	32	-	-	-	11	22	36	36	40	11
THD		-	-	-	-	-	-	-	-	7.1	3.7	-	4.23
CF/N_{Lev}	**α=0.5**	7.05	7.64	7.64	-	-	-	3.5	4.17	4.94	5.05	5.18	3.38
	α=1.5	8.94	9.52	9.52	-	-	-	4.14	5.47	9.18	7.17	9.88	4.02

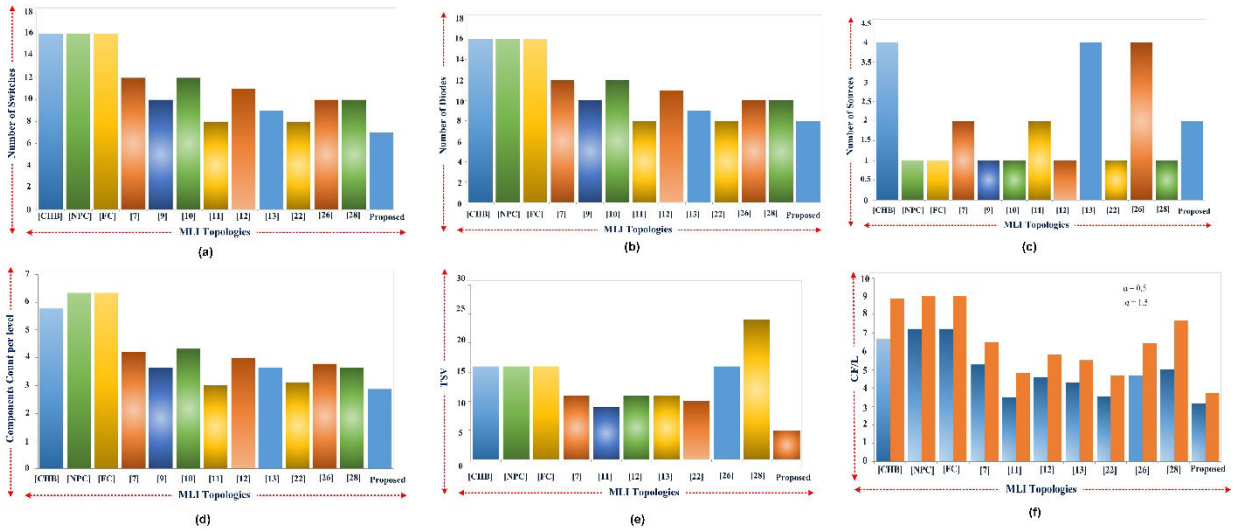

FIGURE 6. Comparison of proposed 9 level inverter topology with other topologies (a) Number of switches (b) Number of diodes (c) Number of sources (d) Components count per level (e) Total standing voltage (f) Cost factor per level.

From TABLE 5 and TABLE 6, the number of power switches needed to produce nine-level and seventeen level staircase outputs for designed topology is less than considered with other topologies. Hence, required gate driver circuits for the switches are reduced, reducing the inverter's ambiguousness. Considering that the components count per level factor F_{CCL} value is more, hence the topology requires more components to build the desired voltage level. In the recent investigations, the primary objective is to decrease components count per level factor in the design of multilevel inverter. It is noticed that the proposed inverter is having fewer components count per level factor F_{CCL} as related to the other nine-level multilevel inverter topologies. The introduced topology uses fewer switches compared to similar topologies. FIGURE 6 presents the comparison of the proposed nine-level inverter with similar topologies. The minimization of switches reduces the requirement of gate driver circuits for switches and limits components count per level factor FCCL hence reducing the inverter's complexity and the cost factor. FIGURE 7 represents the comparison result of the proposed seventeen level MLI with other topologies. From FIGURE 7, the proposed topology uses fewer components count per level factor F_{CCL}; hence the cost factor reduces and the cost factor (CF) is calculated by using the below equation

$$CF = (n + N_s + N_d + N_{dk} + N_{cap} + \alpha TSV) \qquad (24)$$

where α is a current coefficient factor

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

MATLAB/Simulink carries out the validation and practicability of the presented inverter. TABLE 7 describes various MLI parameters used for analysis. In the simulation pulses are actualized at 10 kHz carrier frequency, the design is tested for 80Ω resistive load and an inductive load of 98mH having 50Ω internal resistance. FIGURE 8(a) shows the Simulation results of output Voltage, FIGURE 8(b) shows the Simulation results of output Voltage and Current waveforms for proposed 9 level Inverter topologies. In asymmetric source configuration the magnitude of source voltages V_{dc1}, V_{dc2} considers

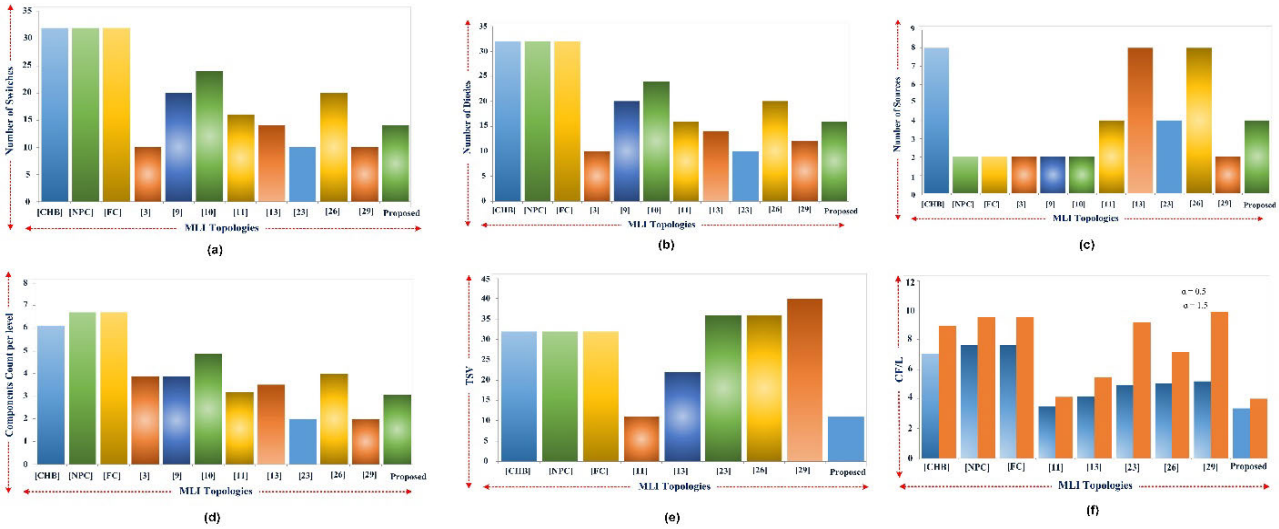

FIGURE 7. Comparison of proposed 17 level inverter topologies with other topologies (a) Number of switches (b) Number of diodes (c) Number of sources (d) Components count per level (e) Total standing voltage (f) Cost factor per level.

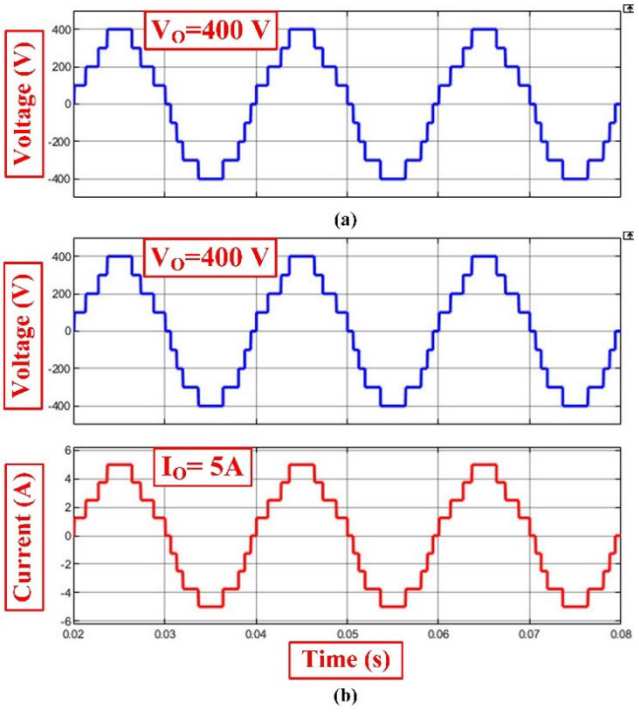

FIGURE 8. (a) Simulation result of voltage (b) Simulation result of voltage and current for proposed 9 level inverter topologies.

as 200V each, the capacitor ratings ($C_1 = C_2$) are 4700 μF with 80 V. The inverter allows to deliver nine-level output with a maximum voltage of 400V and load current of 5A. The output waveform is enhanced with THD of 8.49% shown in FIGURE 9 and FIGURE 10(a) shows the Simulation results of output Voltage, FIGURE 10(b) shows the Simulation results of output Voltage and Current waveforms for proposed seventeen level Inverter topologies. In asymmetric source configuration the magnitude of source voltages V_{adc1},

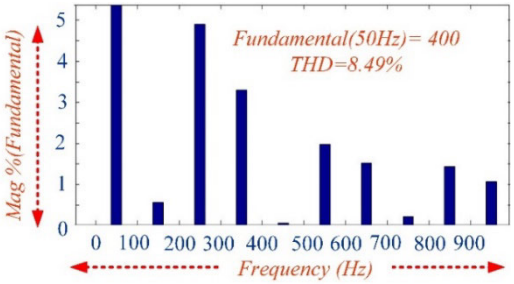

FIGURE 9. Simulation result of voltage harmonic spectrum for the proposed 9 level inverter topology.

V_{adc2} and V_{bdc1}, V_{bdc2} consider as 100V each, the capacitor ratings ($C_{a1} = C_{a2} = C_{b1} = C_{b2}$) are 4700 μF with 80 V, and the inverter allows to deliver seventeen level output with a maximum voltage of 400V and load current of 5A, the output waveform is enhanced with THD of 4.12% shown in FIGURE 11.

B. EXPERIMENTAL RESULTS

To justifying the presented inverter topology, for asymmetrical configuration, an experimental setup is accomplished in a laboratory as depicted in FIGURE 12. The inverter setup comprises seven IGBT's CM75DU-12H incited by MCT2E optocouplers, dual DC supplies with the same magnitude of 200V, and a resistive load of 80Ω, an inductive load of 98mH with 50Ω internal resistance, and dSPACE1104 is used for generating switching pulse. The waveforms of experimental gate pulses, current, and voltage are observed on the digital storage oscilloscope (DSO) shown in FIGURE 13 and FIGURE 14(a)&(b) respectively. Using a power analyzer, voltage harmonic is measured, and the voltage THD spectrum is illustrated in FIGURE 15 and the voltage THD of the proposed modulation technique is 9.85%.

TABLE 7. Various system parameters for proposed topology.

Parameter	Simulation		Experimental	
	9 – Level	17 - Level	9 – Level	17 – Level
Voltage Source	200V	100 V	200V	100 V
Capacitor ratings	80V, 4700μF	80V, 4700μF	80V, 4700μF	80V, 4700μF
Load Resistance	**80Ω**	**80Ω**	**80Ω**	**80Ω**
Inductive load	98mH	98mH	98mH	98mH
Motor load	230V, 0.5HP	230V, 0.5HP	230V, 0.5HP	230V, 0.5HP
Output Voltage (Vo)	Vrms = 282.84V	Vrms = 282.84 V	Vrms = 282.84V	Vrms = 282.84 V
Output Current (Io)	Irms=3.53A	Irms=3.53 A	Irms=3.53A	Irms=3.53 A
Carrier Frequency	10 KHz	10 KHz	10 KHz	10 KHz
Modulation Frequency	50Hz	50Hz	50Hz	50Hz

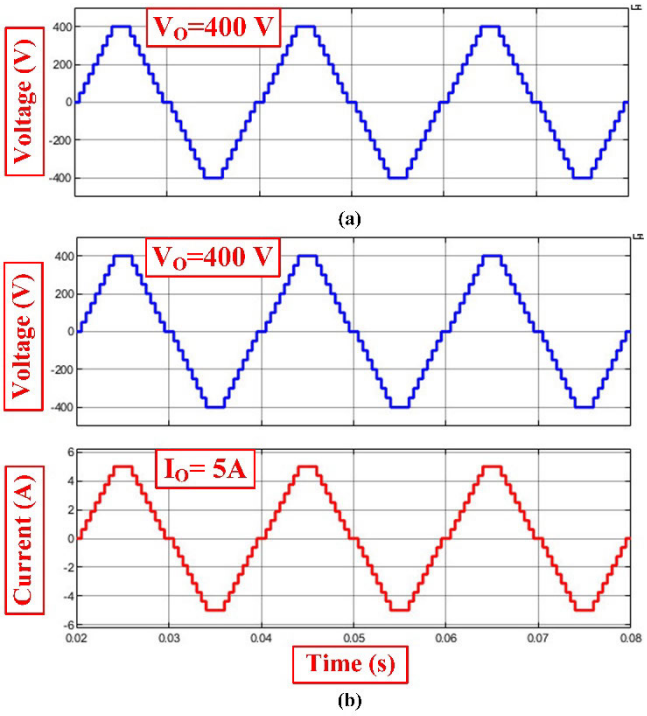

FIGURE 10. (a) Simulation result of voltage (b) Simulation result of voltage and current for proposed 17 level inverter topologies with asymmetric source configuration.

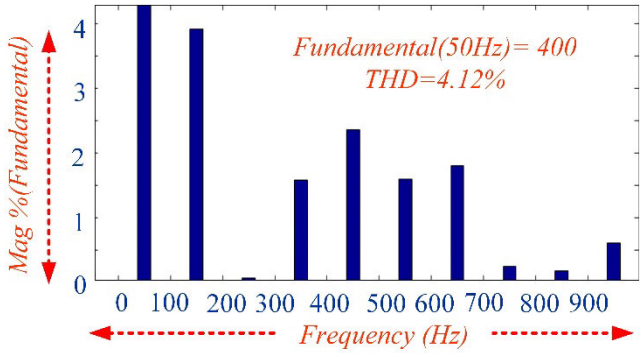

FIGURE 11. Simulation result of voltage harmonic spectrum for the proposed 17 level inverter topology.

Ruderman *et al.* [20] proposed the mathematical formulae for theoretical calculations of voltage THD, the derived value

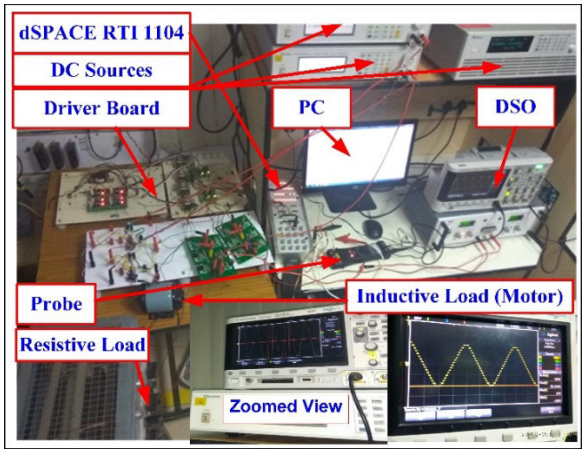

FIGURE 12. Experimental setup for the proposed topology.

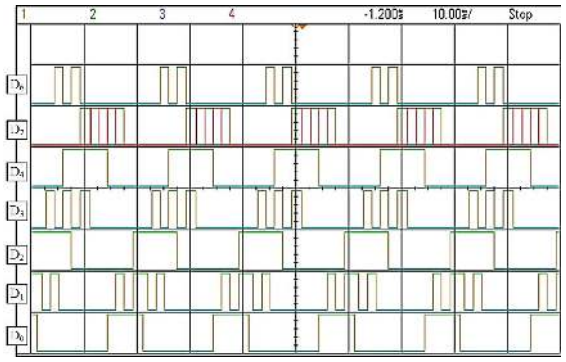

FIGURE 13. Experimental gate pulses of 9MLI.

of% THD is expressed as

$$\%\text{THD} = 1/(\sqrt{3}(N_{Lev} - 1)m_i \quad (25)$$

where N_{Lev} is the output level and m_i is the modulation index.

For $m_i = 0.9$ and $N_{Lev} = 9$, voltage THD's theoretical value is 8.01% very near to simulation and experimental THD presented in TABLE 8.

From the experimental setup, V_{rms} is 282.84V & I_{rms} is 3.53A from (21) the output power is 998.425 W. The parameter values are taken from the IGBT CM75DU-12H, R_s is 0.4-ohm, turn-on delay time as 100 ns, turn-on rising time is 250 ns, turn off delay time is 200 ns and turn off fall time

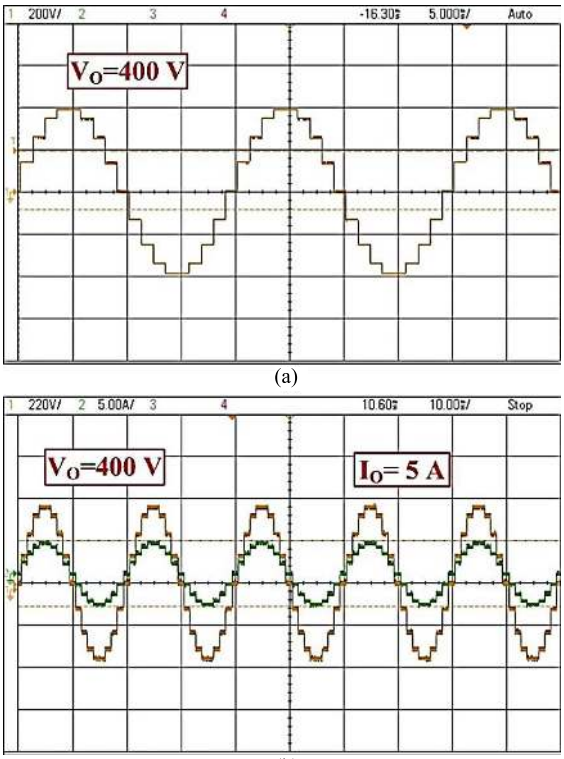

FIGURE 14. (a) Experimental result of output Voltage (b) Experimental result of output voltage and Current for 9 level inverter topologies with asymmetric source configuration.

FIGURE 15. Experimental result of voltage harmonic spectrum for 9 level inverter topology.

TABLE 8. Voltage THD for 9 levels and 17 levels.

Voltage % THD (Mi=0.9)		
9 level		
Theoretical	*Simulation*	*Experimental*
8.01	*8.49*	*8.70*
17 level		
Theoretical	*Simulation*	*Experimental*
4	*4.12*	*4.23*

as 300 ns, V_{SW} is 0.6V taken from performance characteristics. In the proposed inverter design, there are 17 steps

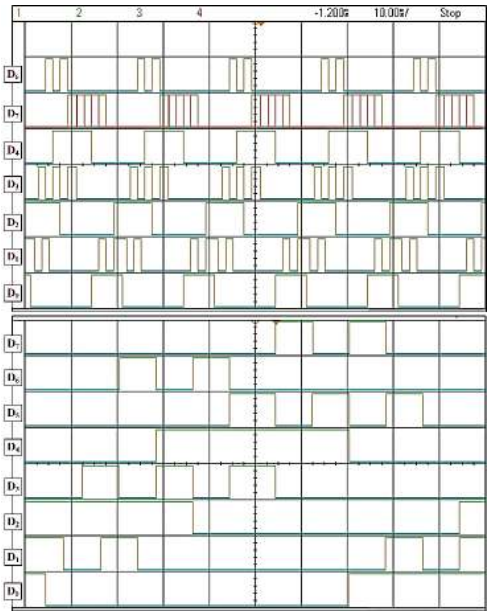

FIGURE 16. Experimental gate pulses of 17 MLI.

in one full cycle for 7 switches. From (10), the conduction losses are 49.71W and $P_{sw,on}$, $P_{sw,\ off}$ is calculated from (16), (17) and the values are 0.0415W, and 0.0594W, respectively. From (18) switching losses are the sum of $P_{sw,on}$, and $P_{sw,\ off}$. Hence the switching losses are $0.0415+0.0594 = 0.1009$ W. Therefore, the total losses are calculated during the conduction time and switching time by using (19) is 49.81W, finally from (20) efficiency η is 95.27% is nearly 2% more than compared to [9] and 15% compared to [10].

The proposed seventeen levels cascaded Inverter setup comprises fourteen IGBT's CM75DU-12H, incited by MCT2E optocouplers, four DC supplies with the same magnitude of 100V, a resistive load of 80Ω, an inductive load of 98mH with 50Ω internal resistance, and dSPACE1104 is used for generating switching pulse. The waveforms of gate pulse, current, and voltage are observed on the digital storage oscilloscope (DSO) shown in FIGURE 16, and FIGURE 17(a), (b) & (c) respectively. Using a power analyzer voltage harmonic is measured, and the voltage THD spectrum is illustrated in FIGURE 18 and the voltage THD of the proposed modulation technique is 4.23%. The output waveform of voltage and current for nonlinear loads is shown in FIGURE 19.

The dynamic responses of voltage and current when the load changes from resistance to inductance by adding an inductive load of 98mH having 50Ω internal resistance in parallel with 80Ω resistance is clearly shown in FIGURE 20, and The dynamic responses of voltage and current when the load changes from inductive load to inductive resistance load by adding a resistance load of 80Ω in parallel with an inductive load of 98mH having 50Ω internal resistance is clearly shown in FIGURE 21. The experimental Vrms is 282.8 V & I_{rms} is 3.53 A form (21) the output power is 998.284 W.

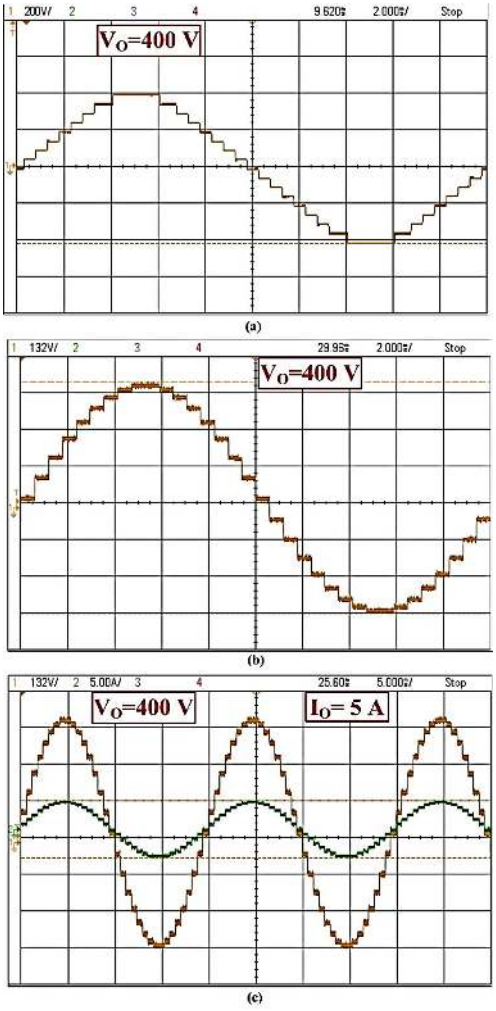

FIGURE 17. (a) & (b) Experimental result of output voltage (c) Experimental result of output voltage and current for 17 level inverter topology with R load.

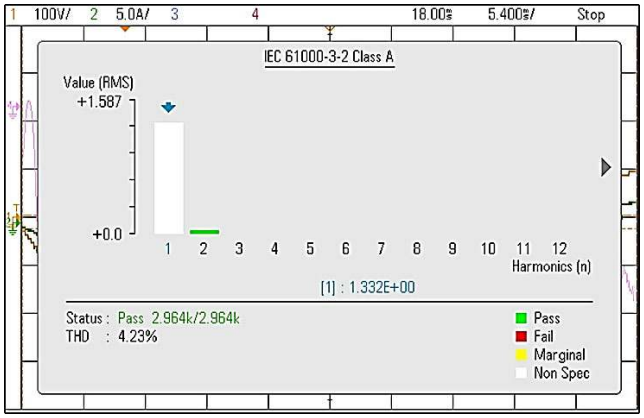

FIGURE 18. Experimental result of voltage harmonic spectrum for 17 level inverter topologies.

The parameter values are taken from the IGBT CM75DU-12H, R_s is 0.4 ohm, turn-on delay time as 100 ns, turn-on rising time is 250 ns, turn off delay time is 200 ns

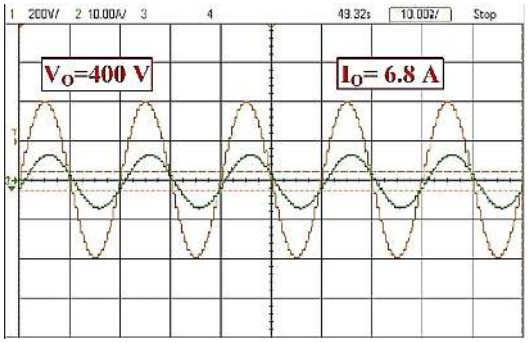

FIGURE 19. Experimental result of voltage and current waveform for 17 level inverter topology with motor load.

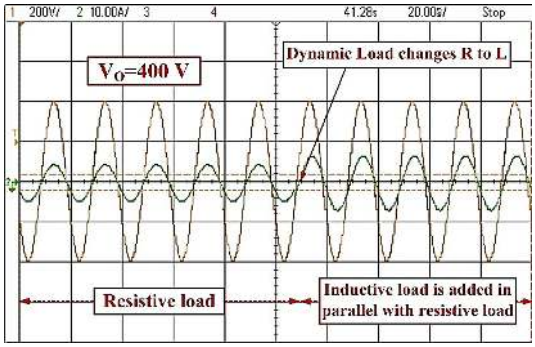

FIGURE 20. Experimental result of voltage and current waveforms for 17 level inverter topology with RL load.

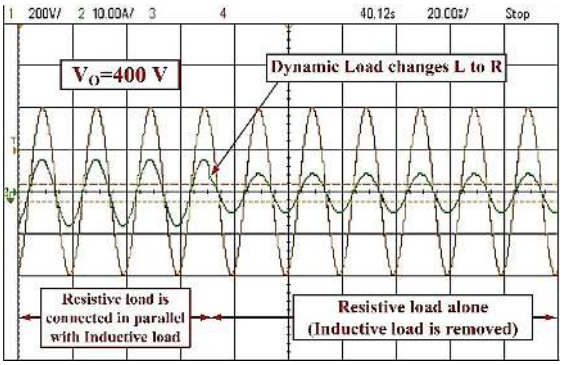

FIGURE 21. Experimental result of voltage and current waveforms for 17 level inverter topology with LR load.

and turn off fall time as 300 ns, V_{sw} is 0.6V taken from performance characteristics. In the proposed inverter design there are 33 steps in one full cycle for 14 switches. From (10), the conduction losses are 99.432 W and $P_{sw,\,on}$, $P_{sw,off}$ is calculated from (16), (17) and the values are 0.276W and 0.394 W respectively, from (18) switching losses are the sum of $P_{sw,on}$, and $P_{sw,\,off}$. Hence the switching losses are $0.276+0.394 = 0.67$ W; therefore, the total losses are calculated during the conduction time, and the switching time by using (19) is 100.102 W, finally from (20) efficiency η is 90.87%. TABLE 9 represents the proposed MLI's efficiency with resistive load and with dynamic load for seventeen levels.

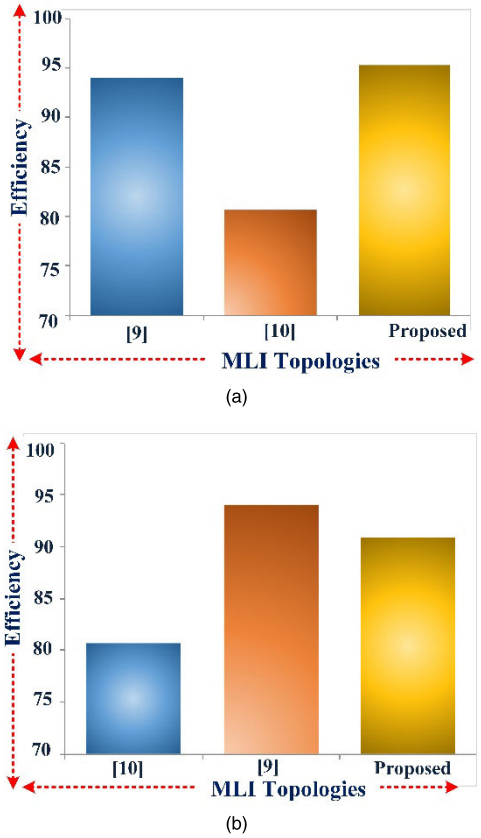

FIGURE 22. Comparison of efficiency to the proposed inverter with other topologies (a) 9 Levels (b) 17 Levels.

TABLE 9. Power and efficiency of proposed nine and 17 level MLI.

Parameters	9 level	17 Level with R load	17 Level with RL load
Vrms (v)	282.84	282.84	282.84
Irms (A)	3.53	3.53	4.80
Conduction losses (W)	49.71	99.462	135.204
Switching losses (W)	0.1009	0.67	0.911
Total losses (W)	49.81	101.102	136.1
Output power (W)	998.42	998.42	1330.08
Efficiency (%)	95.27	90.87	90.67

TABLE 10. Cost of the proposed 17 level MLI.

Components	Rating	Unit price *($)	Number of units	Total cost *($)
IGBT CM75DU-12H	1200 V, 75A	33.48	14	468.72
MCT2E optocouplers	-	0.354	16	4.602
Capacitor B41231A9128M	1.2 mF	1.51	2	3.02
Overall cost *($)				476.342

Courtesy: www.yaspro.com, www.nevonexpress.com, in.element14.com, *prices are subject to change

FIGURE 22 (a) & (b) shows the comparison of efficiency between the proposed inverter topology with other inverter topologies. The comparison of THD of proposed topology to the various nine-level and seventeen level inverter topologies

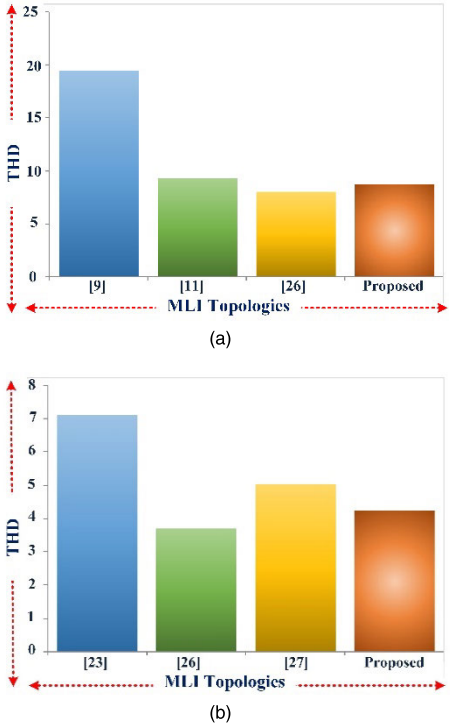

FIGURE 23. Comparison of THD (a) Proposed 9MLI with other topologies and (b) Proposed 17MLI and other similar topologies.

are shown in FIGURE 23(a) & (b). The proposed inverter is stable during nonlinear loads, and it is well suited for FACTS and renewable energy grid-connected applications. The proposed 17 level MLI analysis cost is carried out In TABLE 10. It requires fourteen IGBT's CM75DU-12H, which are incited by MCT2E opto-couplers and two capacitors.

VI. CONCLUSION

In this article, a hybrid Cascaded H-Bridge Multilevel Inverter with reduced components topology was presented. The proposed basic MLI builds a voltage with nine levels and extended to seventeen levels by cascading. This topology uses lesser power switches that reduce the price and volume of the inverter and improves efficiency. The proposed inverter requires relatively less power electronic components to generate the desired output than other similar topologies. Comparative analysis shows that the proposed topology has a superior cost factor per level. In the output, the proposed inverter's harmonic content is comparatively less than similar Cascaded H-Bridge MLI for both linear and nonlinear loads with nearly more efficiency η. The proposed inverter is stable during nonlinear loads, and it is well suited for FACTS and renewable energy grid-connected applications. To authenticate the proposed inverter satisfactory simulation is done in MATLAB/Simulink. The experimental setup is assembled in the laboratory confirmations unique with more significant output voltage levels, having lower harmonic content and reduced power switches, and greater efficiency. Subsequently

proposed inverter appears some encouraging properties when compared with various similar topologies.

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