Design of 5-3 multicolumn compressor for high performance multiplier

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Abstract: Compressors are widely used in multiplier to reduce the partial products. This paper proposed the design of 5-3 multicolumn compressor. The proposed 5-3 multicolumn compressor is used to design the various size multipliers. In this paper, we have designed 6 × 6, 8 × 8, 10 × 10 and 12 × 12 bit multiplier using proposed 5-3 multicolumn compressor, conventional 5-3 multicolumn compressor and conventional 4-2 compressor and compared the results. Simulation result shows that the proposed architecture consumes less power and provides more speed than conventional multicolumn 5-3 compressor and conventional 4-2 compressor. Cadence RTL compiler is used to obtain the results of multiplier.

Keywords: full adder; 5-3 multicolumn compressor; multiplier; energy delay product; EDP.

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1 Introduction

Multiplication is one of the frequently used arithmetic operations in microprocessors and digital signal processors (DSP). It is mainly used in digital signal processing to perform operations such as convolution, correlation and filtering. Multiplier is a circuit which is used to perform the multiplication operation. Multiplication is the complex operation which consumes most of the processing time and power. Minimising the latency of the multiplier is the challenging task for researchers. Several methods have been proposed by several researchers from the last two decade.

The multiplication process mainly consists of three steps. They are:

1 partial product generation

2 partial product reduction

3 final carry addition (Balamurugan et al., 2015; Wallace, 1964; Dadda, 1965).

AND gates are used to generate the partial products. Generation of partial product will not take much time. Optimising the partial product generation would not give better results. Partial product reduction stage takes considerable amount of processor power and it time consuming process. Generally, encoding techniques are used to reduce the partial product. In conventional multiplier, adders are used to reduce the partial product. Later, single column compressors are used to reduce the partial product. Several compressors have been proposed and used in multiplier (Ohsang et al., 2002; Veeramachaneni et al., 2007; Chang and Ahmadi, 2009; Nagdeve et al., 2012; Nirlakalla et al., 2011; Marimuthu et al., 2012, 2013a, 2013b; Bansal and Madhu, 2016; Momeni et al., 2015; Pishvaie et al., 2014). 5-3 multicolumn compressor is proposed Ohsang et al. (2002) and this compressor is used to reduce the partial product of the multiplier. This paper proposed the new design of 5-3 multicolumn compressor and result of this compressor is compared with conventional compressor. Parallel adders are used in final carry addition.

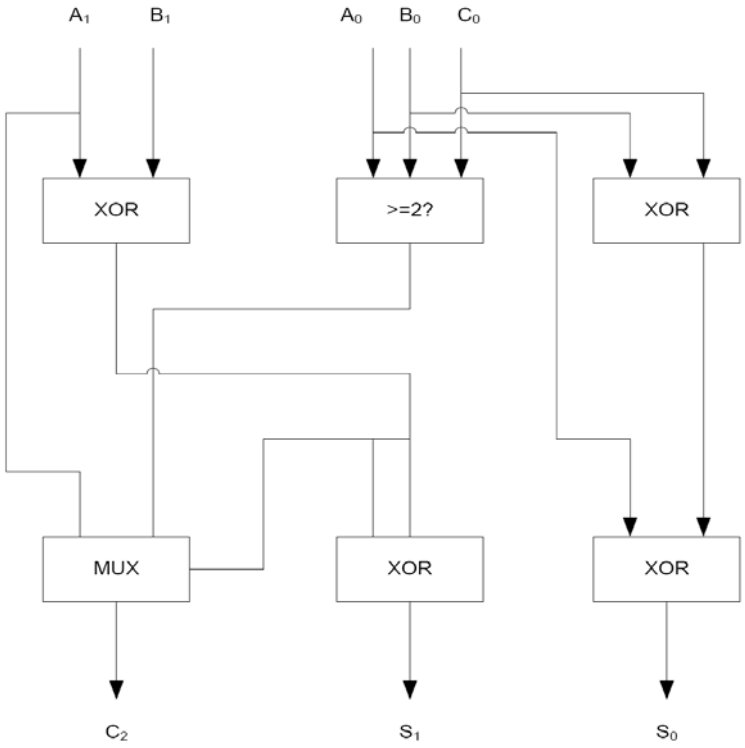
In this paper, Section 2 presents a conventional 5-3 multicolumn compressor. Proposed 5-3 multicolumn compressor is presented in Section 3. Design of multiplier using proposed compressor is described in Section 4. Section 5 describes the simulation results of various multipliers and finally conclusion is presented in Section 6.

2 Conventional 5:3 multicolumn compressor

Ohsang et al. (2002) proposed the conventional architecture of a 5-3 multicolumn compressor is shown in Figure 1. It consists of two full adders. From first column, partial products A_0, B_0, C_0 are used to generate S_0 and C_1. C_1, A_1 and B_1 are used to calculate S_1 and C2. Two XOR gates are required to generate S_0. Carry generation circuit is used to

calculate the C_1 (>=2?). Generation of S_1 requires two XOR gates and it needs to wait for C1. Multicolumn compressor is faster than single column compressor because in single column compressor four XOR gates are used to generate *sum*. Multicolumn compressor is faster because it requires only two XOR gates.

Figure 1 5-3 multicolumn compressor



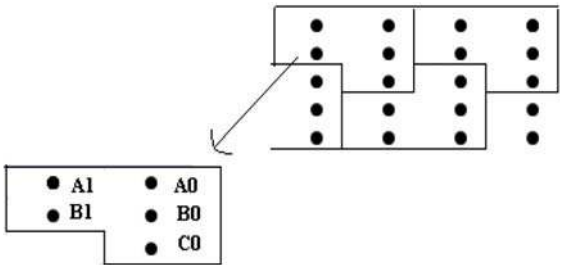
3 Proposed 5:3 compressor

Multiplier which is implemented by conventional multicolumn 5-3 compressor is considerably faster than 4-2 compressor which is proposed by Dandapat et al. (2010). But the power consumption is not reduced considerably. Proposed 5-3 multicolumn compressor is targeting both speed and power. Proposed structure of 5-3 multicolumn compressor is shown in the Figure 3. Multiplexers are used to implement the 5-3 multicolumn compressor.

Dot implementation of 5-3 multicolumn compressor from the partial product array is shown in Figure 2. Inputs for multicolumn 5-3 compressor are five partial products, three from first column and two from second column. It will compress these five partial products into sum_0, sum_1 and $carry_2$.

In this proposed architecture A_0, B_0, C_0 are partial products from a first single column. Similarly, B_0 and C_0 are given as control signals for 4-1 MUX and A_0 is given as an input signal. A_0, B_0 and C_0 are already available partial products. Generation of SUM_0 is done in a fast manner. B_0 and C_0 acts as control signal for generation of C_1.

Figure 2 Dot implementation of 5-3 multicolumn compressor



When B_0 and C_0 is (0, 0) or (1, 1), C_1 is always 0 or 1 respectively, which will reduce the toggling and results in less power consumption. C_1 is given as input to MUX to generate SUM_1 and $Carry_2$ where A_1 and B_1 are partial products from second column. A_1 and B_1 are given to 4-1 MUX as control signals. Sum_1 is generated as soon as C_1 is generated. Outputs of 5-3 multicolumn compressor are shown below.

$$Sum_0 = \left(A_0 \,\&\, \overline{B_0} \,\&\, \overline{C_0}\right) \left| \left(\overline{A_0} \,\&\, \overline{B_0} \,\&\, C_0\right) \right| \left(\overline{A_0} \,\&\, B_0 \,\&\, \overline{C_0}\right) \left| \left(A_0 \,\&\, B_0 \,\&\, C_0\right) \right. \tag{1}$$

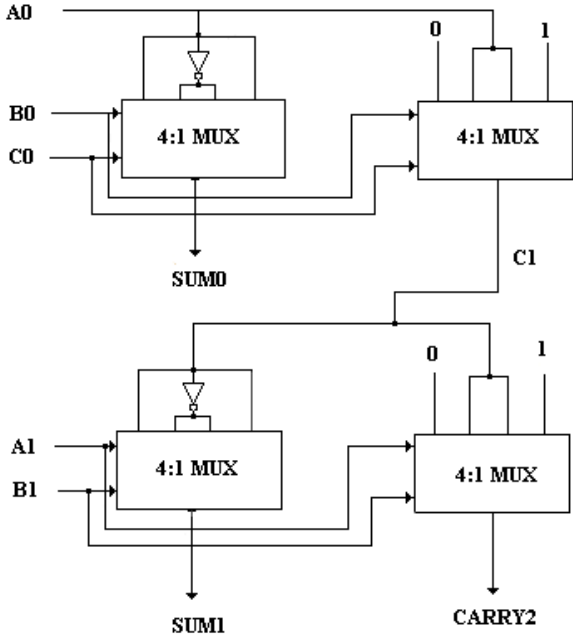
$$C_1 = \left(\text{zero} \,\&\, \overline{B_0} \,\&\, \overline{C_0}\right) \left| \left(A_0 \,\&\, \overline{B_0} \,\&\, C_0\right) \right| \left(A_0 \,\&\, B_0 \,\&\, \overline{C_0}\right) \left| \left(\text{one} \,\&\, B_0 \,\&\, C_0\right) \right. \tag{2}$$

$$Sum_1 = \left(C_1 \,\&\, \overline{A_1} \,\&\, \overline{B_1}\right) \left| \left(\overline{C_1} \,\&\, \overline{A_1} \,\&\, B_1\right) \right| \left(\overline{C_1} \,\&\, A_1 \,\&\, \overline{B_1}\right) \left| \left(C_1 \,\&\, A_1 \,\&\, B_1\right) \right. \tag{3}$$

$$Carry_2 = \left(\text{zero} \,\&\, A_1 \,\&\, B_1\right) \left| \left(C_1 \,\&\, \overline{A_1} \,\&\, B_1\right) \right| \left(C_1 \,\&\, A_1 \,\&\, \overline{B_1}\right) \left| \left(\text{one} \,\&\, A_1 \,\&\, B_1\right) \right. \tag{4}$$

where zero = gnd, one = vdd.

Figure 3 Proposed 5-3 multicolumn compressor



The truth table of proposed 5-3 compressor is given in Table 1.

Table 1 Truth table of proposed 5-3 multicolumn compressor

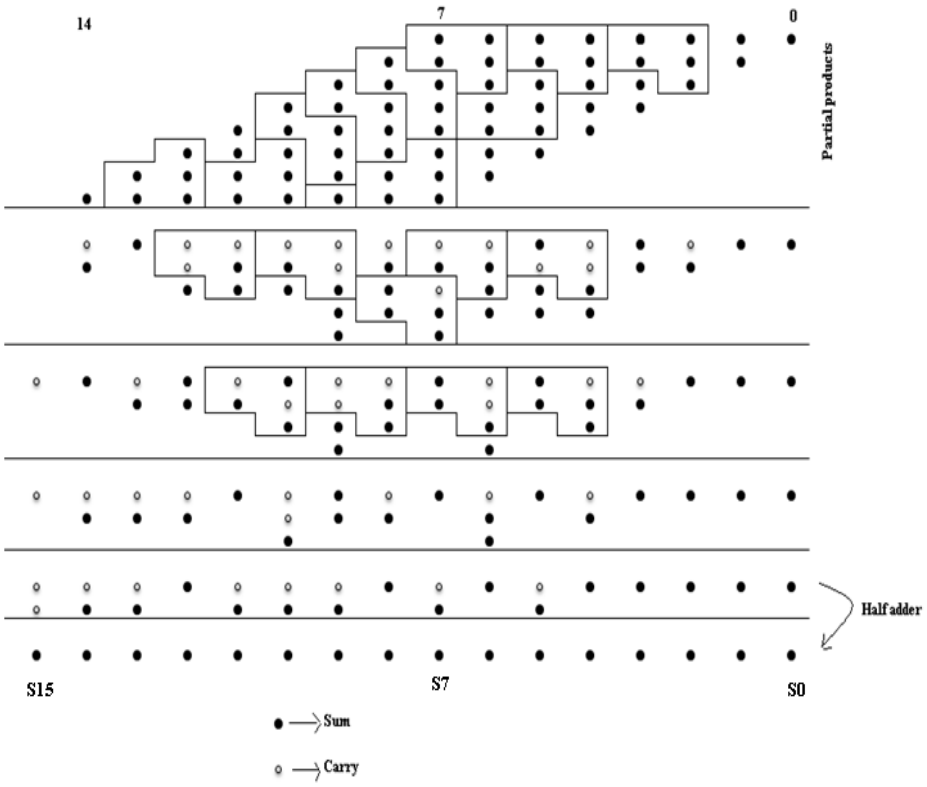
Inputs (A_0, B_0, C_0)	A_1	B_1	SUM_0	SUM_1	$Carry_2$
All the inputs are 0	0	0	0	0	0
Any one input is 1	0	0	1	0	0
Any two inputs are 1	0	0	0	1	0
All the inputs are 1	0	0	1	1	0
All the inputs are 0	0	1	0	1	0
Any one input is 1	0	1	1	1	0
Any two inputs are 1	0	1	0	0	1
All the inputs are 1	0	1	1	0	1
All the inputs are 0	1	0	0	1	0
Any one input is 1	1	0	1	1	0
Any two inputs are 1	1	0	0	0	1
All the inputs are 1	1	0	1	0	1
All the inputs are 0	1	1	0	0	1
Any one input is 1	1	1	1	0	1
Any two inputs are 1	1	1	0	1	1
All the inputs are 1	1	1	1	1	1

Proposed multicolumn 5-3 compressor is 3.4% faster than conventional multicolumn 5-3 compressor and also consumes 36.18% less power.

4 Multiplier design

Proposed 5-3 multicolumn compressor is used in various multipliers like 6 × 6, 8 × 8, 10 × 10 and 12 × 12 multiplier. The obtained results are compared with conventional 5-3 multicolumn compressor and 4-2 compressor proposed by Veeramachaneni et al. (2007). From the comparison, multiplier which is designed by proposed multicolumn 5-3 compressor consumes less power and its energy delay product (EDP) also reduced significantly. Dot diagram of an 8-bit multiplier using multicolumn 5-3 compressor is shown in Figure 4. Initially, generated partial products are compressed into sum and carry forms with the help of multicolumn 5-3 compressor. Dot diagram shows the use of 5-3 compressors in partial product reduction stage. Apart from compressors, half adders and full adders are also utilised.

Figure 4 Dot diagram of 8 bit multiplier using 5-3 multicolumn compressor



5 Simulation results

This section describes the simulation results of different multipliers. Verilog HDL code is written and functionality verification was done in Xilinx software. Simulation results are obtained with the help of Cadence RTL compiler. 90 nm technology typical library file is used in Cadence RTL complier. Random test vector is applied to multiplier to get the results. Multipliers that are implemented using proposed 5-3, existing 5-3 compressor proposed by Ohsang et al. (2002) and 4-2 compressor proposed by Maunika and Devi (2012) are compared and simulation results are shown in Table 2. 6 × 6 multiplier is implemented using proposed 5-3 compressor is 4.96% faster than existing multicolumn 5-3 compressor and power consumption is 19.91% reduced and EDP is reduced by 27.66%. Similarly, area overhead of proportional multiplier is 9.32 % and 12.93 % when

compare to conventional 5-3 compressor and 4-2 compressor respectively. For an 8 × 8 multiplier is 3.384% faster than existing multicolumn 5-3 compressor and power consumption is 17.43% reduced and EDP is reduced by 22.93%. Area overhead of proportional multiplier is 8.32 % and 11.23 % when compare to conventional 5-3 compressor and 4-2 compressor respectively. For a 10 × 10 multiplier is observed that power consumption is 22.20% reduced and EDP is reduced by 23.43%. Area overhead of proportional multiplier is 11.48 % and 13.16 % when compare to conventional 5-3 compressor and 4-2 compressor respectively. For 12 bit multiplier power consumption is 20.31% reduced and EDP is reduced by 20.4%. Area overhead of proportional multiplier is 11.62 % and 13.86 % when compare to conventional 5-3 compressor and 4-2 compressor respectively.

6 × 6 multiplier implemented by proposed 5-3 compressor is 16.02% faster, consumes 23.12% less power and EDP is reduced by 45.78% than multiplier implemented by 4-2 compressor. For an 8 × 8 multiplier, multiplier is 8.5% faster, consumes 23.97% less power and EDP is reduced by 36.34%. For 10 × 10 multiplier, multiplier is 9.84% faster, consumes 20.16% less power and EDP is reduced by 35.1%. For 12-bit multiplier, multiplier is 7% faster, consumes 19.93% less power and EDP is reduced by 30.76%.

Table 2 Simulation results of various multipliers

Multiplier size	*Compressors used in multiplier*	*Area (μm^2)*	*Delay (ns)*	*Power (pw)*	*EDP (10^{-20})*
6 × 6	Using 4-2 compressors	598.34	2,372	50,196	28.24
	Using conventional 5-3 compressor	623.25	2,096	48,186	21.169
	Proposed 5-3 compressor	687.25	1,992	8,589	15.312
8 × 8	Using 4-2 compressors	1,133.19	2,777	86,381	66.61
	Using conventional 5-3 compressor	1,166.35	2,630	79,543	55.019
	Proposed 5-3 compressor	1,276.25	2,541	65,673	42.403
10 × 10	Using 4-2 compressors	1,863.65	3,323	106,265	117.34
	Using conventional 5-3 compressor	1,905.82	3,020	109,054	99.46
	Proposed 5-3 compressor	2,145.73	2,996	84,840	76.153
12 × 12	Using 4-2 compressors	2,770.89	3,741	212,073	296.798
	Using conventional 5-3 compressor	2,842.86	3,481	213,061	258.174
	Proposed 5-3 compressor	3,216.89	3,479	169,789	205.503

6 Conclusions

The architecture of multicolumn 5-3 compressor is analysed. New multicolumn 5-3 compressor architectures have been proposed and implemented in different size of multipliers and also compared with the existing 5-3 architectures and 4-2 architecture. Simulations have been performed for different size of multipliers. Proposed multicolumn 5-3 compressor leads to 3.4% speed improvement and also observed with 36.18% less power consumption than conventional multicolumn 5-3 compressor. Performance of the proposed architecture is better than the existing ones in power, delay and EDP. Proposed

structure occupies more area than conventional. In future, researcher can work towards the minimising the area overhead. Also, design of higher order multicolumn compressors for large size multiplier would help to get better results.

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