

PAPER • OPEN ACCESS

Design of energy efficient carry lookahead adder using novel CSIPGL adiabatic logic circuit

To cite this article: Abhishek L Bhalerao *et al* 2020 *J. Phys.: Conf. Ser.* **1716** 012033

View the [article online](#) for updates and enhancements.

A promotional banner for the 240th ECS Meeting. The banner features a colorful striped border at the top. On the left, the ECS logo is displayed in a green circle. To its right, the text reads "240th ECS Meeting" in large blue font, followed by "Oct 10-14, 2021, Orlando, Florida" in a smaller blue font. Below this, it says "Register early and save up to 20% on registration costs" in bold black font, and "Early registration deadline Sep 13" in a smaller black font. At the bottom left, there is a red "REGISTER NOW" button. On the right side of the banner, there is a photograph of a diverse group of people in a professional setting, with a man in a white shirt and tie clapping and smiling.

Design of energy efficient carry lookahead adder using novel CSIPGL adiabatic logic circuit

Abhishek L Bhalerao, Aishwarya Mane, Kartik Pensenwar,

B P Bhuvana, A Anita Angeline and V S Kanchana Bhaaskaran*

School of Electronics Engineering, VIT, Chennai Campus, Chennai – 600 127.

Email: *kanchana.vs@vit.ac.in

Abstract. This paper presents a novel energy efficient logic called Charge Sharing Improved Pass Gate Adiabatic Logic (CSIPGL) operating using four phase power clock sources. The CSIPGL based circuit is capable of operating through a wider range of frequency from 100MHz to 1GHz. CSIPGL logic has been designed using UMC 90nm technology model files and are simulated using Cadence® Virtuoso EDA tools. Efficiency of CSIPGL circuit is validated by comparing it against CSSAL, SQAL, SyAL, adiabatic logic circuits based on single charge sharing transistor [14] and EE-SPFAL circuit designs. Power consumption of AND/NAND and XOR/XNOR sub modules used in the design of 4-bit Carry Lookahead Adder circuits (CLA) are compared. 4-bit CLA is taken as a benchmark circuit to validate the efficiency of the proposed CSCPAL circuit.

1. Introduction

In the last few decades, increasing demand in the usage of portable devices such as laptops, mobile phones and tablets have made the researchers focus on development of strategies that can reduce the overall power consumption of circuit. Plenitude of articles are found describing various low power circuit design practices. Conventional CMOS (Complementary Metal Oxide Semiconductor) circuits dissipate more energy during charging and discharging process. Also, the dynamic power consumption is a major concern to be considered as it depends on the switching activity of circuit. Adiabatic logic principle is a non-conventional technique that has the capability to achieve low power dissipation [1]. Adiabatic logic circuits are energized by a power clock source, which acts both as power supply and clock signal for synchronization purpose. This slow varying pulse can be either two phase sinusoidal power clock source or four phase trapezoidal power clock source. Utilization of power clock source in the design aids in constant current flow during charging and discharging processes. Some of the most common adiabatic logic circuits found in the literature are 2N2P [2], 2N2N2P [3], Positive Feedback Adiabatic Logic (PFAL) [4], Differential cascode Pre-resolve and Sense Adiabatic Logic (DCPAL) [5], Pre-resolve Sense Adiabatic Logic (PSAL) [6][7][8][9][10], Secured Quasi Adiabatic Logic (SQAL) [11], Symmetric Adiabatic Logic (SyAL) [12], Charge-Sharing Symmetric Adiabatic Logic (CSSAL) [13], adiabatic logic circuit based on single charge sharing transistor [14] and Energy-Efficient Secure Positive Feedback Adiabatic Logic (EE - SPFAL) [15]. In this paper, a novel Charge Sharing based Improved Pass Gate Adiabatic Logic (CSIPGL) has been proposed. Performance characteristics of the adiabatic circuits are evaluated by Cadence® Virtuoso simulations using UMC 90nm technology models. 4-bit CLA circuit has been designed to validate the efficiency of the proposed logic. The efficiency of the proposed logic is proven by comparing with single charge sharing transistor based adiabatic logic and EE-SPFAL structures.



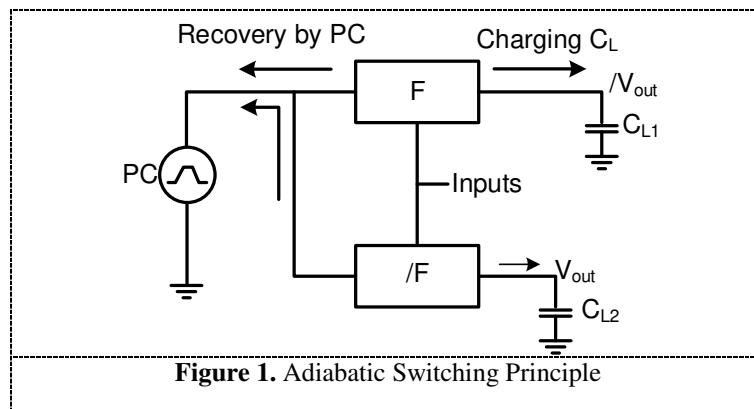
This paper is organized as follows. Section 2 describes the principle of adiabatic logic, Section 3 explains the operation of CSIPGL, Section 4 depicts the various adiabatic logic designs using CSIPGL and Section 5 presents the results and discussion and Section 6 concludes the paper.

2. Adiabatic Logic

Conventional CMOS circuits dissipate energy during the charging and discharging of output nodal capacitances through the pull up and pull-down networks. Energy dissipation in CMOS is given by

$$E_{\text{CMOS}} = \alpha \frac{1}{2} C_L V_{DD}^2 \quad (1)$$

Here, V_{DD} is the supply voltage, α is the switching factor and C_L is the output nodal capacitance.



Energy dissipation in conventional CMOS can be reduced by curtailing any one of the following factors, namely, 1) Reducing the nodal capacitances, 2) Reducing the number of transitions or 3) Supply voltage reduction, which can drastically reduce the energy of CMOS based circuits. However, it also degrades the speed and noise performance of the circuit. These limitations lead to the development of a new-fangled logic called *Adiabatic Logic* or *Energy Recovery Logic*, which is a non-conventional low power VLSI design technique. As mentioned earlier, Adiabatic logic utilizes a time varying voltage pulse as its power-clock, while the CMOS counterpart circuits use a constant voltage power supply. Each power-clock signal consists of four different phases of operation, viz. a) Evaluate Phase, b) Hold Phase, c) Recovery Phase and d) Wait Phase. Total energy consumption of an adiabatic circuit is given by

$$E_{AL} = 2 \left(\frac{RC_L}{T} \right) C_L V_{DD}^2 \quad (2)$$

where R is the resistance across the charging path and T is the transition time. Figure 1 shows the principle of adiabatic logic.

3. Proposed Novel Charge Sharing Improved Pass Gate Adiabatic Logic (CSIPGL)

Operation of the proposed Charge Sharing Improved Pass Gate Adiabatic Logic (CSIPGL) is presented in this section. Figure 2a and figure 2b depict the logic structure and input-output transients of CSIPGL. Let A and $/A$ be the input and its complementary input signals, OUT and $/OUT$ be the output and the complementary output, PC be the power clock source and CS be the charge sharing signal. Any desired logic function can be implemented in place of functional block (F) and its complementary functional block ($/F$).

During the WAIT phase, power clock source PC is constant at 0V. Input A slowly increases from 0V to V_{DD} and /A remains at 0V. CS signal is at V_{DD} . When the gate to source voltage of MN2 and MN4 is greater than the threshold voltage of the respective devices, they start to conduct. However, MN5 remains OFF with /A at 0V. During the evaluation phase, input A is HIGH at V_{DD} and /A is at 0V. Power clock source PC ramps up to V_{DD} . CS signal is disabled and hence MN3 is switched OFF. MN2 and MN4 are enabled as A is HIGH and this in turn causes OUT node to be connected with the ground. The voltage at OUT node is LOW which switch on MP2 transistor. During the HOLD phase, power clock PC remains stable at V_{DD} , charging process at the /OUT node continues and /OUT node follows PC.

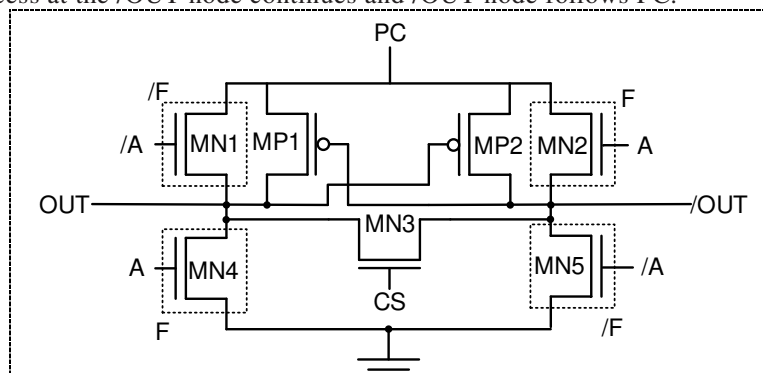


Figure 2a. Proposed CSIPGL circuit

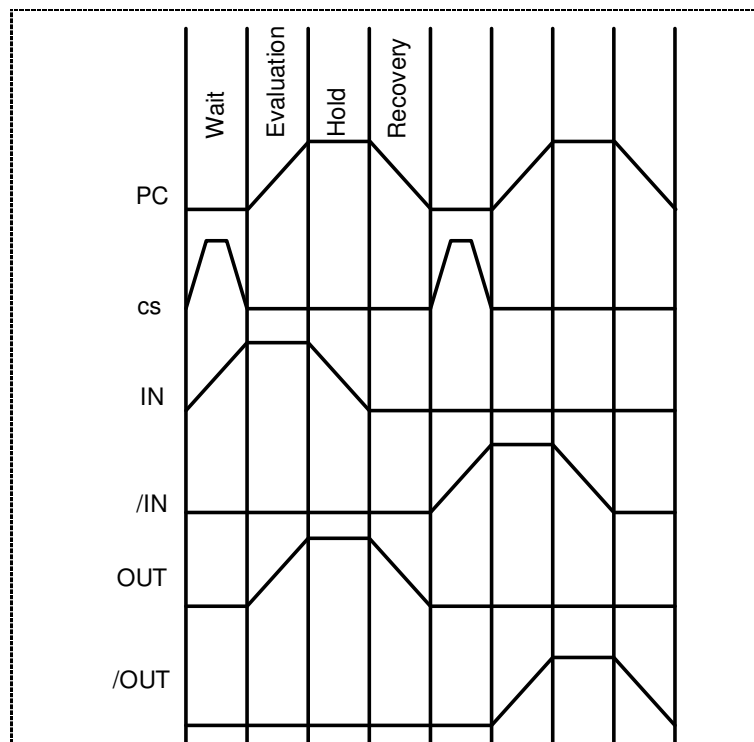
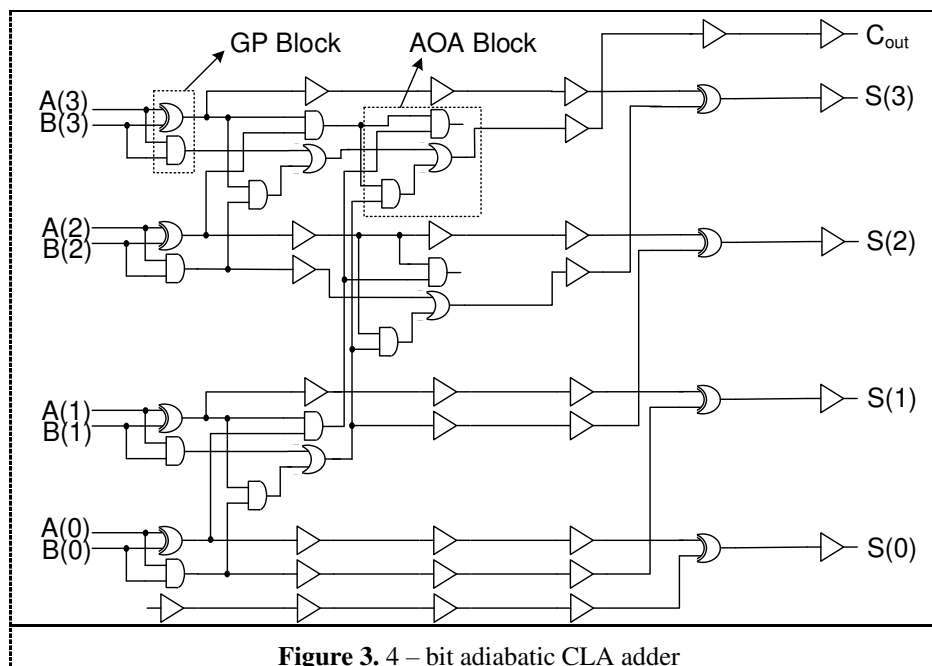


Figure 2b. Input – Output waveform transients of CSIPGL inverter circuit

During the recovery phase, inputs A and \bar{A} are at 0V. MN1, MN2, MN4 and MN5 are disabled. The charge deposited in the nodal capacitances of /OUT node are recovered to the PC through MP2 transistor. During the Wait phase of next cycle, when CS is enabled, depending upon the inputs, either A or \bar{A} input is switched ON. The corresponding transistor in the pull-up network recovers the left-over charge from the output nodal capacitances to PC and the transistors in the pull-down network provides a path for the trapped charges to ground.

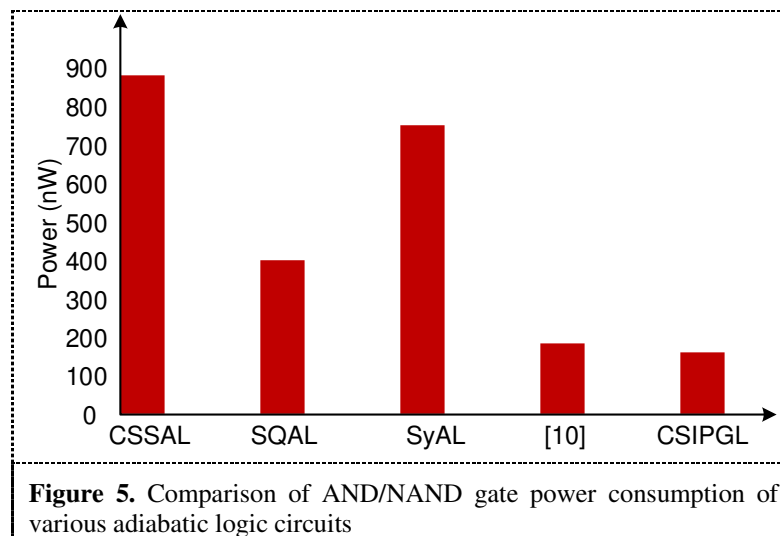
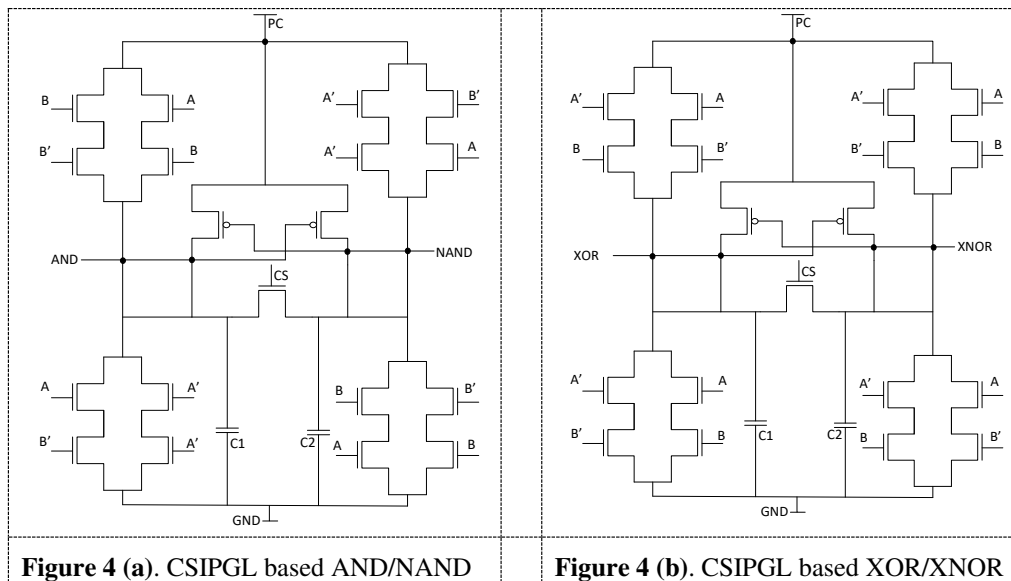
4. Design of 4-Bit Adiabatic CLA Circuit

The structure of a 4-bit adiabatic Carry Lookahead Adder (CLA) is shown in Figure 3. Major circuit modules in the CLA adder are AOA block (AND-OR-AND) and GP (Generate-Propagate) block. Generate propagate signal is expressed by $(A_i) = A_i.B_i$ and $(A_i) = A_i + B_i$. The carry bit computation is given by $C_{i+1} = G_i + (P_i.C_i)$. Consider $A(0), A(1), A(2), A(3)$ and $B(0), B(1), B(2), B(3)$ as inputs and the corresponding sum output bits are represented by $S(0), S(1), S(2), S(3)$ and carry bit as C_{out} . Figure 4a and Figure 4b shows the CSIPGL based AND/NAND and XOR/XNOR circuit structure which is used in the design of CLA adders.



5. Design of 4-Bit Adiabatic CLA Circuit

This Section validates the power efficiency of Charge Sharing Improved Pass Gate Adiabatic Logic (CSIPGL) circuit. UMC 90nm technology models are used for the design and simulation of all adiabatic logic circuits under considerations. Simulation environment considered for simulating circuits is Cadence Virtuoso[®] EDA tool. A nodal capacitance of 1fF is connected at the output nodes while simulating the circuits for emulating the fan-outs. A 4-bit CLA circuit is considered as a benchmark circuit for validating the efficiency of CSIPGL circuit. Average energy consumption of CSIPGL based 4-bit CLA is compared with EE-SPFAL and adiabatic logic circuit based on single charge sharing transistor based 4-bit CLA. Additionally, power efficiency of sub circuit components used in the design of CLA adder such as XOR/XNOR logic and AND/NAND logic are also investigated.



5.1. AND/NAND logic gate

Figure 5 shows the power consumption of AND/NAND gates designed based on CSSAL, SQAL, SyAL, adiabatic logic circuit based on single charge sharing transistor [14] and CSIPGL at an operating frequency of 500MHz with a supply voltage of about 1V. Power consumption of about 841.8nW, 381.2nW, 716.6nW, 174.4nW and 151.7nW is consumed by CSSAL, SQAL, SyAL, adiabatic logic circuit based on single charge sharing transistor [14] and CSIPGL circuits, respectively. Hence, it is clear that CSIPGL circuit is power efficient when compared with the prevailing circuit counterparts.

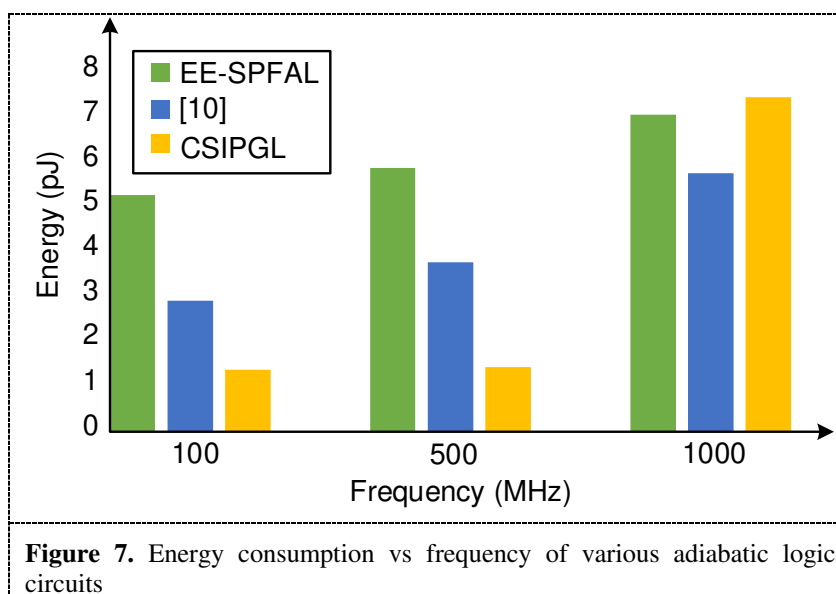
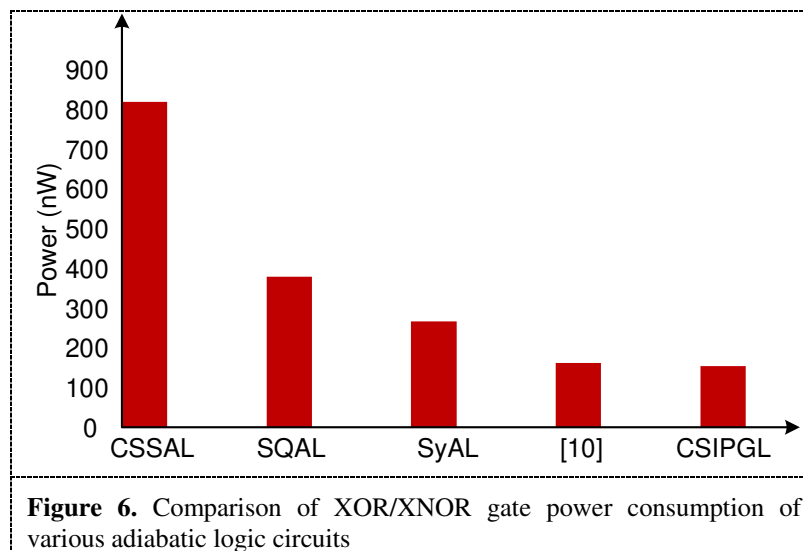
5.2. XOR/XNOR logic gate

XOR/XNOR logic circuit is designed using CSSAL, SQAL, SyAL, adiabatic logic circuit based on single charge sharing transistor [14] and CSIPGL circuits. These circuits are operated at a frequency of 500MHz at 1V supply voltage. Figure 6 depicts the power efficiency of the proposed circuit

CSIPGL. It is clear from the figure that CSIPGL consume very less power when compared with all other circuit counterparts.

5.3. 4-bit CLA

Brent Kung Carry lookahead adder is designed with the EE-SPFAL, adiabatic logic circuit based on single charge sharing transistor [14] and CSIPGL circuits. These circuits are operated at various frequency from 100MHz to 1GHz with a supply voltage of about 1V. Figure 7 depicts the energy comparison of CLA adder designed using the above said counterparts. EE-SPFAL and adiabatic logic circuit based on single charge sharing transistor [14] are considered for the design of 4-bit CLA as these are the most efficient circuits proposed so far in the literature. It is evident from the results that CSIPGL consumes lower energy than the above-mentioned counterparts. Also, CSIPGL is energy efficient at lower frequency and as frequency increases, the efficiency of CSIPGL is degraded. Hence, CSIPGL is best suited for low frequency applications.



6. Design of 4-Bit Adiabatic CLA Circuit

This paper validates the efficiency of CSIPGL circuit through the design of arithmetic architectures operating through a wide range of frequency from 100MHz to 1GHz. CSIPGL circuit reduces the floating nodal issues which are prevalent in the existing counterpart designs and thereby increasing the power efficiency. Performance of the proposed circuit is validated by the design of 4-bit carry lookahead adder designs. CSIPGL based 4-bit CLA is 73% and 52% more efficient than EE-SPFAL and adiabatic logic circuit based on single charge sharing transistor circuit operating at 100MHz frequency. CSIPGL circuit is proved energy efficient at low frequencies because of its superior energy recovery characteristics, lower leakage current and reduced number of transistors.

References

- [1] Teichmann P 2011 *Adiabatic logic: future trend and system level perspective* Springer Science & Business Media 34.
- [2] Kim S, Ziesler C H and Papaefthymiou M C 2005 Charge-recovery computing on silicon. *IEEE Transactions on Computers* **54**(6) 651-659.
- [3] Kramer A, Denker J S, Flower B and Moroney J 1995 2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits. *Proceedings of the 1995 international symposium on Low power design* pp.191-196.
- [4] Vetuli A, Pascoli S and Reyneri L M 1996 Positive feedback in adiabatic logic *Electronics Letters* **32**(20) pp.1867-1869.
- [5] Kanchana Bhaaskaran V S and Raina J P 2008 Differential cascode adiabatic logic structure for low power *Journal of Low Power Electronics* **4**(2) pp.178-190.
- [6] Kanchana Bhaaskaran V S and Raina J P 2012 Pre-resolve and sense adiabatic logic for 100 KHz to 500 MHz frequency classes *Journal of Circuits, Systems, and Computers* **21**(05) 1250045.
- [7] Kanchana Bhaaskaran V S and Raina J P 2010 Two-phase sinusoidal power-clocked quasi-adiabatic logic circuits *Journal of Circuits, Systems, and Computers* **19**(02) 335-347.
- [8] Sasipriya P and Kanchana Bhaaskaran V S 2018 Design and Analysis of Clocked CMOS Differential Adiabatic Logic (CCDAL) for Low Power *Journal of Low Power Electronics* **14**(4) 548-557.
- [9] Bhuvana B P and Kanchana Bhaaskaran V S 2019 Design of FinFET-based Energy Efficient Pass-Transistor Adiabatic Logic for ultra-low power applications *Microelectronics Journal* 92 104601.
- [10] Kanchana Bhaaskaran V S 2010 Energy recovery performance of quasi-adiabatic circuits using lower technology nodes *India international conference on power electronics* pp.1-7.
- [11] Avital M, Dagan H, Levi I, Keren O and Fish A 2014 DPA-secured quasi-adiabatic logic (SQAL) for low-power passive RFID tags employing S-boxes *IEEE Transactions on Circuits and Systems I: Regular Papers* **62**(1) 149-156.
- [12] Choi B D, Kim K E, Chung K S and Kim D K 2010 Symmetric adiabatic logic circuits against differential power analysis *ETRI journal* **32**(1) 166-168.
- [13] Monteiro C, Takahashi Y and Sekine T 2013 Charge-sharing symmetric adiabatic logic in countermeasure against power analysis attacks at cell level *Microelectronics Journal* **44**(6) 496-503.
- [14] Raghav H S and Kale I 2019 A balanced power analysis attack resilient adiabatic logic using single charge sharing transistor *Integration* **69** 147-160.
- [15] Kumar S D, Thapliyal H and Mohammad A 2016 EE-SPFAL: A novel energy-efficient secure positive feedback adiabatic logic for DPA resistant RFID and smart card. *IEEE Transactions on Emerging Topics in Computing* **7**(2) 281 – 293.