

Design of Low Power and Area Efficient 4-bit Arithmetic and Logic Unit using Nanoscale FinFET

Deshpande Akshay, Sanidhya Mohan Sharma, Lochan Anil Vyas and K. Sivasankaran*

School of Electronics Engineering, VIT University, Vellore, Tamil Nadu, India;
ksivasankaran@vit.ac.in

Abstract

In order to strive in VLSI Technology, we have to keep up with the Moore's law which states that in every 18 month number of transistors gets doubled on a chip. But as we scale down the transistor size problems like Short Channel Effects (SCE), Sub-threshold voltage variation, Drain Induced Barrier Lowering (DIBL), Gate oxide tunnelling leakage etc., comes into the account. To overcome the above problems we moved towards the FinFET based transistor. In this paper we have proposed the "Design of Low power 4-bit arithmetic & logic unit using nanoscale FinFET". Arithmetic Logic Unit (ALU) is the backbone of any processor, we have performed the logical operations like AND, OR, Inverter, 2's complement of the number etc. & Arithmetic operation like addition, subtraction, multiplication, parity generation etc. Different techniques are used to achieve the low power on different modules in the design.

Keywords: Adder, ALU, FinFET, SCE, Transmission Gate

1. Introduction

To strive in VLSI world we have to scale down the transistor size. But as we shrink down the channel length the gate loses the control over channel and hence Short Channel Effects (SCE's) come into the picture. SCE introduces the Drain Induced Barrier Lowering (DIBL), static power dissipation, gate oxide tunnelling leakage, sub-threshold voltage variation¹. To overcome these problems we move towards the Double Gate FinFET (DG-FinFET) transistor, which has two gates to control the channel. So gate acquires better control over channel and SCE's can be minimized².

The DG-FinFET is characterized by height (H) and Thickness (T) of the fin, ratio of height and thickness defines the aspect ratio of the DG-FinFET. The typical aspect ratio is 3:1. [Ref] We are using 30nm technology DG-FinFET model provided by Berkeley Simulator (BSIM). We have attached the transistor model to the Cadence Virtuoso environment by some predefined

procedure. The symbolic representation DG-FinFET is as shown in Figure 1.

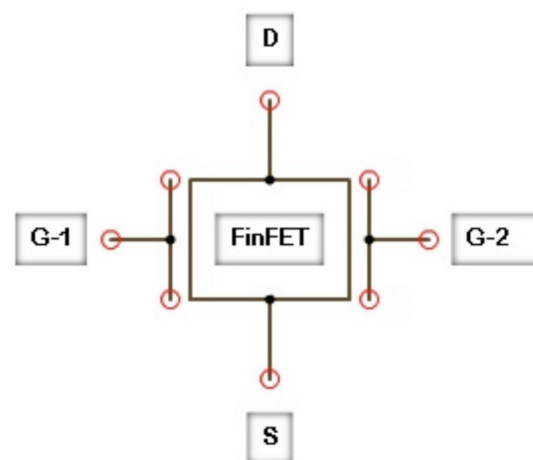


Figure 1. DG-FinFET symbol.

Many works have been carried out on the design of ALU³. In this paper we have proposed different design

* Author for correspondence

techniques for a low power 4-bit ALU using DG-FinFET. ALU will perform following operations on 4-bit operands. The paper is organized as follow: Section 2 describes related work, section 3 is dedicated to ALU and its working and we will discuss results in section 4 followed by conclusion and references.

2. Related Work

The performance of ALU can be enhanced for features like power and area by optimising standard cell blocks. When we compare the performance of static CMOS style standard cell with other logic style standard cells, static CMOS style outperforms other logic styles⁴, when it comes to AND, OR, NOT cells. Hence the usage of these cells with static CMOS style in this paper has been encouraged.

In the case of full adder, static CMOS style has transistor count of 58, which causes increment in area. For pass transistor logic style, degraded output has been

experienced since NMOS transistor and PMOS transistor passes '1' and '0' respectively⁴. Hence our focus has been shifted towards transmission gate construction so as to overcome the degradation obtained at the output. The proposed design for Full-Adder has a transistor count of 18 which extensively helps in reduction of area and power consumption. This has been achieved by implementing the construction of EX-OR using transmission gate logic^{5,6}. Also, design for 'carry' logic has been improvised which has further benefited the entire design in terms of area and power consumption. Hence non-degraded output has been achieved. The circuit design has been shown in Figure 2.

Multiplexer is always considered as an extensive unit for an ALU design. Hence optimisation of multiplexer is done precisely so as to achieve low power consumption and area-efficiency. The proposed 2X1 multiplexer is designed using transmission gates which give the non-degraded output without any trade-off in terms of area usage and power consumption⁷. The circuit design implemented has been shown in Figure 3.

Multiplexing of adder and subtractor will help to achieve an area efficient design. As summation and difference will produce same output, we need to multiplex

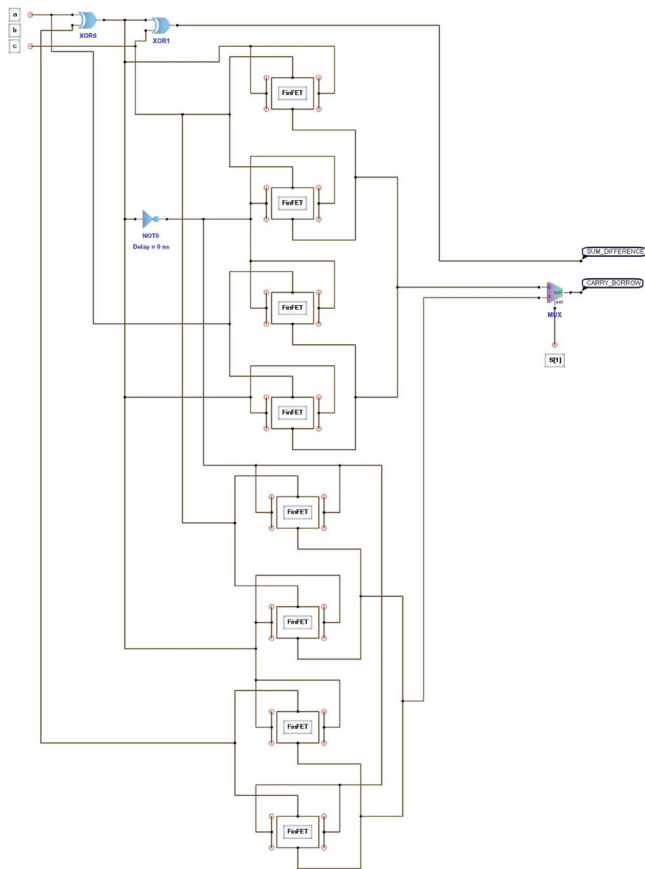


Figure 2. Full adder.

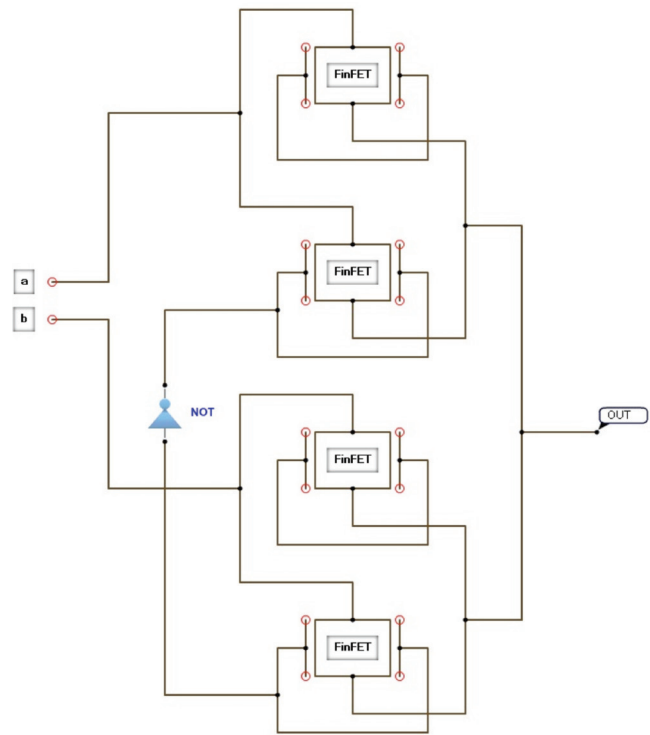


Figure 3. 2:1 multiplexer design.

carry and borrow. Proposed design consists of one 2:1 MUX which will produce the carry or borrow according to selection input. Again, this has helped in obtaining area efficient and low power consumption design.

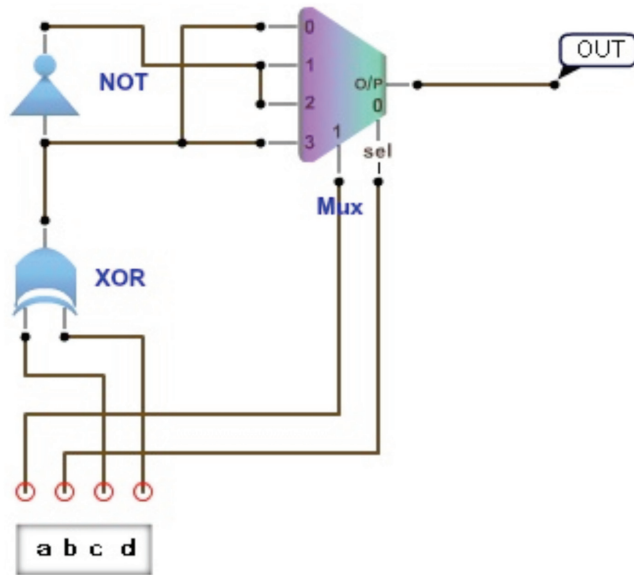


Figure 4. Even Parity Generator.

Proposed parity generator has one 4:1 MUX, EX-OR gate and inverter as shown in Figure 4. This circuit generates even parity which can be used to detect any error if present in the received message. Due to this improvised design with respect to the traditional design, low power has been achieved. Traditional approach has been used for the designing of multiplier which consists of the proposed full adder and static CMOS style half adder.

3. ALU and Its Working

Architecture of ALU as depicted in the Figure 5. The ALU performs the 4-bit operations on operands⁸. The ALU consists of eight 4X1 MUXs and to multiplex the outputs of these 4X1 MUXs, four 2X1 MUXs are used for the selection of the required operation which is to be performed. To select any one among the eight operations, three selection lines have been used. Out of these eight operations, four are logical operations and the remaining four are arithmetic operations. The MSB of select line (S_2) chooses whether the operation to be performed is arithmetic type or logical type.

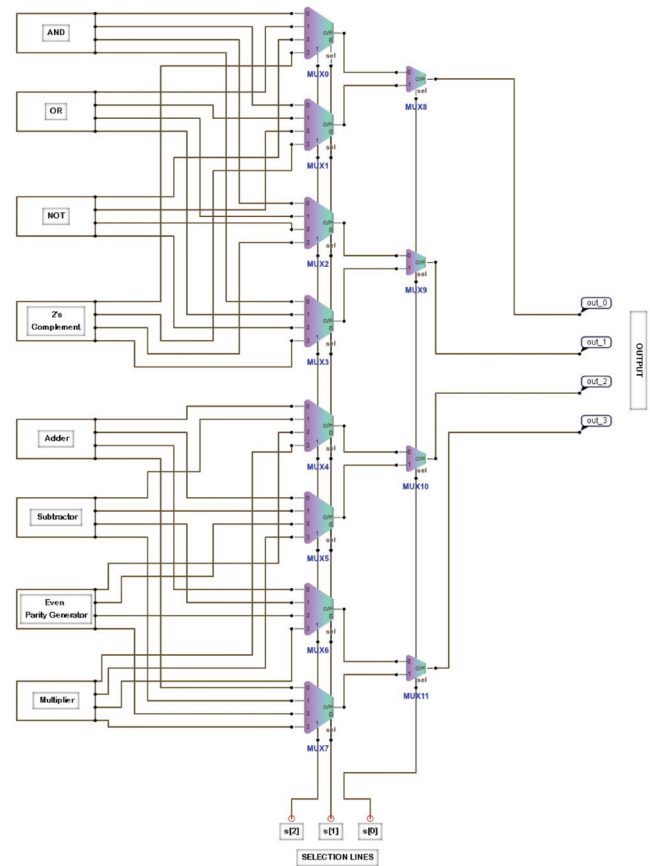


Figure 5. ALU Architecture.

The remaining 2-bits of select lines (S_1, S_0) specifies the operation after choosing between arithmetic and logical. The operations performed and their respective binary combination is tabulated below.

4. Discussion

Due to the degraded output that used to be one of the greatest trade offs during implementation of pass transistor logic, the change in logic style from pass transistor logic style to transmission gate logic style has prevented the degrading of the output. Given below are the simulation results which depict the non-degrading output. Figure 6 shows operation of adder and subtractor in which the outputs of summation or difference are same. Also the carry and borrow are depicted with different outputs.

Figure 7 depicts the operation of 4:1 MUX in which two select lines selects the input to obtain the desired output.

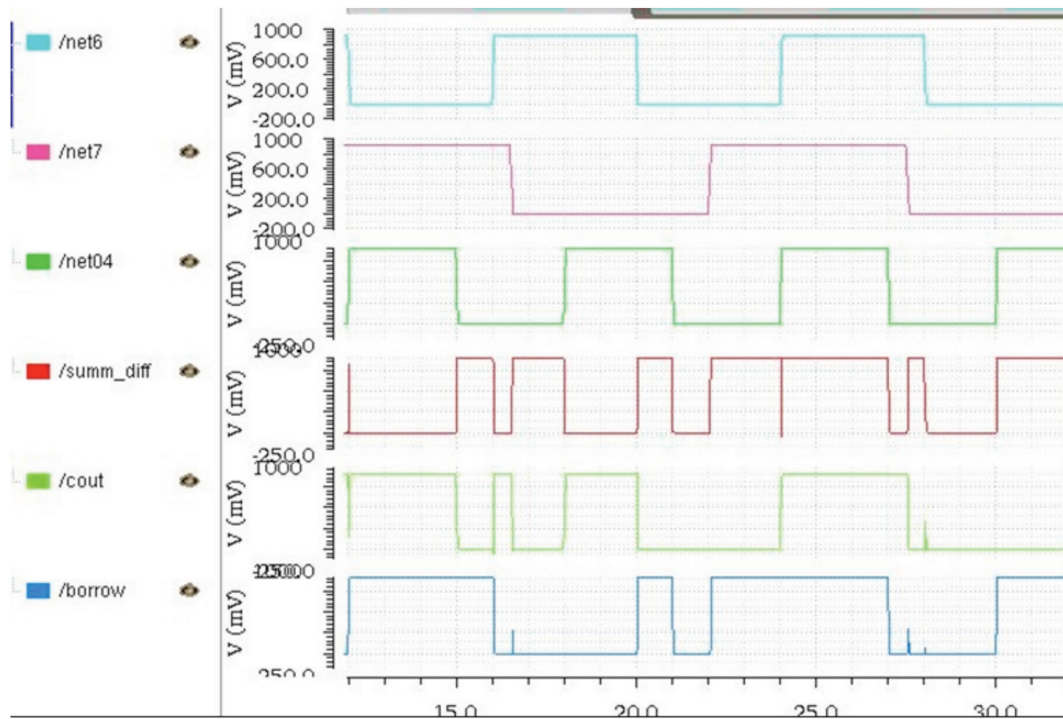


Figure 6. Output waveform for Addition & Subtraction

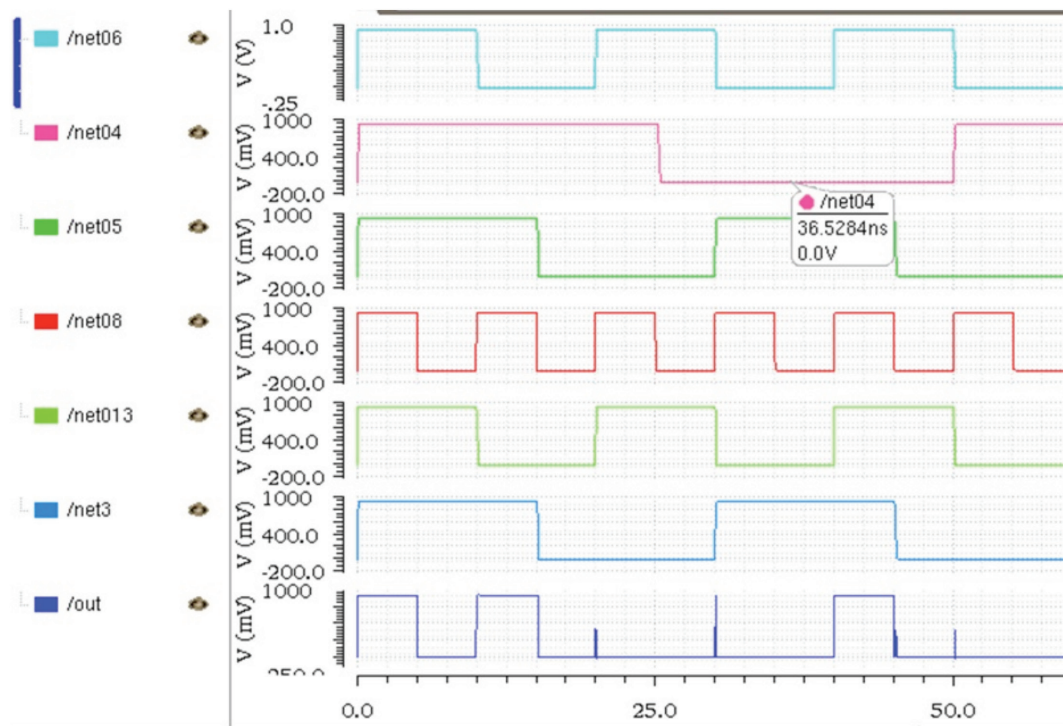


Figure 7. Output waveform for 4:1 multiplexer

Figure 8 depicts the operation of even parity generator in which produces high output if the number of ones in the input is odd and vice versa.

Figure 9 shows the final output of the ALU. It is the control circuit for the entire ALU operation and performs the operation according to the select input. From the

above given simulation results we can conclude that along with obtaining non-degrading outputs, area efficiency and low power consumption can be achieved too. Hence the proposed designs are effective and can be used for low power and low area usage designs. Comparison has been made in terms of power and delays between proposed

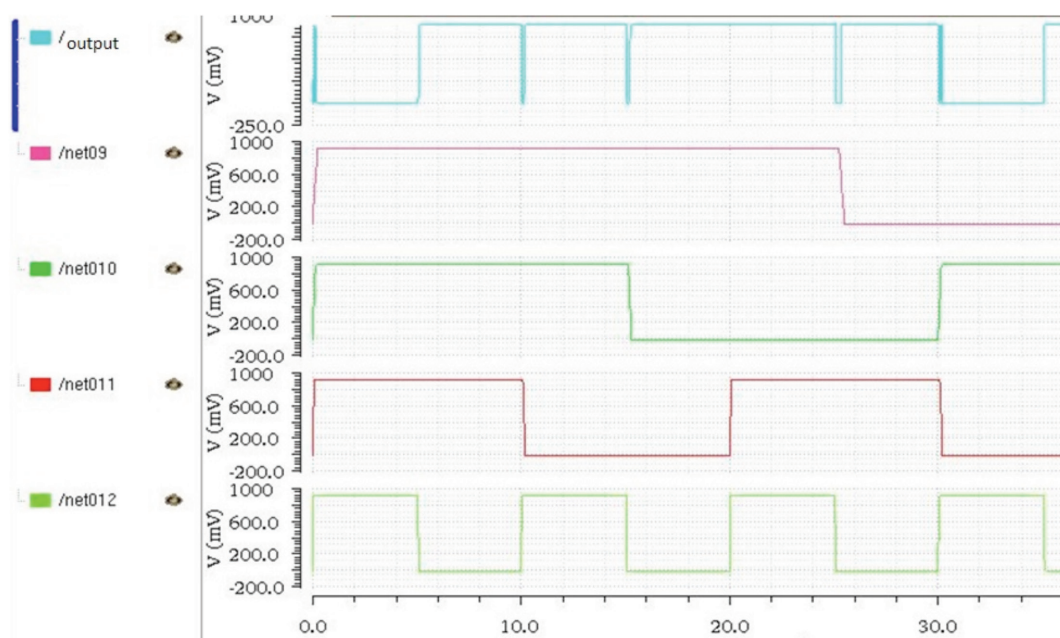


Figure 8. Output Waveform Even Parity Generator

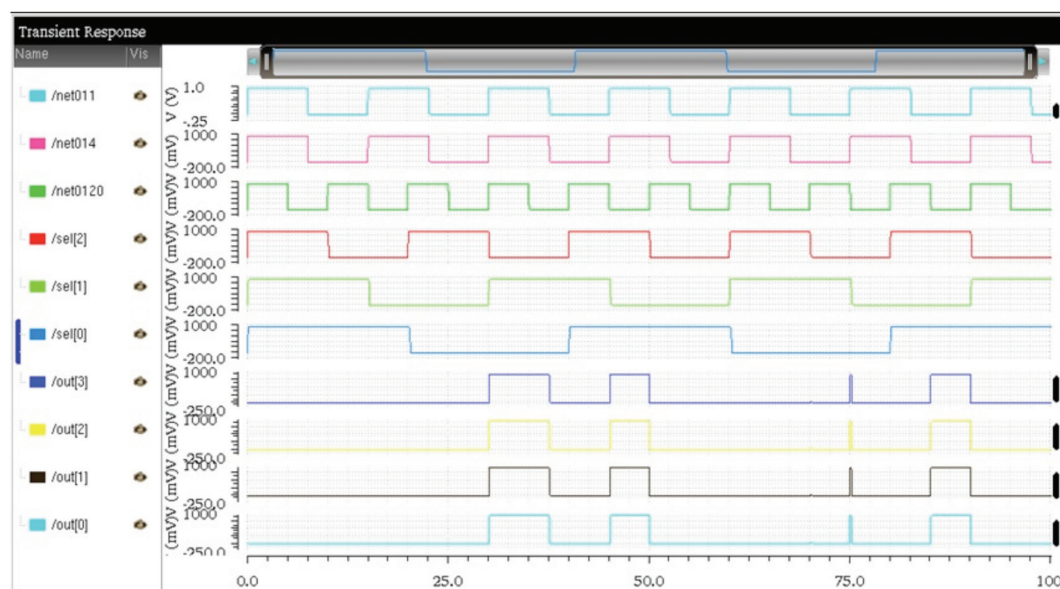


Figure 9. Output waveform for ALU block

ALU with respect to standard CMOS ALU & following observations have been noted^{3,9}

5. Conclusion

The design of 4-bit ALU has been implemented by categorising it into different blocks as discussed earlier. Every block in ALU is individually optimised to achieve low power and area efficiency. The design of 4-bit ALU is based on 30nm technology using DG-FinFET's. The area optimization of ALU is achieved by decrementing the number of transistors for different operation implementation. We have proposed new designs for Adder, Subtractor and Parity Generator which have been successfully simulated and have obtained non-degradable results. We have achieved considerable power reduction area efficient.

Table 1. Different Operation performed by ALU

Logical	Arithmetic
• AND	• Addition
• OR	• Subtraction
• NOT	• Multiplication
• 2's Comp	• Parity Generator

Table 2. Operation of ALU

S2	S1	S0	Operation
0	0	0	AND
0	0	1	OR
0	1	0	NOT
0	1	1	2'S COMPLEMENT
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	PARITY GEN.
1	1	1	MULTIPLICATION

Table 3. Power comparison between proposed ALU and standard CMOS ALU

Operation	Power (Proposed Design)	Power (Standard CMOS ALU)
AND	12.48nW	24nW
OR	14.36nW	21.66nW
NOT	2.26nW	14.22nW
2'S COMPLEMENT	22.14nW	-
ADDER	10.71nW	16.675uW
ADDER-SUBTRACTOR	15.69nW	-
PARITY GENERATOR	8.1nW	-

Table 4. Delay comparison between proposed ALU and standard CMOS ALU

Operation	Delay (Proposed Design)	Delay (Standard CMOS ALU)
AND	23.42ps	58.5ps
OR	597ps	32ps
NOT	4.99ps	10.1ps
2'S COMPLEMENT	14.9ns	-
ADDER	2.43ns	26ns
ADDER-SUBTRACTOR	4.89ns	-
PARITY GENERATOR	6.27ns	-

Table 5. Number of transistor used for proposed design

Operation	Number Of transistors for proposed design
ADDER	18
ADDER-SUBTRACTOR	22
PARITY GENERATOR	24
2:1 Multiplexer	6

6. References

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