Design of Low Power SRAM Cell Using Adiabatic Logic

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Abstract. In VLSI system design power consumption and energy dissipation are become more important. To optimize the power consumption we are using adiabatic logic which is having capability of reusing power. In this paper we proposed novel 7T SRAM cell using MCPL adiabatic logic. We compared the performance of energy dissipation and power consumption of conventional 7T SRAM and adiabatic SRAM. Furthermore, the conventional 6T,7T SRAM cell and the designs which are related are designed using FINFET devices to achieve low power.7T SRAM is more stable compared to 6T SRAM but due to excess transistor in 7T SRAM the power consumption will be more. SRAM cells are designed in cadence EDA environment and layouts for these circuits are carried out in cadence Assura tool.

1. Introduction

Now a days, while designing a very large scale integrated circuits power dissipation is the main concern. VLSI circuits leads to the increase in the density of transistors and decrease in size of devices. Several researchers have presented various techniques to reduce the power dissipation some of the low power techniques are reducing the supply voltage, scaling the devices etc. Mainly we concentrated on memories because memory arrays occupy a large part of the area on the chips [1]. To design a SRAM cell using conventional CMOS employ DC source. The energy consumption in conventional circuits consists of dynamic charging and discharging of node capacitance, because of the switching activity in the circuit there exists a direct path from rail to rail connection for a short duration of time and this leads to the short circuit power consumption and the leakage power consumption. To reduce this power consumption SRAM cell is designed using adiabatic logic. Conventional CMOS circuits use dc power supply whereas adiabatic circuit uses AC power supply. Several literatures have presented on different type of adiabatic logics are DCPAL,PFAL,2N2P,2N2NP,ECRL [2].

In this paper SRAM is designed with various logics in order to increase the performance of the design in terms of power and energy.6T SRAM cell, 6T SRAM cell using MCPL, 6T SRAM cell using transmission gates and similarly 7T SRAM cell are designed using CMOS and FINFET devices. Section 1 brief about the SRAM cells and adiabatic logic. Literature survey is discussed in section 2. Section 3 describes about working principle of SRAM cell, and MCPL SRAM cell. Section 4 explains the operation of SRAM cells using FINFET devices. Section 5 presents the simulated graphs and analyzes the results. Section 6 gives information about future work concludes the paper.

2. Literature Survey

Nakata Shunji [3] presented a design of single bit line SRAM with a reduced voltage during read operation. In their paper they discussed about the static noise margin of an adiabatic SRAM with dual bit line voltages has less SNM compared to the single bit line voltage SRAM. The SNM can be increased in single bit line voltage SRAM if the bit line is not precharged to Vdd [3]. Sense amplifier is designed with some adiabatic logics like 2N2N,2N2N2P,PFAL and the performance is analyzed.

These are Quasi adiabatic logic circuits operated with four phase sinusoidal clock [4]. FINFET based SRAM is designed with 45nm and 32nm technologies with a controlled voltage(Vt) to reduce the power and stability of noise margin is compared with the design of existing SRAM [5].

3. SRAM CELLS USING CMOS DEVICES

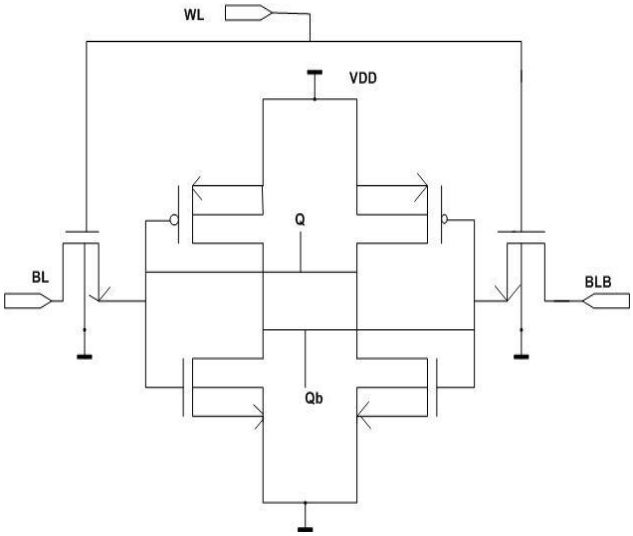

Figure 1. 6T SRAM cell.

The Figure 1 shows the schematic of conventional 6T SRAM, while Figure 2 presents the circuit diagram of 6T SRAM with MCPL logic. On the otherhand, Figure 3 presents the schematic of the proposed 7T SRAM which is structurally equivalent to the 9T SRAM. During write operation if the word line (WL) is activated it enables the NMOS pass transistors of the cell then the data in the BL and BLB will be stored in latch. If logic zero is applied to the word line (WL) then there is no connection between the latch and BL or BLB lines. The latch consists of two cross coupled inverters. When there is no connection existing between the latch and bit lines then the data remain in the cross coupled inverters of SRAM cell. During read mode it reads the values which are already present in the memory. BL and BLB lines acts as output and these are pre charged to the supply voltage. Now, let us consider Q=1 & QB=0 then there exists a voltage difference between the BLB and QB line. Hence BLB starts discharging and this voltage difference is read by sense amplifier which is connected between the BL and BLB lines. This sense amplifier acts as a comparator.

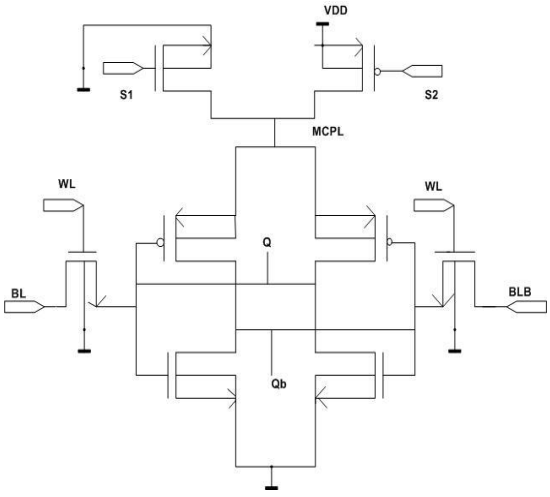

Figure 3. 7T SRAM cell with MCPL.

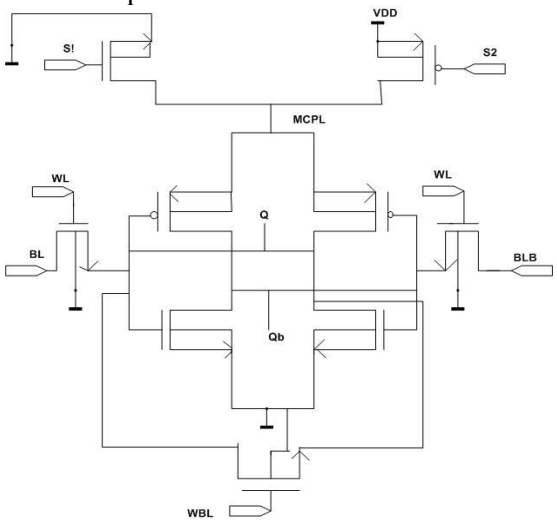

Figure 2. 6T SRAM cell with MCPL.

MCPL logic there is no constant power supply like conventional SRAM. There are two switches namely S1 & S2 in the Figure 2 and Figure 3. The PMOS with S1 is connected in between the power line VDD and MCPL, whereas the NMOS with S2 is connected in between the ground and MCPL. The S1 and S2 are the control signals used to control the MCPL node. Based on the operation of S1 and S2 the MCPL node has either VDD, ground or a floating node. When the S1 and S2 are off, the PMOS is ON and the MCPL follows the VDD. When the S1 and S2 are on then the MCPL follows the GND as NMOS is ON. When S1 is ON and S2 is OFF then, both the NMOS and PMOS are off hence the MCPL node is floating. Then the charge coming from the bit lines through the cross coupled inverters are used to charge the node MCPL. During write mode of operation, the BL (Bit Line) is gradually charged after the control signals S1 is ON and S2 is OFF then Q node follows the BL. The MCPL is already in floating mode. When Q is charged to HIGH the P1 is OFF and N1 is ON. Similarly, the Qb is LOW then P2 is ON and N2 is OFF. Now there is a path for charge to flow from Q node to MCPL through P2.
During the read mode of operation, the control signals are given as S1 and S2 are OFF, then the SRAM works as tradition 6T SRAM with MCPL as the Power rail VDD.

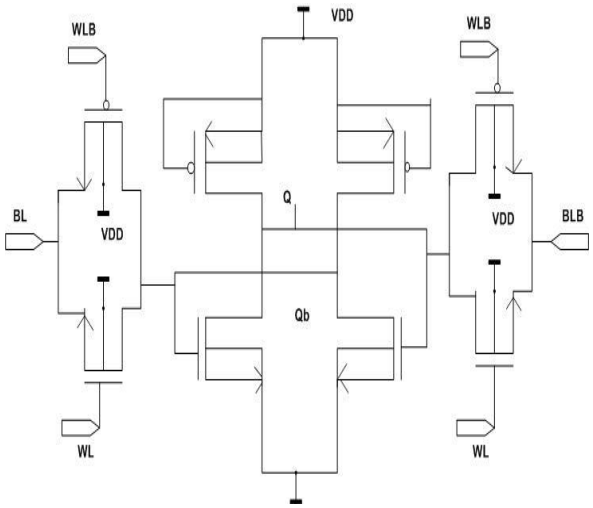

Figure 4. SRAM cell with Transmission gates.

The Figure 4 represents the 6T SRAM with transmission gates. Here in the memory cell pass transistors are replaced with the transmission gates. Transmission gates are used because of its simplicity. The modified SRAM cell drives the trapezoidal word line and bit signals to use adiabatic logic in the cell. The SRAM cell design with transmission gates give the better performance compared to MCPL SRAM cell.

4. SRAM CELLS USING FINFET DEVICES

The structure and working principle of CMOS based SRAM cells are already discussed in the previous section. There are two types of FINFET devices are available namely Independent gate FINFET and Shorted gate FINFET. In this paper we prefer to use Shorted gate FINFET (SG). In SG FET the pins gate(g) and enable(e) are connected together and termed as single gate. It has FIN type structure, hence there exists a small channel. In FINFET devices Power dissipation is less compared to CMOS devices because of its channel length. In CMOS devices the leakage current and short channel effects will be more. Transistor sizing has been done here in order to get the perfect read and write specifications of the memory cell.

5. SIMULATION RESULTS

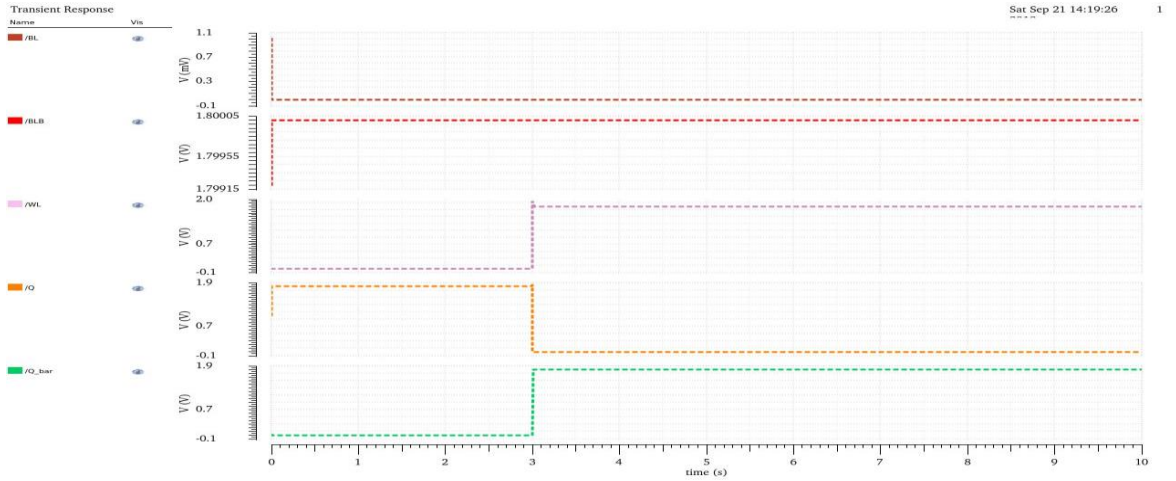

Figure 5. Write operation of SRAM cell.

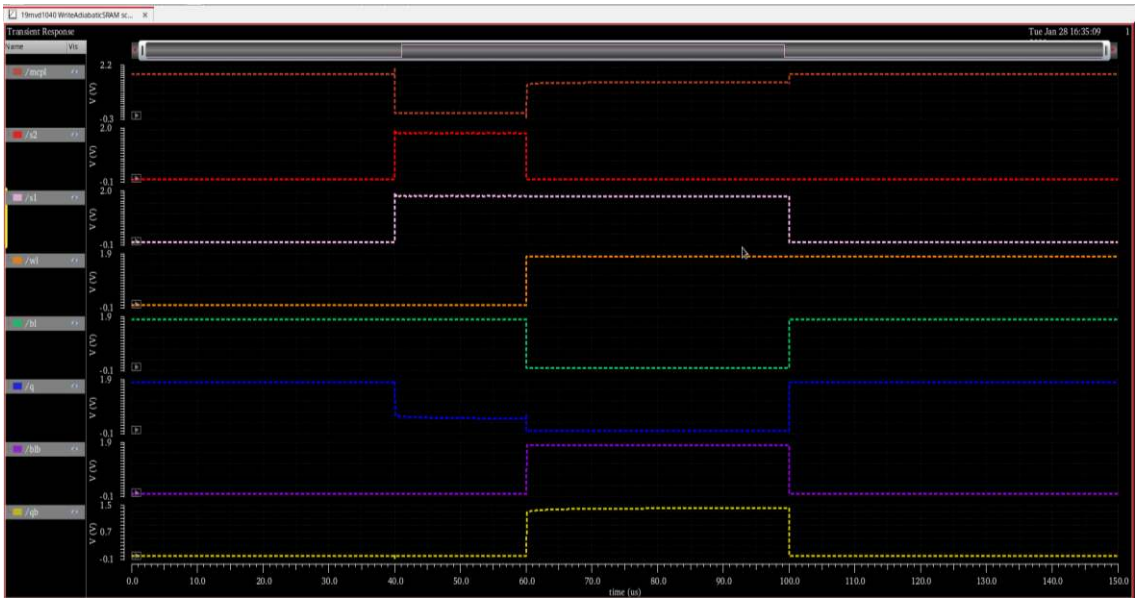

Figure 6. Write operation of SRAM cell with MCPL.

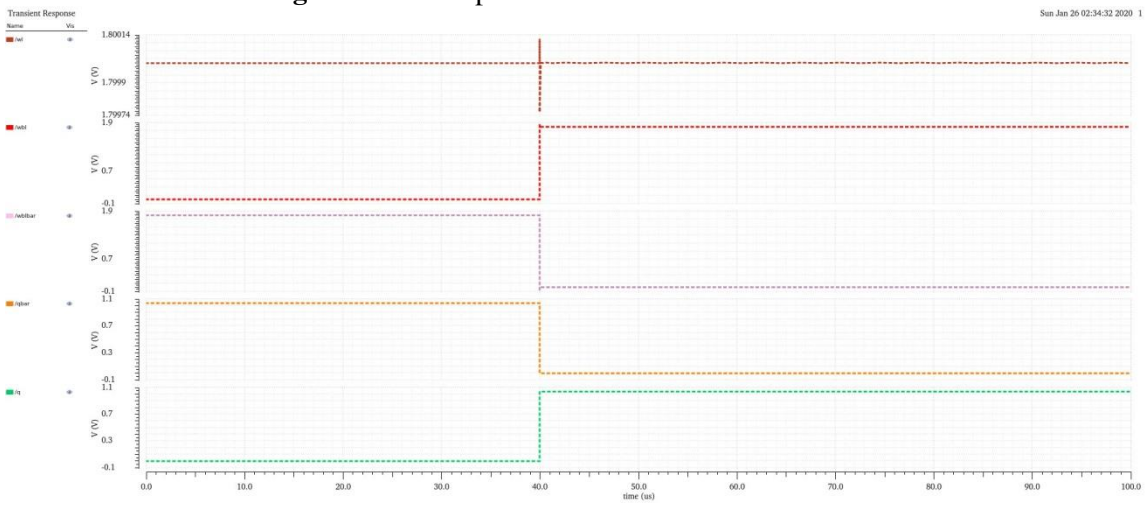

Figure 7. SRAM cell with transmission gates.

Simulation results are obtained using cadence virtuoso. Figure 5 shows the write operation of the proposed SRAM cell. By observing Figure 5 we can say that when the WL is activated then only BL and BLB writes the data into the latch. The data is available in the SRAM cell as long as the power is supplied. Figure 6 illustrates the write operation waveforms when MCPL logic is applied. The MCPL output line varies depending upon the signals S1 and S2.Word line is in logic high state during the charging phase of MCPL signal in write mode. Figure 7 shows the trapezoidal word lines and bit lines of the transmission gate based SRAM cell.

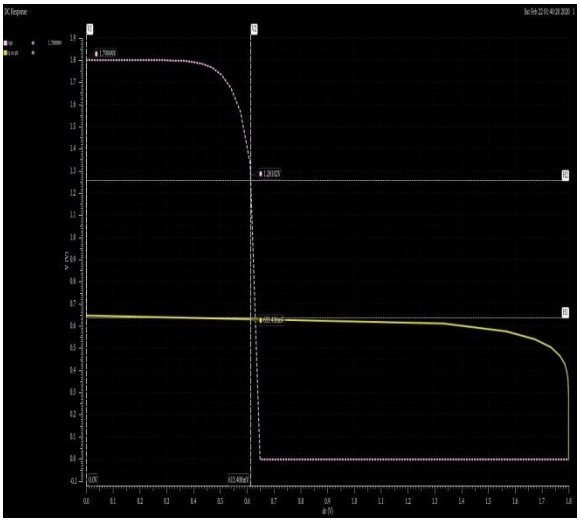

Figure 8. SNM of 6T SRAM cell.

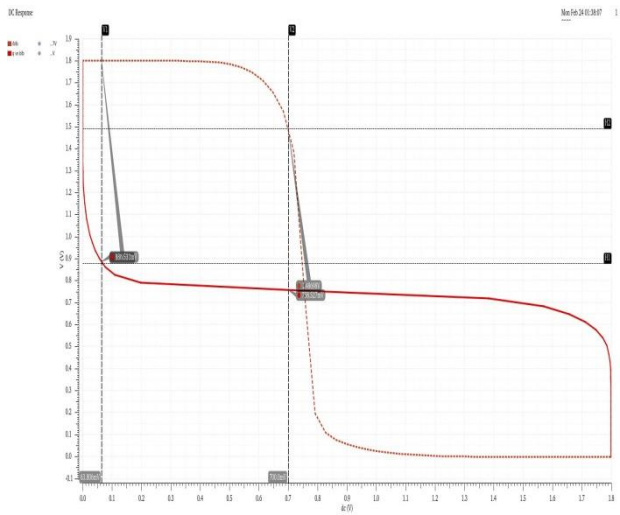

Figure 9. SNM of 7T SRAM cell.

From the Figures 8 & 9 we can observe the stability of 6T and 7T SRAM cell [6-8]. The stability of 7T SRAM is 0.3 times greater than the 6T SRAM cell. SNM is calculated by connecting the dc voltages on both sides of the inverter. Maximum square is drawn in the butterfly diagram by moving vertical and horizontal axis.

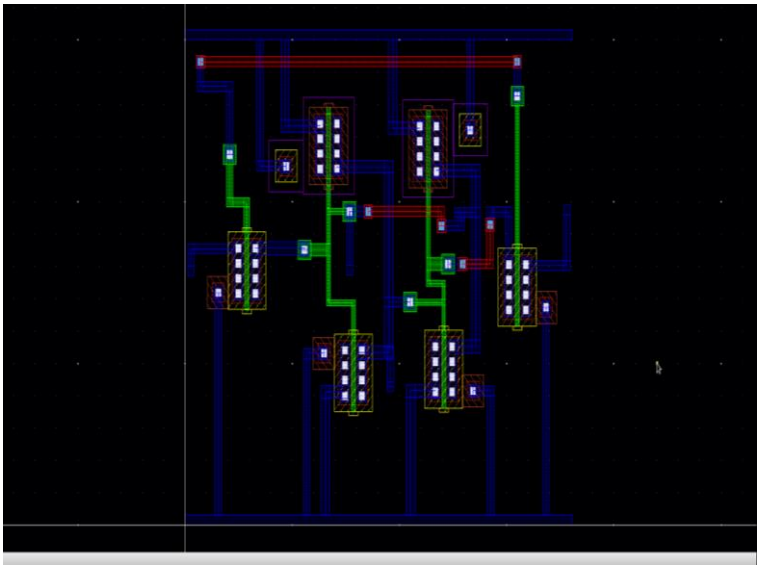

Figure 10. 6T SRAM cell layout.

The Figure 10 shows the layout of conventional 6T SRAM cell. The design is carried out in cadence platform using 180nm technology library and verified using Assura tool. The design rule checks (DRC) and the layout vs schematic (LVS) are completed as a part of the research.

Table 1 Various SRAM structures using CMOS devices

SRAM cell	**Power(w) 180nm**	**Energy(J) 180nm**	**Power(w) 32nm**	**Energy(J) 32nm**
6T SRAM cell	85.6e-6	15.4e-9	4.6e-6	0.64e-12
6T SRAM with MCPL	26.9e-7	15.4e-15	2.34e-7	7.5e-15
6T SRAM with Transmission gate	24.05e-9	9.36e-15	12.2e-9	3.4e-15
7T SRAM cell	90.2e-6	6.32e-9	24.9e-6	13.4e-12
7T SRAM with MCPL	30.1e-7	117.9e-15	5.4e-7	40.5e-15

Table 2 Various SRAM structures using FINFET devices.

SRAM Cell	**Power(W)**	**Energy (J)**
6T SRAM cell	1.3e-9	7.6e-12
6T SRAM with MCPL	0.67e-9	10.13e-15
6T SRAM with Transmission gates	5.67e-12	1.2e-15
7T SRAM cell	2.48e-9	2.34e-12
7T SRAM with MCPL	0.543e-9	0.38-15

Table 2 represents the power and energy comparison of FINFET based SRAM cells with 32nm technology. By observing the above tables we can say that transmission gate based SRAM cell has less power dissipation and less energy dissipation .FINFET devices has less power compared to cmos devices. Figure 11 presents the comparison of power dissipated in the CMOS and FinFET structures under 180nm and 32nm technology nodes.

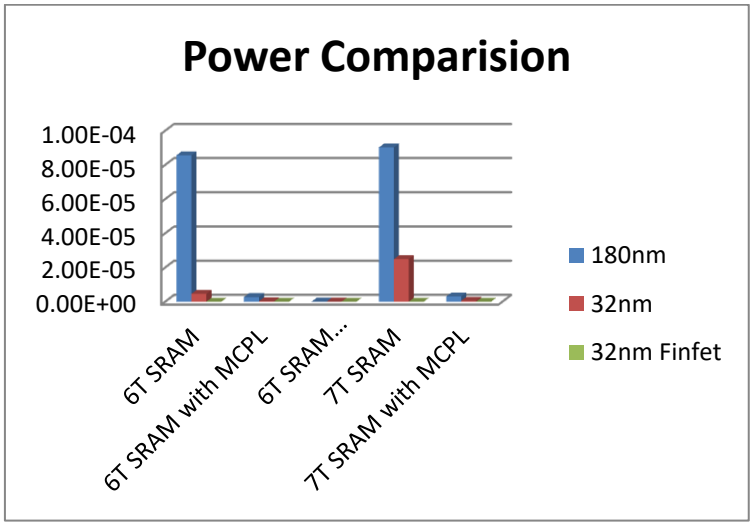

Figure 11. Power comparison of CMOS and FINFET structures.

6. Conclusion

In this paper, we presented the various structures of SRAM cell using adiabatic logic. With the help of adiabatic logic the power dissipation and energy is reduced. These structures are designed, simulated and results are taken from the cadence EDA tool. 91% of power reduction is achieved with the MCPL adiabatic logic from the conventional SRAM. Further in future new SRAM cell can be designed which will reduce the power dissipation and energy.

7.References

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