Dual Input Full Bridge Isolated DC to DC Converter

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DUAL INPUT FULL BRIDGE ISOLATED DC TO DC CONVERTER

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Abstract. This paper presents isolated dc to dc converter. It has dual input followed by two cascaded multilevel H bridge inverter and rectifier. This topology reduces the no of switches and components. Hence the cost of inverter is reduced and complexity is decreased. This is a major advantage over conventional topologies. This topology uses two DC sources which are asymmetrical, because of that seven level output voltage is obtain on the primary side of the transformer and step-up voltage obtain across the load. Switching techniques are used for proper working on this isolated converter and hence fulfil the objective of reducing overvoltage and stress in semiconductor devices. Simulation results are obtained in PSIM software.

Keywords— Multilevel inverter (MLI), Cascaded H-Bridge (CHB)

1. Introduction

For high power and high voltage application, bridge converter gained popularity and increased more attention in industry applications. As a full-bridge converter is an isolated DC-DC converter, it rectifies the disadvantage of boost converter. In various applications like switched-mode power supply, military application, battery charging system of a vehicle, medical application, renewable energy and distributed power system isolated converters are required. In many applications there is a need for electricity security demand. Hence to fulfil this demand isolated DC-DC converter should be cascaded in such a manner that consists of inverter high-frequency transformer and then rectifier. Hence scheme is like DC-AC-DC. The use of high-recurrence transformer can understand voltage proportion modification in fluctuates application events and diminish the volume of the transformer. In proposed topology, semiconductor devices like MOSFET are preferred, as there is a need for high-frequency application and MOSFET has high switching capability. As inverter is less efficient and it has demerits like high cost and high switching loss, hence multilevel inverter is preferred instead of it. The term called Multilevel originated from the three-level converter. In recent days for high voltage high power application MLI used. It produces a staircase pattern waveform; it seems to be like a sinusoidal wave, as many levels increased harmonic reduce and approximately smooth waveform obtained which is like a sinusoidal waveform. Compared to conventional inverter MLI output voltage has fewer harmonics. To reduce the total harmonic distortion, number of levels of MLI increase to N level. In MLI on reduction in step voltage between levels, the switching stress on the device is also reduced.
The multilevel inverter is classified as Neutral point diode clamped, Flying capacitor inverter and H bridge type inverter. In the proposed topology H-Bridge MLI used, is connected at the primary side of the transformer. H-bridge in cascaded fashion is the most attractive topology in Multilevel Inverter as its construction is easy and control techniques are simple. In proposed topology Two H-Bridge are connected in series and each having a separate DC source. Generally, both dc sources have the same

value but in proposed topology, both dc sources are in 1:2 ratios so that number of levels is increased than normal H-Bridge converter. Because of new topology by using fewer semiconductor devices the number of steps increases the cost of the overall system is reduced. If the ratio of two voltage sources increases then the number of levels again increases. Hence as per our requirement, we can boost the voltage. As per requirement transformer winding ratio also help to boost the voltage.

2. Different topology of multilevel inverter

2.1. Diode clamped multilevel inverter

To restrain the voltage pressure on power devices, diode is used in topology for clamping the voltage. A voltage (Vdc) is applied across each capacitor so that voltage stress over each clamping device is bounded to Vdc by using a clamping diode. This is the first topology which is practically implemented. In this topology configuration is as follow:

Required input voltage source= $K-1$ … (1)
Required number of switches for K-level= $2(K-1)$ … (2)
Required diodes for clamping voltage= $(K-2)(K-2)$ … (3)

As this topology has some disadvantage like number of levels are related to no of clamping diode hence system gets complex for higher output voltage applications [1]. The system is not flexible. Hence proposed H-bridge DC-AC converter topology is efficient for DC-DC full-bridge converter.

2.2. Flying capacitor multilevel inverter

It is similar to diode clamped inverter only the dissimilarity is instead of a diode; capacitor is used for clamping purposes. At the dc side it has a tree-like structure of the capacitor where the voltage of each capacitor is different than the next capacitor. The size of the voltage levels in the output waveform is obtained by the increase of voltage between two nearby capacitor legs. Configuration for this topology is followed:

The required number auxiliary capacitors= $(K-1)(K-2)$ … (4)
The required number of switches for K -level = $2(K-1)$ … (5)
The required number of DC-link capacitors= $(K-1)$ … (6)

As this topology have some disadvantages like purchasing capacitors for the same level of voltage. Also efficiency of this topology is very poor and it has switching realization problem. Circuits become more costly, heavily bulky and complicated than diode clamped circuit. Hence for higher voltage applications use of flying capacitor-based inverter topology is not efficient.

2.3. The cascaded H-bridge inverter

The proposed topology of Dual input isolated Full-Bridge DC-DC converter, two sources H-Bridge inverter is connected in a cascaded fashion. In H-Bridge inverter which has more than one DC source is used and each inverter produces different voltage levels. And the total produce voltage of the MLI is a sum of voltage level which is produced by each cell.

The no of level in output voltage is $2K=1$ … (7)

Where k= number of input sources. The main feature of this H-Bridge MLI is less number of semiconductor devices like switches and diode. As in H-Bridge inverter topology, sources are different so isolation is provided to each source, and also a rating of each source is low hence voltage stress on switches is reduced and at last voltage levels are added so the output voltage is boosted. H- Bridge inverter is more flexible and easy to reconstruct in case of fault. Fig.1. Shows cascaded H –Bridge inverter in which both sources have the same value it is nothing but symmetrical Cascaded H –Bridge inverter [2].

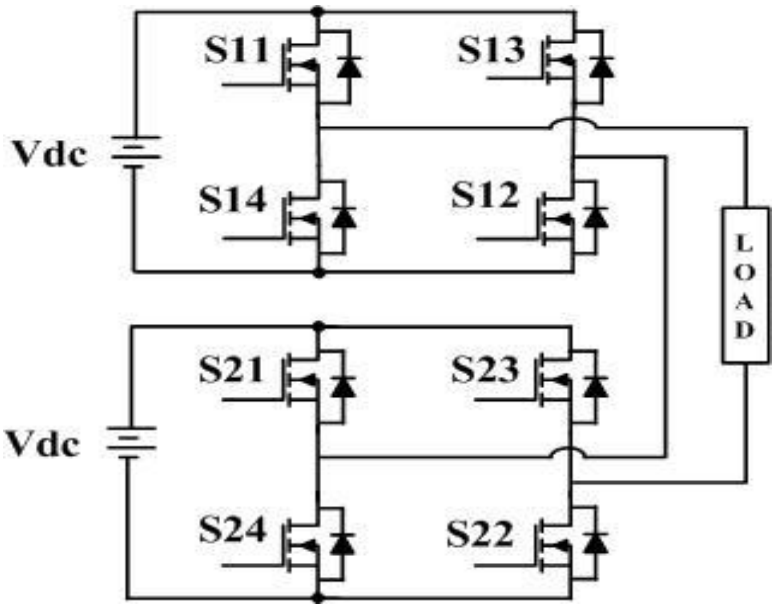

Fig.1 cascaded type H-bridge inverter

3. Proposed topology

In this paper dual input are used which are asymmetrical input voltage source. For high-frequency application eight MOSFET switches are used. Generally MOSFET is a semiconductor device and is used for an application that needs high frequency, load variation and long duty cycle. MOSFET has high voltage stress withstand capacity. Mosfet switches are used, as they have fast switching capability. In proposed topology according to switching sequence, we get 7 level output voltage at primary of the transformer which is an output of a multilevel inverter. To get this seven-level output voltage using eight switches, Two H-Bridge inverter is connected in a cascaded fashion. At the secondary of the transformer, output voltage is boosted according to the transformer turns ratio and as high-frequency transformer is used hence a size of the transformer is reduced though voltage is increased. Further to convert AC voltage in constant DC full bridge rectifier is used. Inverter output voltage is not proper sinusoidal it is a staircase wave but because of the increasing number of level total harmonic distortion (THD) reduced and get approximately sinusoidal output.

In proposed topology two H-Bridge inverter are used which have an asymmetric voltage source. As shown in fig.2 this cascaded H-Bridge inverter is different than conventional topology.

The number of voltage level $= \boldsymbol{2P+1}$, where P signifies the number of sources … (8)

Number of switches required$= \boldsymbol{2(K-1)}$, where K denotes no of level … (9)

Hence in conventional H-bridge topology 5 levels can be obtained using 2 sources and 8 switches. But in proposed topology as an asymmetric voltage source (i.e. voltage sources are in 2:1 ratio) are used we can get seven levels of output voltage using the same two sources and 8 switches. Also if voltage source in the ratio of 3:1 then using the same two voltage source and 8 switches nine levels of output voltage is obtained. Hence this proposed topology is more advantageous than conventional one as more no of output voltage level obtained using fewer devices so cost and complexity of system get reduced. Comparison between conventional topologies and proposed topology is showing in table 2.

Using proper switching sequence voltage levels can be increased. Table.1 shows the switching sequence. According to table 1, sources are 12 Volt and 6 Volt respectively. When both sources are acting then S11, S12, S21, S22 conducting and obtain 18 voltage output levels. For 12 volt output voltage only one source is acting that is 12 volt at that time S11, S12, S22 conduct and mosfet internal diode

conduct. For 6 volt S11, S12 conduct also internal diode of mosfet is forced to conduct. At time of 0 voltages no one switch conduct. Similarly for obtaining negative voltage level proper switching sequence is necessary. For -6V S13, S14 conducts. For -12 volt S13, S14, and s24 conducts. Similarly for -18 voltage output S13, S14, S23, S24 conducts. Hence as per switching sequence 7 level of output voltage is obtained as 18 V, 12V , 6V, 0V, -6V, -12V, -18 V.

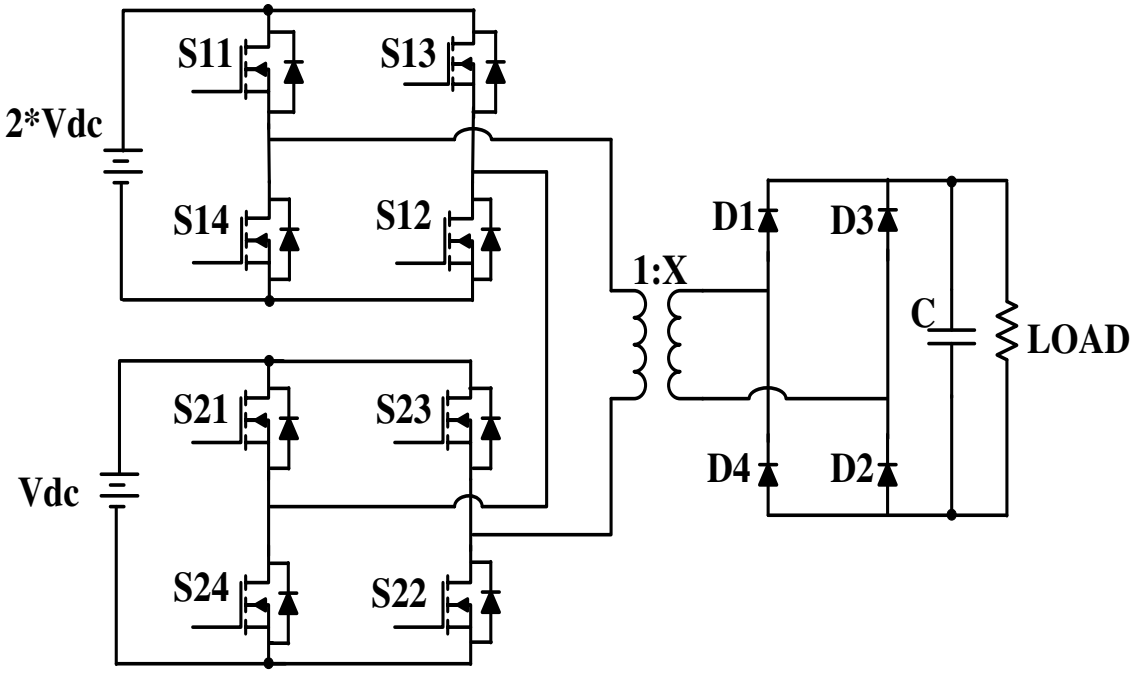

Fig2: Dual input full-bridge dc-dc isolated converter

Voltage level	S 11	S 12	S 13	S 14	S 21	S 22	S 23	S 24
18	1	1	0	0	1	1	0	0
12	1	1	0	0	0	1	0	0
6	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
-6	0	0	1	1	0	0	0	0
-12	0	0	1	1	0	0	0	1
-18	0	0	1	1	0	0	1	1

Table 1. Switching sequence of switches

Sr. no	Characteristics	Multilevel Inverter Types			
		Diode Clamped	Flying Capacitor	Cascaded H-bridge	Proposed cascaded H – Bridge
1	No of level (K)	5	5	5	7
2	Switches required	2(K-1)	2(K-1)	2(K-1)	2(K-3)
3	Diode	2(K-1)	2(K-1)	2(K-1)	0
4	Clamping diode	(K-1)(K-2)	0	0	0
5	Balancing Capacitor	0	[(K-1)(K-2)] / 2	0	0
6	DC- bus capacitor	(K-1)	(K-1)	0	0
7	Auxiliary capacitor	0	(K-1)(K-2)	0	0
8	DC source	1	1	2 symmetric fashion	2 asymmetric fashion

Table 2. Comparison of topologies with proposed topology

According to comparison given in table number 2. Cascaded H- bridge inverter topology is better than conventional h- bridge topology and also other topologies. As it required less number of devices, cost is reduced.

4. Calculations and Simulation results

As in proposed topology staircase modulation technique is used. Using equal partition method, switch conduction period is calculated as follows.

$$\propto_i = (i \times 180) \div K \quad \ldots (10)$$

Where, i = 1, 2… [(K-1)/2] and K= no of level. Conduction period according to firing angle is given in table3. Design inductor value and capacitor value for proposed topology is given in table 3. Inductor and Capacitor are act as dc side backend filter.

Switches	Conduction period	
S 11	$\propto_1 = 25.71^\circ$	$\propto_6 = 154.29^\circ$
S 12	$\propto_1 = 25.71^\circ$	$\propto_6 = 154.29^\circ$
S 13	$\propto_7 = 205.71^\circ$	$\propto_{12} = 334.25^\circ$
S 14	$\propto_7 = 205.71^\circ$	$\propto_{12} = 334.25^\circ$
S 21	$\propto_3 = 77.14^\circ$	$\propto_4 = 102.6^\circ$
S22	$\propto_2 = 51.42^\circ$	$\propto_5 = 128.58^\circ$
S23	$\propto_9 = 257.14^\circ$	$\propto_{10} = 282.84^\circ$
S24	$\propto_8 = 231.42^\circ$	$\propto_{11} = 308.55^\circ$

Table 3. Switches conduction angle

For full bridge converter Output voltage equation is given as follows

$$V_0 = \frac{V_{in}\, n_2}{2n_1\,(1-D)} \quad \ldots (11)$$

Inductor critical value calculated by following equation no. 12

$$L_{CRITICAL} = 2\left(\frac{n_1}{n_2}\right)^2 R(1-D)^2\left(D-\frac{1}{2}\right)T \quad \ldots (12)$$

4.1. Waveform of seven level output voltage

The input voltage of topology is 12 volt and 6 volt. Hence 7 level output voltage is obtained as 18 V, 12V, 6V, 0V, -6V, -12V, -18V. Seven level output voltage of MLI on the primary side of the transformer is shown in fig.3

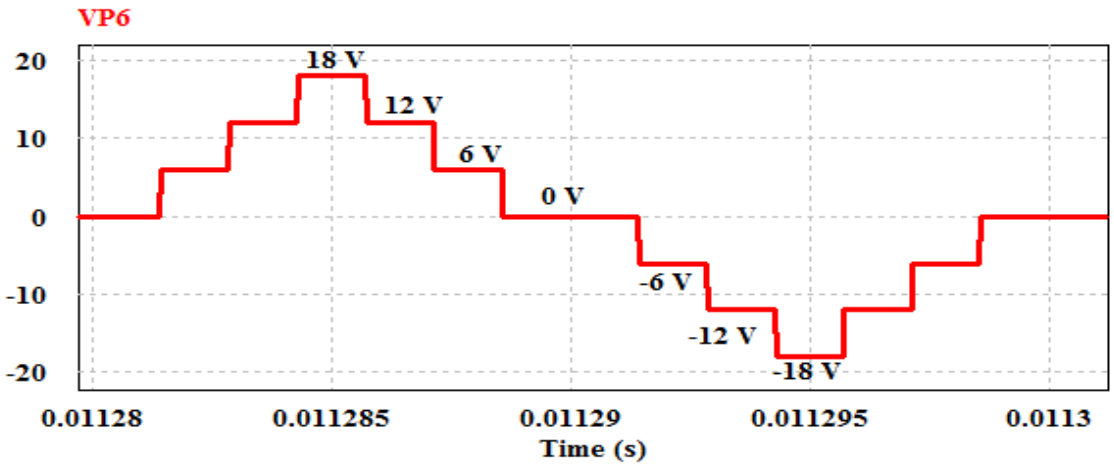

Fig.3 Waveform of seven-level output voltage

4.2. Waveform of input current from two sources

Average value of input current of each source is shown in fig. 4

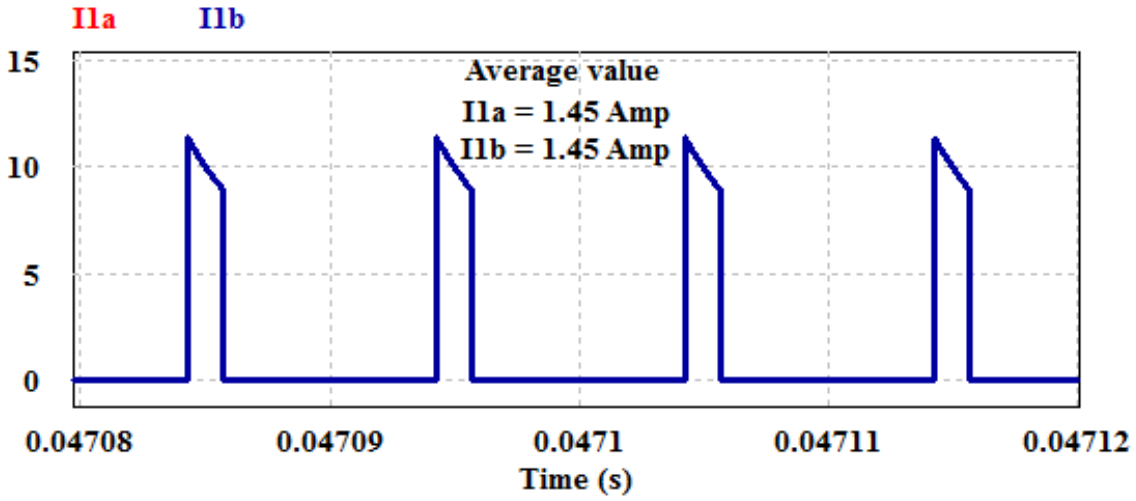

Fig.4 waveform of the average value of current

4.3. Waveform of output voltage

Output voltage waveform of dual input full bridge dc-dc converter when the transformer ratio is 1:2. As input sources voltage is 12 and 6 hence maximum voltage is 18 volt obtaining at primary side of transformer.

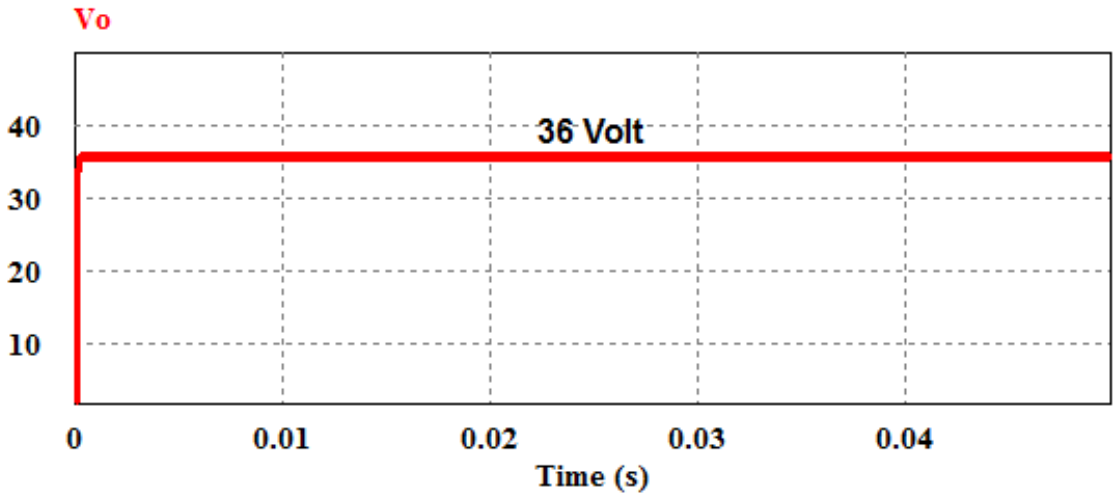

Fig.5 waveform of output voltage

4.4. Waveform of output power

Output power 25 watt is shown in Fig. 6

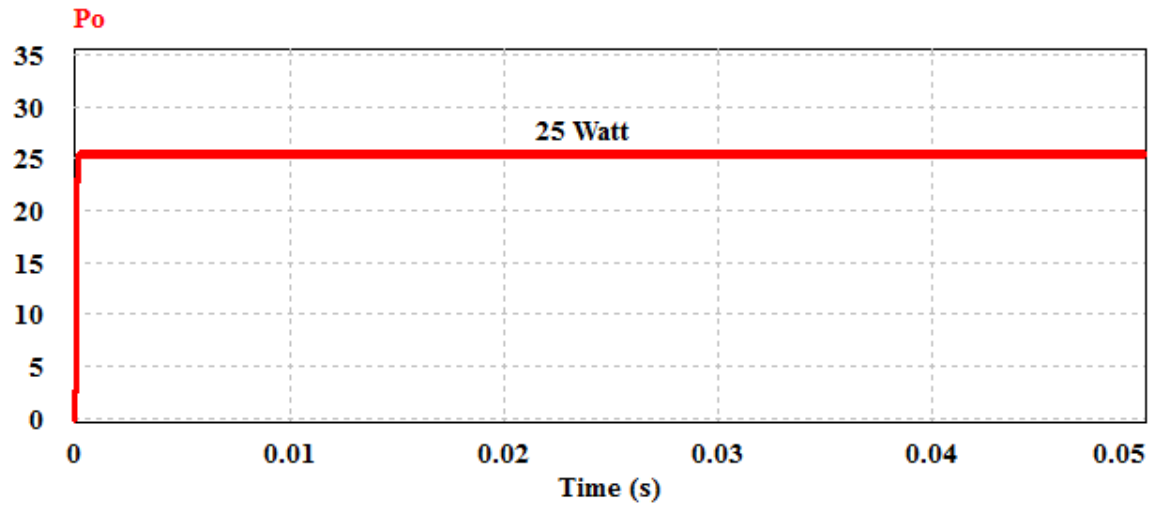

Fig.6 The output power waveform

From simulation waveform V out = 36 volt, Ia average = 1.45 Amp Ib average = 1.45 Amp and output power = 25.52 watt, Input power = (12*1.45) + (6*1.45) = 26.1 Watt, Hence the efficiency of dual input full-bridge isolated DC to DC converter is 97%

4.5. The output voltage waveform

When the transformer ratio is 1: 20 then using same 12V and 6 V input source, 351V output voltage obtained. Output voltage is shown in fig.7

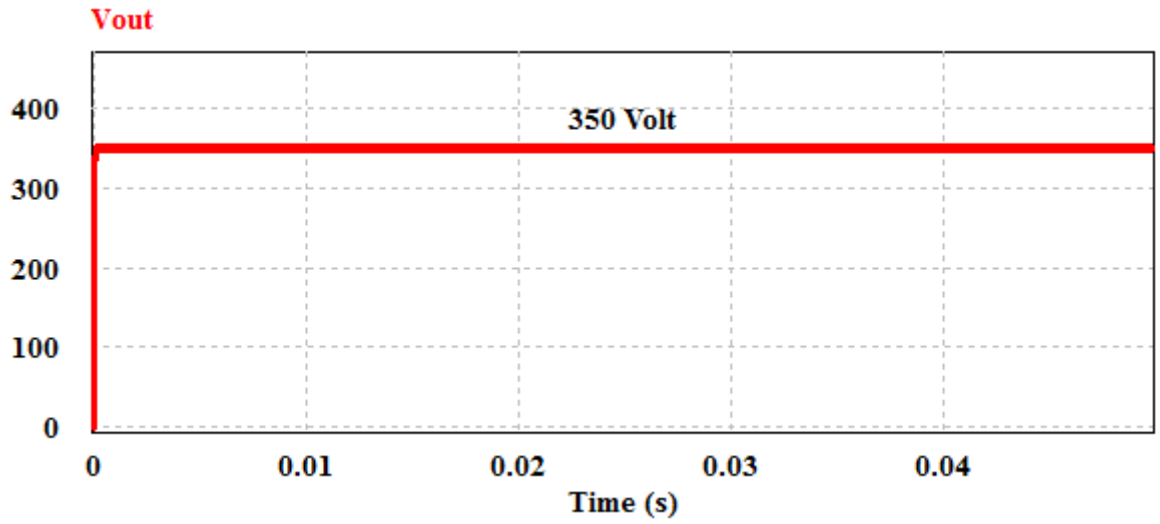

Fig.7 waveform of output voltage

5. Conclusion

In this paper, using two asymmetrical input source, numbers of voltage level increased on the transformer's primary side. The boosted output voltage is obtained using a high-frequency transformer which has a high transformer turns ratio. Hence the efficiency of the Full bridge converter is increased using two cascaded multilevel inverter. Also cost is reduced because number of devices gets reduced. According to simulation result, this topology has low power losses, high reliability, high power density and a wide range of handling input and output voltage.

6. Reference

[1] M. Pahlevani, S. Eren, H. Pahlevaninezhad, I. Askarian, and S. Bagawade, *"Digital current sensorless control of current-driven fullbridge DC/DC converters," IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1797–1815, Feb. 2018.

[2] N. Sandeep, and U. R. Yaragatti*, "A Switched-Capacitor-Based Multilevel Inverter Topology With Reduced Components,"* IEEE Trans. Power Electron., vol. 33, no. 7, pp. 5538-5542, July 2018.

[3] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi*, "A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series–Parallel Conversion With Less Number of Components," IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582-3594, June 2016.

[4] W. J. Cha, J. M. Kwon, and B. H. Kwon, *"Highly efficient asymmetrical PWM full-bridge converter for renewable energy sources," IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2945–2953, May 2016.

[5] R. Kathiresan, P. Das, T. Reindl, and S. K. Panda, *"A novel ZVS DC–DC full-bridge converter with hold-up time operation,*" *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4491–4500, Jun. 2017.

[6] K.K. Gupta, A. Ranjan, P. Bhatnagar, L.K. Sahu, S. Jain, "Multilevel Inverter Topologies with Reduced Device Count: A Review," IEEE Trans. on Power Electron., vol.31, no.1, pp.135–151, Jan. 2016.

[7] M. Malinowski, K. Gopakumar, J. Rodriguez, M.A. Perez, *A survey on cascaded multilevel inverters,* IEEE Trans. Industr. Electron. 57 (7) (2010) 2197–2206.

[8] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, *"Power Routing for Cascaded H-Bridge Converters," IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9435-9446, Dec. 2017.

[9] International Journal Of Engineering And Computer Science ISSN: 2319-7242 Volume 3 Issue 6 June, 2014 Page No. 6341-6346 "*Analysis of Three Level Diode Clamped Multilevel Fed Induction Motor Drive"* Sadhana pandey, Sulochana Wadhwani, Praveen Bansal

[10] "*Asymmetric cascaded half-bridge multilevel inverter without polarity changer",* Ahmed, A Sheir, M Orabi - Alexandria engineering journal, 2018 - Elsevie