Experimental Verification of Single-Stage Power Factor Correction Converter with Improved Light-Load Efficiency

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Abstract. Single-stage single-switch ac/dc converters with power factor correction will have higher power losses under a light-load condition, as compared to that of two-stage approach, due to sharing of a common power transistor such that the power factor correction (PFC) stage cannot be switched OFF separately to save power losses. This paper addresses the problem by using a buck topology for the PFC stage of single-stage single-switch converters as it can completely turned OFF. This converter topology is capable of working in both buck mode and buck-boost mode depending on the rectified voltage at input side and power at load side. A simple and effective topology incorporating PFC for low power applications is simulated in Matlab/Simulink environment. Hardware implementation of the converter was and performance was verified with various practical light loads. It also satisfies the harmonic compliance of source current in accordance to the IEEE519:1992 recommendations. The control is very simple and gives good performance.

1. Introduction

In mid nineties, since the research of single-stage PFC converters, they have now been embraced for various low-control change hardware. The acknowledgment of converters is a direct result of their improved converter structure and controller circuit when compared with two-stage PFC design. As of late, energy efficiency concept has been joined into switching power supply design because of the implementation of stringent guidelines from administrative bodies, for example, Energy Star and AU/NZ Minimum Energy Performance Standards (MEPS). There are different ways to deal with reducing power utilization under a light-load condition. Including a small auxiliary power conversion circuit in parallel with the output load enhances the overall efficiency, especially under a light-load condition. The thought is to enhance both principle and assistant power conversions by fluctuating the sharing of aggregate output power among the two transformations under light load conditions.

A single-switch bridgeless boost PFC converter is proposed in [1] employing a single switch that performs both PFC at the the input side and boosting of the dc voltage. It uses the same number of energy storage elements as in the conventional converter. It aims at minimizing the switching loss for improving the efficiency.

The buck PFC front-end has higher light-load effectiveness than that of its boost counterpart because of its lower voltage stress on switching devices. At light load, switching loss is more overwhelming than conduction loss and the voltage stress is the key component in deciding

switching loss. By powerfully scaling of gate drive voltage, the switching loss can be decreased. For two-stage PFC design, turn off the PFC stage has been demonstrated a compelling strategy to decrease power loss. It is hard to apply the same technique to PFC converters as the PFC stage and dc/dc stage have the same power switch, unless the converter has various switches and is built diversely such that it can control currents from the AC line and intermediate storage capacitor to flow into the converter in partitioned time spaces inside of an switching period. The conceivable methodology with turning off the PFC stage in single-switch PFC converters like that in the two-stage approach is proposed in [2]. The thought takes advantages of varying the input voltage and dead angle of input current characteristic for the ac/dc converter. The buck or buck-derived PFC converter naturally has such trademark as there are times during a line cycle when the input voltage is smaller than the output voltage and the PFC stage is successfully turned off. The motivation behind this is consequently to clarify, analyze, and show this methodology through a selected single-stage single-switch buck-determined PFC topology under the light-load operation where the power consumption of the load is just a few watts or less and to assess diverse changing examples to scan for the least power misfortunes under this condition. Experimental results are displayed to exhibit the effectiveness of the proposed light-load power losses reduction plan. Main advantage of this topology is simple and it can be used for low power applications as well as improvement in power factor can be easily implemented by this converter.

With the concept of zero-voltage switching boost-integrated technique (ZVS BIT), a ZVS flyback-boost converter with voltage doubler rectifier is derived and investigated in detail as an example. In addition, focused on the soft switching characteristics of the ZVS BIT, the LLFM control method is analyzed to extend a ZVS load range[3]. A buck-boost converter topology for implementing digital power factor correction based on low cost digital signal controller that operates the converter in continuous conduction mode, thereby significantly reducing input current harmonics [4]. A two-stage optimization procedure to optimize the power converter efficiency from light load to full load is proposed. The optimization procedure first breaks the converter design variables into many switching frequency loops.[5]

A detailed design-oriented analysis of the clamped-current buck (CCB) PFC converter is presented. The design is focused on the slope of the external current ramp. It is shown that with a constant slope of the external current ramp in the whole input voltage range, an optimum design cannot be achieved. The slope of the external ramp should be variable and increase with increasing input voltage [6]

The bulk capacitor voltage feedback with a coupled winding structure can effectively reduce both the voltage and current stresses in single-stage PFC ac/dc converters. It is also pointed out that changing the L_m has no effect on bulk capacitor voltage and duty ratio if L_m operates in CCM at heavy load[7].

By dynamically scaling the gate voltage swings of large, integrated MOS power devices, light-load efficiency can be improved and the usable load current range extended in synchronous rectifier buck converters [8]. The PFC for single phase AC-DC Buck-Boost Converter operated in Continuous Conduction Mode (CCM) using inductor average current mode control is discussed in [9]. It has the advantage of robustness even under large variations in the voltage and load variations.

2. Single-stage PFC buck converter

The circuit of single-stage PFC buck converter is shown in figure 1.

2.1. Operating principle

To smooth the advancement of the clarification of light-load operation in single-stage PFC converters, an as of late presented transformerless high step down single-stage PFC converter is

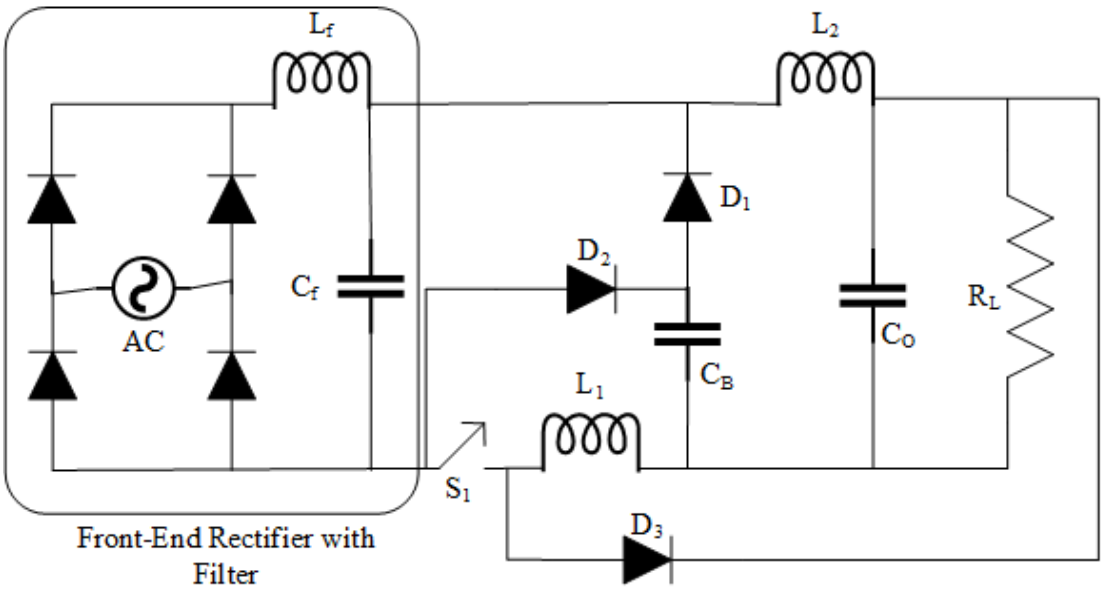

Figure 1. Circuit of single-stage PFC buck converter.

utilized as a sample. The converter, as appeared in figure 1, is a coordination of a buck PFC cell with a buckboost dc/dc cell. The buck PFC cell comprises of L_1, S_1, D_1, C_o and C_B, while the buckboost dc/dc cell comprises of L_2, S_1, D_2, D_3, C_o and C_B . Since the information voltage V_{in} changes somewhere around zero and its top worth, furthermore as the buck converter just works when data voltage is more noteworthy than output voltage, the proposed converter has two operation modes.

Mode 1:

Mode 1 starts when $V_{in} \leq V_B + V_o$ (where V_B is the dc-link capacitor voltage and V_o is the output voltage). The buck PFC cell is inactive and there is no input current flowing into the converter. In this mode just the buck-boost dc/dc cell is active. At the point when the switch S_1 is turned ON, L_2 is charged by C_B through D_2. The voltage voltage is supported by the output capacitor C_o. After duration of dT_s, S_1 is turned off. The energy stored in L_2 is exchanged to output by means of D_3. The inductor current i_{L2} is totally discharged before the beginning of the next switching cycle.

Mode 2:

Mode 2 begins when $V_{in} > V_B + V_o$. Both PFC cell and dc/dc cell are active. At the point when S_1 is turned ON, both inductors L_1 and L_2 are charged directly by $V_{in} - V_o - V_B$ respectively. After duration of dT_s, S_1 is turned off. L_2 discharges its energy to output through D_3 while L_1 couples its energy to both output and dc bus capacitors as $C_o - R_L$ and C_B are in series of the current path of i_{L1} . Both i_{L1} and i_{L2} are totally discharged before the start of the following switching cycle.

2.2. Design parameter

In this section, the proposed buck and buck-boost PFC converter is designed with all circuit parameter [10, Chap. 13].

For buck converter:

The duty ratio is given by

$$D = \frac{V_0}{V_{in}} \tag{1}$$

Table 1. Design Parameters.

S. No	Parameter	Values
1	Supply voltage	24 V_{rms}
2	Supply frequency	50 Hz
3	Switching frequency	30 kHz
4	Duty ratio 'D'	0.2
5	Filter inductor	2 mH,10 A
6	Filter capacitor	2.2μF, 450 V
7	Output Capacitor	100μF, 160 V
8	Output capacitor	10 μF, 450 V
9	Converter Inductor	10 mH, 15 A
10	Converter Inductor	120 mH, 10A
11	Output voltage	6 V

where,
V_0 = Output voltage of the converter
V_{in} = input voltage of the converter

The critical value of the inductance L_{cric} design is under the condition that buck converter, which can be expressed as

$$L_{cric} = \frac{(1-D)R}{2f} \tag{2}$$

where,
R = Output load
f = switching frequency of the converter

The critical value of output capacitor is,

$$C_{cric} = \frac{(1-D)}{16 * L * f^2} \tag{3}$$

Therefore, the critical inductor and capacitor of the proposed converter can be designed according to equation (2) and (3) where the inductance of inductor and output capacitance should be chosen higher than the critical value.

For buck-boost converter:

The critical value of the inductor L_{cric} design is under the condition that buck converter, which can be expressed as same in equation (2), whereas the critical value of output capacitor is given by

$$C_{cric} = \frac{D}{2fR} \tag{4}$$

Therefore, the critical inductance and capacitance of the proposed converter can be designed according to equation (2) and (4) where the inductance and output capacitance should be chosen higher than the critical value.

3. Simulation of single-stage PFC buck converter

The single stage PFC buck converter for low power application and power factor correction circuit under open loop is designed and simulated under MATLAB/Simulink environment. Resistive load is considered for the simulation. The design parameters of the converter are listed in Table 1.

3.1. Simulation studies

The single-stage PFC buck converter is designed following design constraints and is implemented in Simulink environment. Appropriate measurement blocks are used for measuring the fundamental component of voltage and current to calculate the phase difference between the current and voltage at the source side. The converter is simulated under open loop configuration with a resistive load. A 24 V ac supply is applied to diode bridge rectifier. An LC - filter is used to reduce ripple content of rectifier output. The presence of this LC-filter causes distortion in the supply current, resulting in high THD, losses and poor power factor.

The results of simulation are described as follows. The supply voltage and current of the ac supply is shown in figure 2. Upon comparing the zero-crossing of the source current and voltage, the power factor is near to unity.

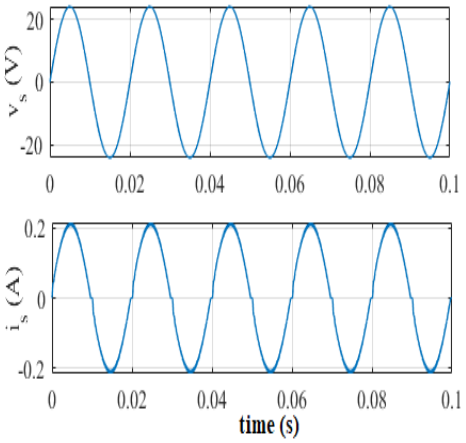

Figure 2. Waveforms of supply voltage and current.

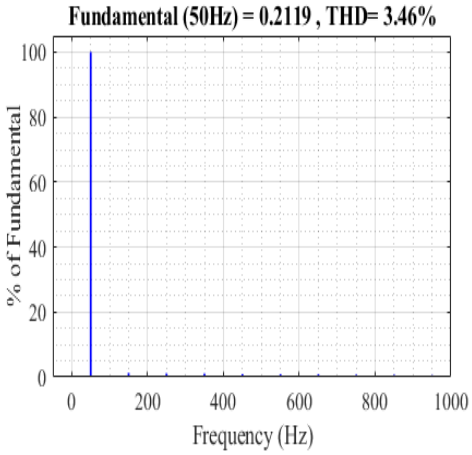

Figure 3. Frequency spectrum of source current.

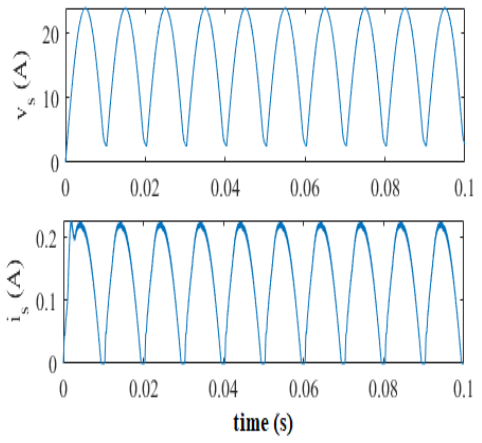

Figure 4. Waveforms of rectifier voltage and current.

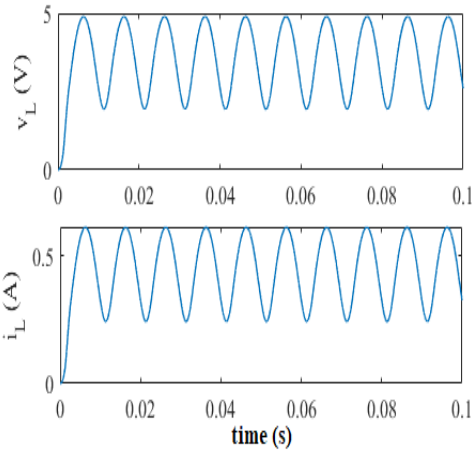

Figure 5. Waveforms of buck converter output voltage and current.

The harmonic spectrum of source current computed using FFT tool in simulink is shown in figure 3. The THD of the ac source current is 3.46 %.

The power factor corresponding to this operating point is given by

$$Power factor(pf) = \sqrt{\frac{1}{1+THD^2}} = 0.995(lag) \tag{5}$$

The output voltage and current of the rectifier is shown in figure 4 and the source current is discontinuous. In figure 5, the output voltage and current of buck converter are shown where the load current is continuous. From the results, output power is computed as 10 W satisfying the low power application for converter.

4. Hardware implementation

The simulated single stage PFC buck converter is implemented in hardware and tested for its performance under laboratory conditions. The converter was tested with two different types of loads wiz resistive load and LED load. The experimental setup of single stage PFC buck converter is shown in figure 6. The low ac voltage is derived from supply mains through an autotransformer and is applied to the bridge rectifier. It is then converted into dc and applied to the PFC buck converter.

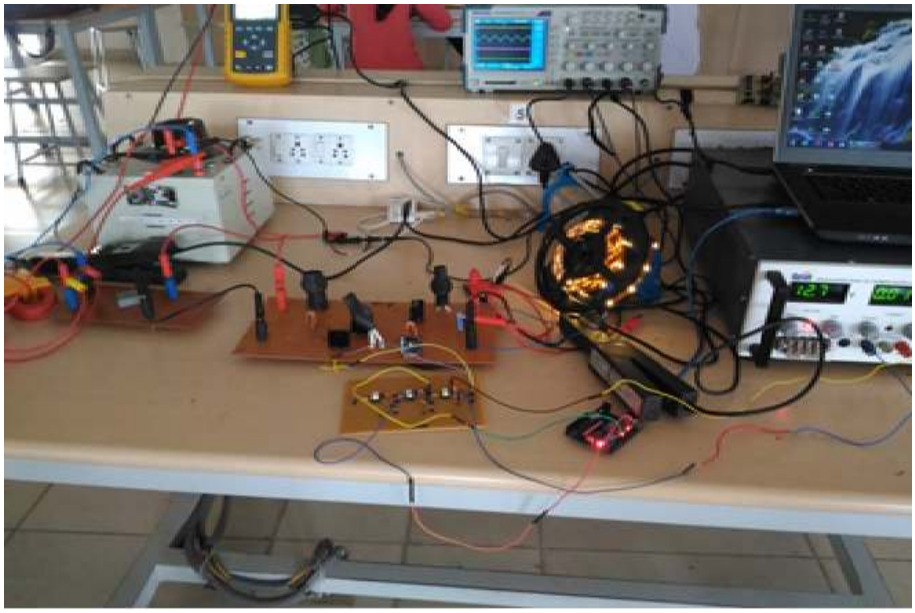

Figure 6. Experimental setup of single-stage PFC buck converter.

4.1. With 'R' load

The circuit is tested for its performance with resistive load connected at the output. A rheostatic load is used so as to adjust the current level of the converter to its rated value. The waveforms are captured using Tektronix TPS2024B four channel isolated DSO with suitable voltage probe and current probe arrangement. The captured source voltage, source current, output voltage and output current are shown in figure 7.

The source current is nearly sinusoidal and is in phase with the supply voltage. The harmonic distortion in the source current and other parameters such as real, reactive and apparent powers are measured using Fluke 3B - power quality analyzer. The captured source voltage and current

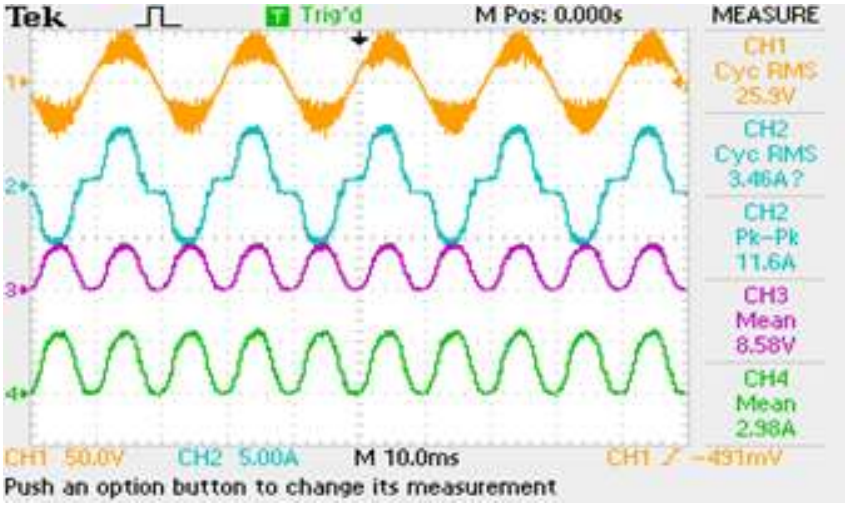

Figure 7. Experimental results of single-stage PFC buck converter captured using TPS2024B DSO.

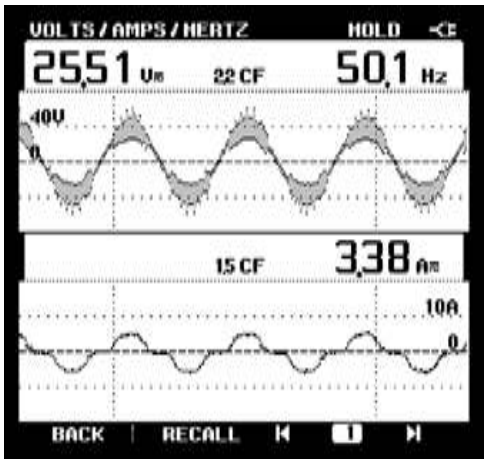

Figure 8. Source voltage and current captured using Fluke-3B.

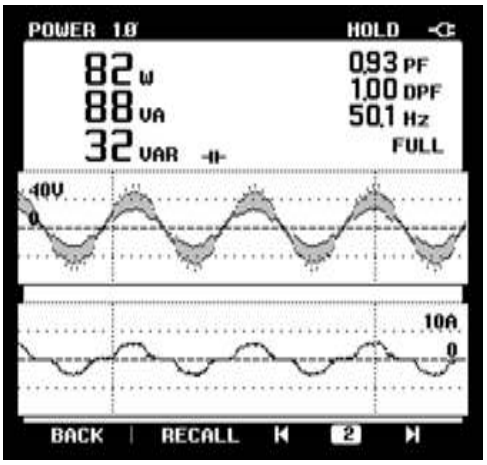

Figure 9. Power Measurements using Fluke-3B.

waveform with measurements are shown in figure 8 and the power measurement is presented in figure 9 respectively.

The harmonic spectrum of source current in figure 10 measures the current THD to be 29%.The power factor of the ac source from the measurements is 0.93 lag and the displacement power factor is unity.

4.2. With LED load

The experiment is repeated with LED strip as load on the PFC buck converter. The performance of the converter with LED load is observed using Tektronix DSO and Fluke-3B power quality analyzer. The source voltage and current, load voltage and current waveform captured in Textronix DSO is shown in figure 11.

The source current and voltages are captured using Fluke-3B power quality analyzer is shown in figure 12. The power drawn by the converter is 73 W at a power factor of 0.97 lag. The

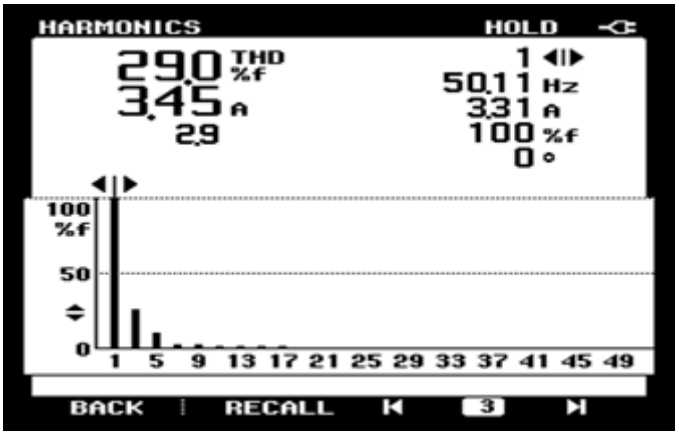

Figure 10. Harmonic spectrum of Source current captured using Fluke-3B Power Quality Analyzer

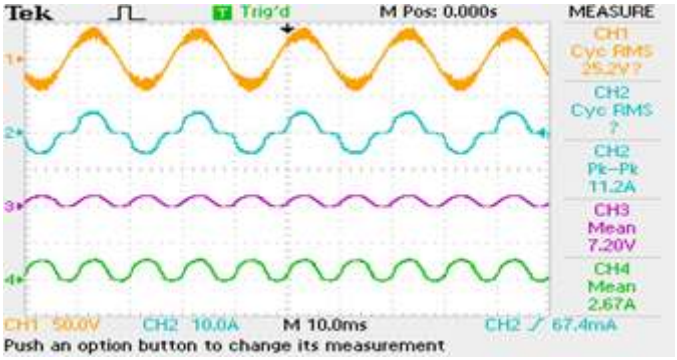

Figure 11. Measurements of source current captured using TPS2024B DSO for LED load.

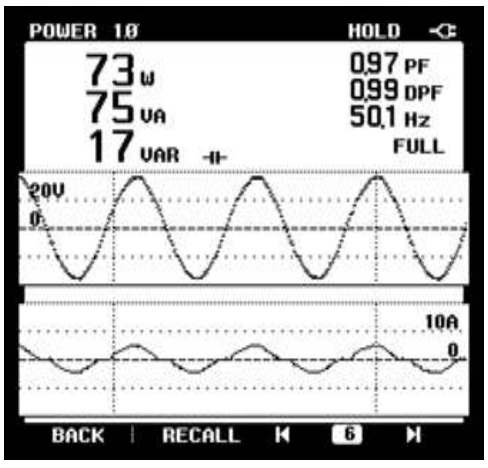

Figure 12. Power measurements for LED load using Fluke-3B.

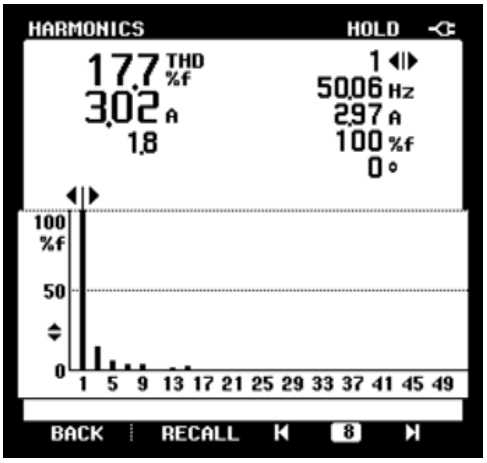

Figure 13. Source current spectrum with LED load.

harmonic spectrum of the source current is measured and is shown in figure 13. For both types of loads, the power factor is measured to be 0.93 and 0.97 respectively which is close to unity. The hardware is powered continuously under lab environment for the duration of 90 minutes with LED load and tested for reliable operation. The objective is to test the converter performance under continuous operation. The converter performance was observed to be satisfactory.

5. Conclusion

Single-stage PFC buck converter for low power applications was implemented in hardware and tested for its performance. The design of the converter is validated through simulation using Matlab/Simulink tool. The hardware model is tested with two different types of load and the power factor of the ac supply is observed to be close to unity. In the absence of DC - DC converter stage, the power factor of the ac supply is poor due to LC - filter at the rectifier which cannot be eliminated. The single stage converter can work more reliably at low output power with reduced losses when compared with conventional two-stage PFC circuits. The single stage PFC converters have more than one power processing stage and hence its efficiency will be lower than conventional buck PFC rectifier. In future, the converter performance can be analyzed with sudden load changes or sudden changes in the supply voltage conditions. Based on the performance, a suitable controller can be designed to regulate the converter under supply voltage fluctuations and/or load changes.

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