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Feasibility Study of Conical Channel Nanowire MOSFETs for Improved Performance

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Abstract

In the nano-electronics era silicon nanowire MOSFET in gate all around configuration has proved to be good candidate due to its ability to suppress the short channel effects. In this paper a novel architecture introduced which is the modified form of cylindrical channel silicon nanowires. The proposed structure consists of a conical channel with tapered end near the drain. The regular tapering helps for equal distribution of field along the cross- section of the channel. The simulation results show that this architecture can improve the drain current and gain of the MOSFET. The effect of rate of tapering to various characteristics is also analyzed through simulation.

Keywords: Conical channel; GAA Silicon Nanowire MOSFET; channel tapering; tapering ratio.

1. Introduction

As the scaling of devices below 100nm causes several issues like short channel effects, the development of three dimensional devices like Multigate MOSFETs, ultra thin SOI MOSFETs, FinFETs, Silicon Nanowires, Nanotubes etc. become important for the further advancement in the integrated chip industry. Among these, the Silicon Nanowires are the ultimate candidate for nano-electronics due to its better gate control over the channel. As a result of better gate control over channel, it can suppress the short channel effects more effectively. In this paper, cylindrical silicon nanowire MOSFETs with tapered and untapered channel is taken for the study. In cylindrical silicon nanowire, the corner effects are less even at higher doped channels [1]. The corners cause formation of regions with different threshold

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voltage, resulting in the regions which turn on at different voltages. The characteristics of the Gate All Around Silicon Nanowire MOSFET depends on the diameter of the channel. Increase in diameter causes increase in the drain current [2]. The dependence of the diameter on the drain current is given in eqn. (1).

$$I_{DS} = \mu \frac{2\pi R}{L} \int_0^{V_{DS}} Q(V)\, dV \tag{1}$$

Usually the silicon nanowires are considered ideally as cylindrical with uniform diameter. But the nanowires fabricated using Vapour-Liquid-Solid method in bottom up approach show temperature dependence on the morphology of nanowires grown [3]. As a result tapered nanowires are formed during nanowire synthesis. It has been reported the improved field emission characteristics shown by tapered nanowires over untapered ones [4]. This phenomenon of tapering is used for the improvement of performance. The tapering control can be done by advanced techniques [5][6].

In this paper a novel channel architecture for GAA Silicon Nanowire MOSFET is introduced which is the modified form of the cylindrical silicon nanowire. Here the channel of proposed device is conical in shape. The performance variation in the conical shaped GAA Silicon Nanowire MOSFET is compared with cylindrical shaped GAA Silicon Nanowire MOSFET. Analysis is done based on the simulation results and is given in the next section. Then, the effect of tapering ratio on the performance is also analyzed.

2. Device Structure and Simulation.

Here the GAA Silicon Nanowire MOSFET structure is created and simulated using the Sentaurus Device Simulator. The channel is lightly doped at $10^{13}/cm^3$. Source and drain are heavily doped at a range of $10^{18}/cm^3$ to $10^{20}/cm^3$. The device with uniform channel diameter is Device A with 10nm. Device B is having a tapered diameter with tapered end near the drain. This forms the conical channel which is the proposed architecture. Device C is with a uniform diameter of 5nm. The schematic diagram of the simulated devices is as shown in Fig.1.

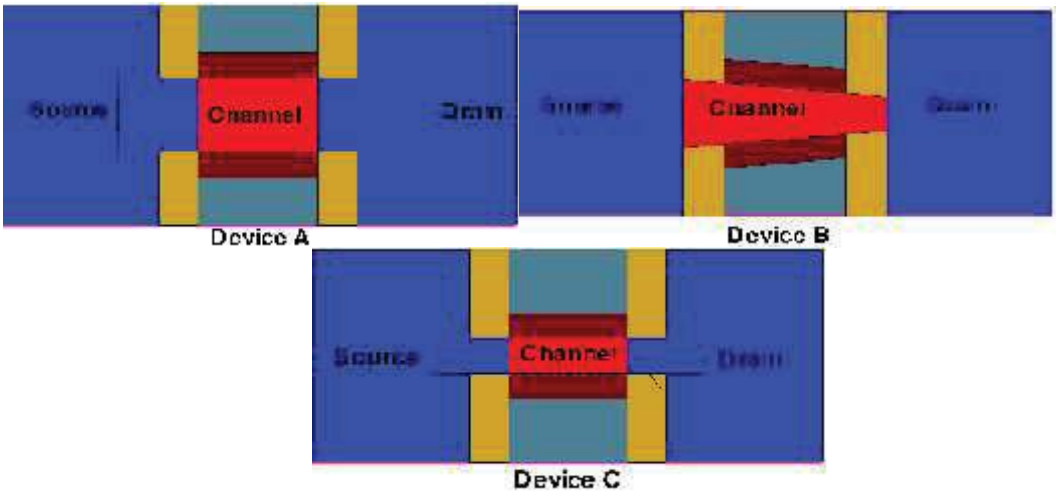


Fig.1 Schematic diagram of various simulated devices

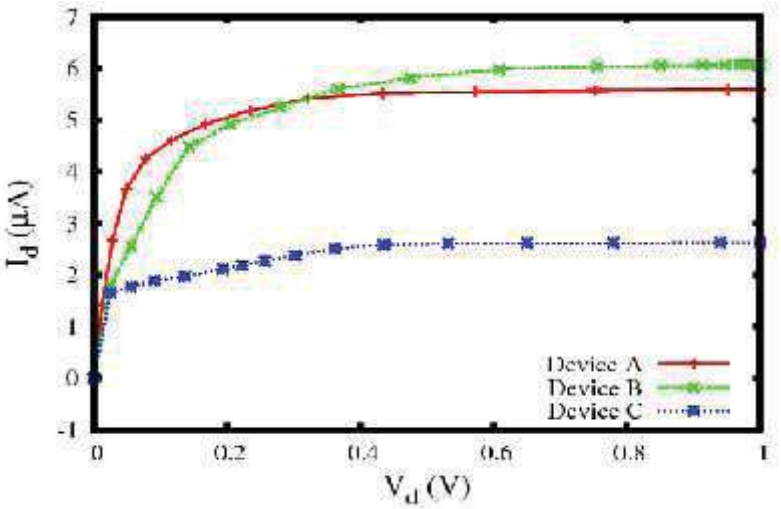


Fig.2. I_d-V_d characteristics for different devices

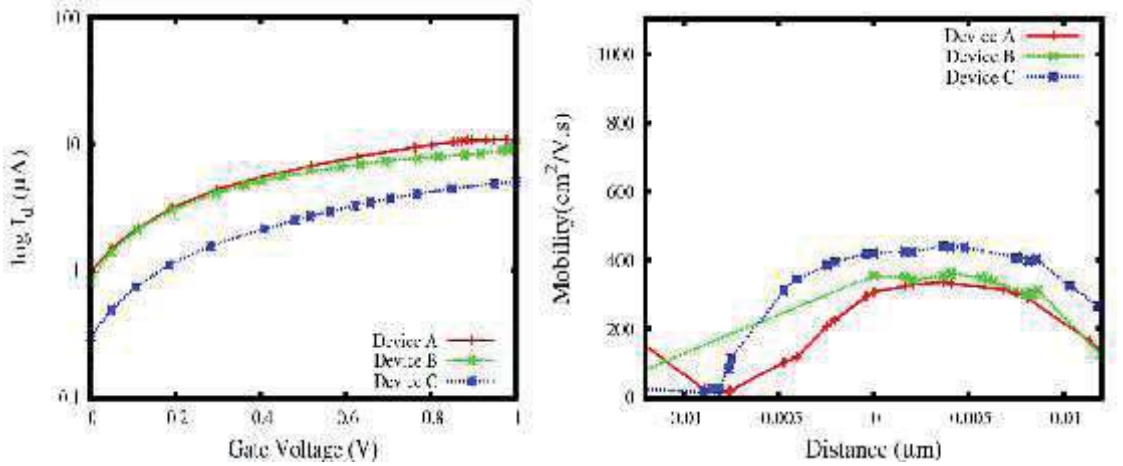


Fig.3. a) log I_d-V_g characteristics of various devices. b) Mobility of electrons along channel of various devices

The devices are simulated using Sentaurus Device Simulator [7] and the I_d-V_d characteristics are obtained as shown in the Fig. 2. From the Fig.2, it is clear that the Device B which is having the conical channel gives more drain current than the Device A which is having a uniform channel with 10nm diameter. In the Device B, the tapering of channel results in a pumping effect, since at the tapered end electric field strength is more. Due to this, the mobility of the electron increases. Rate of increase of the drain current due to this improved mobility is more than the current decreased by the reduction of diameter of the channel. As a result, the net current in the tapered channel get increased than the untapered channel. The increase in the mobility also leads to the improved transconductance of the device. Device B has an improved transconductance of 28.3μS compared with Device A which has got the transconductance of 11.8μS. The log I_d-V_g characteristics is obtained as shown in Fig.3a.

Table 1. Devices with various tapering ratios

Device Name	Channel diameter near drain	Tapering ratio	Angle made by surface
Device B	5	0.5	84.29
Device D	7	0.7	86.56
Device E	8	0.8	87.70
Device F	9	0.9	88.85
Device A	10	1.0	90.00

Fig.3 a. shows that, if the diameter is reduced in uniform channel Silicon Nanowire MOSFET, the current reduces as a result the transconductance reduces. But the transconductance of tapered channel device get improved. This improvement in the current is due the improved mobility which is shown in Fig.3b.

It is clear that the tapering channel has improved the performance. Now the effect of rate of tapering of the channel has to be analyzed. For this, various devices with different diameters are created in the Sentaurus Device Editor. The channel parameters are as shown in Table1.

The devices are simulated and the drain current characteristics are obtained as shown in Fig.4a. From the Fig.4a, it is clear that the drain current increases as the tapering ratio increases initially. The current is more for Device E than Device B, as the ratio increased from 0.5 to 0.8. But, further increase in the ratio causes the decrease in the drain current. This is because the mobility of the electrons reduces, even if the area of cross section increases. Here the dependence of current to mobility is more. The peak saturation current varies as shown in the Fig.4b. The saturation current is maximum for the Device E having the ratio of 0.8. Then, as the ratio increases, the saturation current decreases.

This can be explained by analyzing the mobility variation for varying the tapering ratio. As the diameter of channel near drain decreases by keeping the channel diameter near the source constant, the mobility

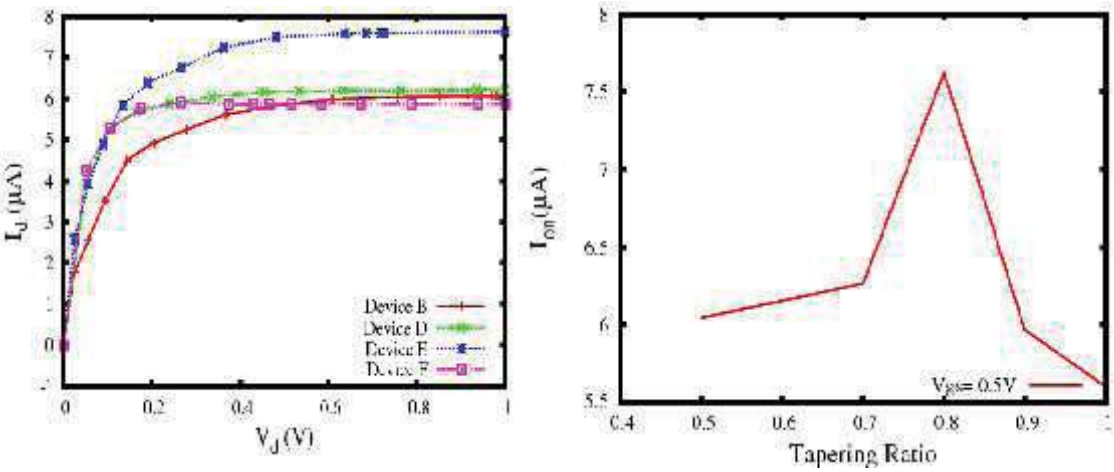


Fig.4. a) I_d-V_d characteristics for devices with different tapering ratios b) I_{on} variation with tapering ratios

increases. But, due to the less area of cross section the current decreases as tapering ratio decreases for devices below 0.8 tapering ratio. At tapering ratio of 0.8, the current is maximum. So, the optimized tapering ratio in terms of drain current is Device E. Then the current decreases as the ratio increases to 1.0. The mobility of electron in the channel is as shown in Fig.5.

Due to the improved mobility, the transconductance also increases. Fig. 6 gives the variation of transconductance with tapering ratio for various drain bias. The transconductance of various devices is normalised based on the transconductance of cylindrical Silicon Nanowire and the difference is plotted. From the Fig. 6, it is clear that the peak transconductance occurs at the tapering ratio of 0.7. As the tapering ratio changes the threshold voltage also gets shifted. But the shifting occurs only in small amount. The shifting of threshold voltage with respect to the threshold voltage of cylindrical nanowire for various tapering ratio is shown in Fig.7a. Here the ΔV_{th} is the difference the threshold voltage of tapered and cylindrical nanowires. That is,

$$\Delta V_{th} = V_{th}(\text{cylindrical}) - V_{th}(\text{conical})$$

As the diameter of the channel near the drain decreases, the gate control over the channel increases. As a result the short channel effects like Drain Induced Barrier Lowering decreases. This is shown in Fig.7b. The DIBL has reduced to 72mV/V for the tapering ratio of 0.7. For tapering ratio of 0.6, the DIBL is decreased further to 18mV/V. But for tapering ratio less than 0.6, the threshold voltage increases and g_m decreases. So Conical Channel MOSFET (CCMOSFET) has more immunity to short channel effects compared to cylindrical channel MOSFET and the optimized tapering ratio can be in the range of 0.7 to 0.8.

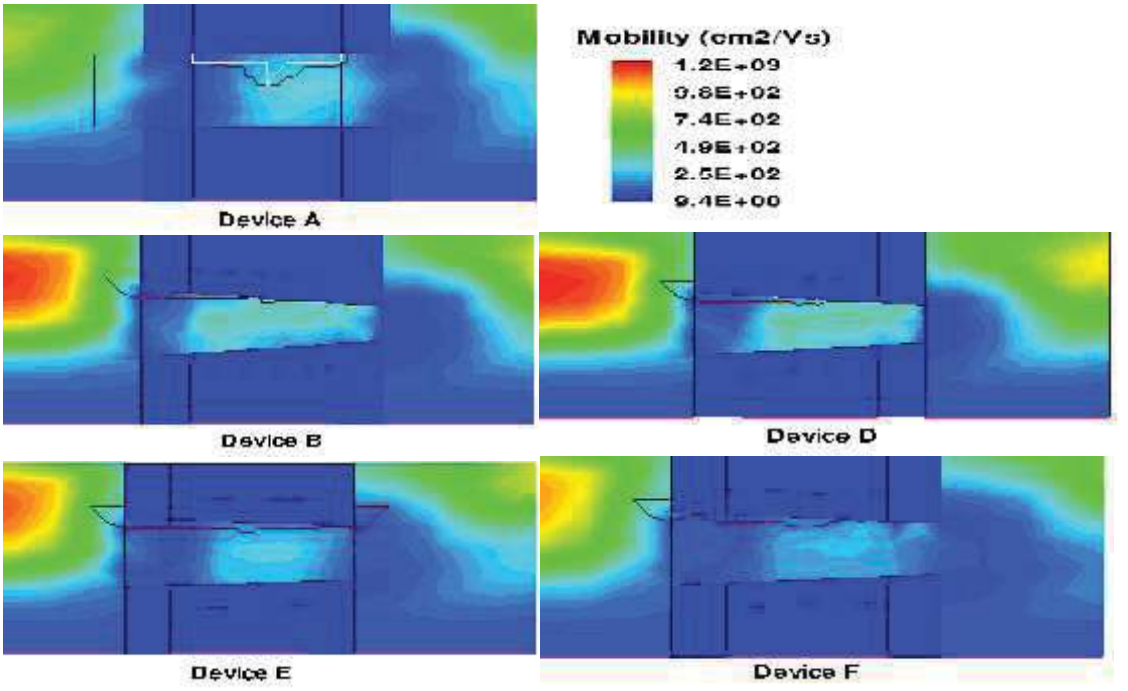


Fig.5. Mobility variation along the channel for various tapering ratios

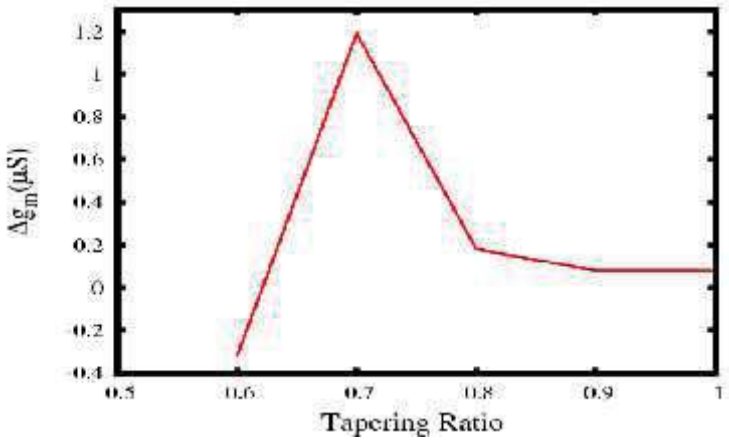


Fig.6 Variation of transconductance with tapering ratio

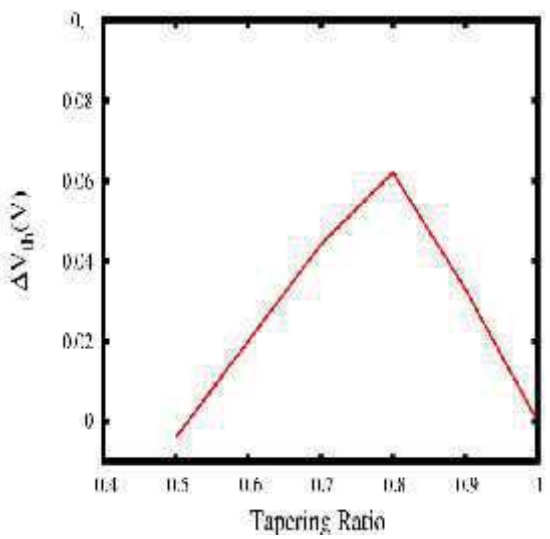
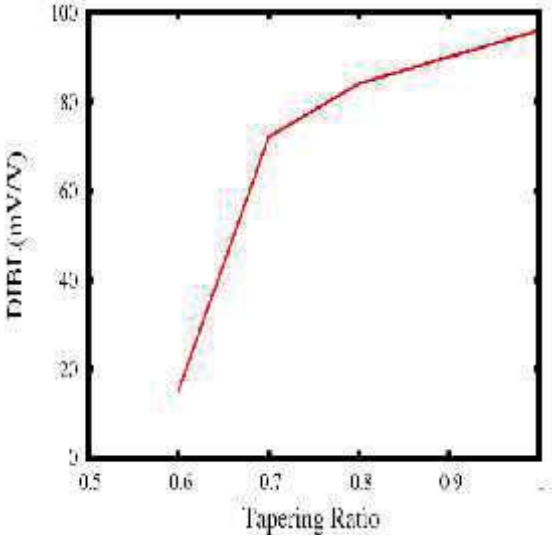


Fig.7 a) Threshold voltage shift for different tapering ratios



b) DIBL variation with tapering ratios

3. Conclusion

From the simulation results, it is clear that the Conical Channel MOSFET (CCMOSFET) has improved mobility. It helps to improve the performance by increasing the ON-current. The transconductance also get increased due to improved mobility. It shows that the peak value of transconductance is at tapering ratio of 0.7. The optimized tapering ratio is in the range of 0.7 to 0.8. Also at this tapering ratio the DIBL is also reduced much giving immunity to short channel effects. From the analysis, it is clear that the Conical Channel MOSFET (CCMOSFET) is a promising candidate for the nanoelectronics.

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