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High-speed sub-threshold operation of carbon nanotube interconnects

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Abstract: Sub-threshold voltage operated circuits are the future for ultra-low-power applications. These circuits are inherently slow due to the very small sub-threshold currents. Here, the authors propose two approaches for improving the speed of SWCNT bundle interconnects driven by CNTFET-based circuits under sub-threshold conditions. First, the authors modulate the channel length of the CNTFETs that are used in the driver circuits to increase sub-threshold output current. The output current is maximum when the channel length is optimised to 15 nm. Second, the authors design driver circuits made of CNTFET-based inverters and transmission gates for SWCNT bundle interconnects at sub-threshold voltages. The authors consider five different configurations of the driver and load circuits. SPICE simulations show that transmission gates play a vital role in driver circuits by reducing the propagation delay and increasing the switching speed at high frequencies. Finally, the authors perform temperature-dependent analysis of the best cases from the proposed circuits and show that the propagation delay and power dissipated by them increases drastically at increased temperatures up to 500 K.

1 Introduction

Carbon nanotube interconnects are found to be ideal candidates in scaled down ICs to carry power, ground, clock, and transistor-level signals, compared to existing Cu interconnects which suffer from high resistance, grain boundary scattering, and electromigration [1–4]. The last decade has seen extensive research on modelling, design, fabrication, and testing of CNT-based VLSI interconnects [5–12]. Based on the successful operation of multi-walled CNT (MWCNT) interconnects at 1 GHz [7, 8], researchers have proposed them for use in sub-threshold voltage-operated circuits [13–15]. The performances of these circuits are characterised by the speed at which they operate and the amount of power they dissipate. For scaled down ICs, reducing the supply voltage (V_{dd}) to sub-threshold levels is inevitable to achieve low-power operation. Whereas smaller V_{dd} makes the circuits slower as the circuit RC delay becomes dominant.

Recent advancements in CNT interconnect design for sub-threshold circuits show that single SWCNTs are suitable as local interconnects as they have less delay due to small wire capacitance [15]. They are driven by big transistors with a W/L ratio of 5 for nFETs and 10 for pFETs, which makes the driver resistance dominant. Again, for global interconnects, the driver width was changed to make the driver resistance higher than the interconnect resistance [16]. Basically, this technique is used to increase the sub-threshold output current of the drivers. In the case of CNT bundle interconnects, the resistance was decreased by increasing the number of metallic CNTs in the bundle at the cost of increased capacitance [16].

However, these conventional methods cannot enhance the performance of sub-threshold circuits at scaled technologies. The idea of up-scaling transistors for higher resistance [14, 16] does not go well with 'scaling-down' approach. Further, the overall path delay of the circuit remains high as the driver is optimised for higher output current and not for lesser delay. This leads to the slower performance of circuits at sub-threshold voltages than at super-threshold voltages. Recent findings from fabrication of graphene nanoribbon interconnects for sub-threshold FPGAs shows that they operate at about 150 KHz only [17]. For long global interconnects, buffer insertion is not feasible when they conduct sub-threshold current [14, 16]. Pable and Hassan (2012) [14] suggested for dynamic threshold MOSFETs (DTMOS) as drivers to avoid use of repeaters. The DTMOS consumes high dynamic power and are not suitable for low-power operation.

High speed operation and low-power consumption in scaled down circuits at sub-threshold region can be achieved by using nanoscale transistors like FinFETs [18], CNTFETs [19–21], or GNRFETs connected by CNT interconnects.

Here, we propose two approaches to tackle the issues of small sub-threshold currents and high propagation delay in scaled integrated circuits. First, we modulate the channel length and width of the CNTFETs that we propose to use in driver circuits. We find an optimal length and width of the FETs where the output sub-threshold current is maximum so that the interconnects can conduct the input signals faithfully. This is also the optimal width and length for least possible resistance and capacitance of the driver, respectively. Second, we design new driver and load circuits using transmission gates (T-gates) along with inverters to drive SWCNT bundle interconnects at sub-threshold voltages. We utilise the pull-up/pull-down operation of the T-gates, which gives a full swing of the output waveform as well as their lesser dynamic power consumption to our advantage at sub-threshold voltages. By doing so, we were able to reduce the propagation delay and thereby increase the speed of the interconnects.

Further, we study the effects of temperature on the performance of sub-threshold circuits. Rai et al. (2016), (2017) [22–25] and other groups [22–28] have studied the temperature-dependent performance of SWCNT bundle, mixed CNT bundles, and multi-layer graphene nanoribbons (MLGNR) interconnects. In all their studies, temperature plays a major role in determining the propagation delay and power dissipated by the interconnects. The main reason behind this phenomenon is the temperature dependence of the mean free path (MFP) which in turn increases the wire resistance. So, we consider both temperature-independent and temperature-dependent analysis of sub-threshold interconnects to find out the impact of temperature on their performance. Here, we do the analysis of SWCNT bundle interconnects. However, this can be extended to MWCNT, mixed CNT bundle (MCB), and ML-GNR interconnects also in the future.

2 CNTFET current model

CNTFET is regarded as the most advanced device which has similarities of MOSFET but has an advantage of working in

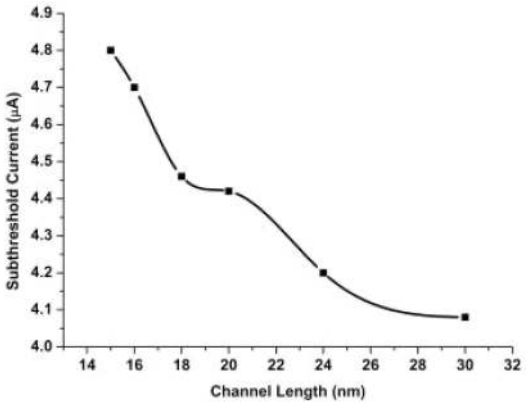

Fig. 1 *Sub-threshold current for different channel lengths of the CNTFETs in an inverter*

ballistic regime [19, 29]. The threshold voltage in a CNTFET is dependent on the diameter of the CNTs used in the channel and is expressed as

$$V_{th} \simeq \frac{E_g}{2e} = \frac{a_0 V_\pi}{eD_{CNT}} \simeq \frac{0.43}{D_{CNT}} \tag{1}$$

where,e is the unit electron charge, E_g is the CNT bandgap, V_π is the carbon π-π bond energy and D_{CNT} is the diameter of the CNT given by

$$\begin{aligned} D_{CNT} &= \frac{\sqrt{3}a_0\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \\ &= 0.0783\sqrt{n_1^2 + n_1 n_2 + n_2^2} \end{aligned} \tag{2}$$

where (n_1, n_2) is the chiral number, a_0 is the carbon-carbon bond length which is 0.142 nm [29]. For a CNT with chiral indices (n_1, n_2) as (19, 0), its diameter is 1.5 nm and the threshold voltage is 0.3 V. The ON current in a CNTFET is influenced by the channel length L_{ch}. It can be expressed as

$$I_{CNTFET} = \frac{N g_{CNT}(V_{dd} - V_{th})}{1 + g_{CNT} L_{ch} \rho_S} \tag{3}$$

where N is no. of CNTs in the channel, g_{CNT} is the transconductance per CNT, ρ_S is the resistivity of the CNT channel. This is the sub-threshold current of the CNTFET that we use in our design of driver and load circuits here.

3 Transistor sizing for sub-threshold operation

The overall RC delay of the circuit depends on the driver resistance (R_{driv}) and capacitance (C_{driv}). By changing the size of the length and width of the transistor, one can change the RC delay as well as the output current (sub-threshold current) of the driver [30]. The threshold voltage in a circuit is reduced when the width of the transistors is reduced. This is called inverse narrow width effect (INWE) [31]. Ideally, minimum-sized drivers are necessary for high speed and low power circuits. However, it must be noted that the current is not minimum when the width is minimum [32].

As per (3), I_{CNTFET} is dependent on transistor channel length. However, traditionally, sizing of the transistor was mainly done by decreasing the width and not the length, for sub-threshold operation [14–16]. While scaling of the gate width reduces capacitance (given as $C_{CNTFET} = N \,.\, C_{CNT} + C_{gate}$ [19]), scaling of channel length reduces resistance. The expression for the width of the gate of the CNTFET is given by

$$W_{gate} = \mathrm{Min}(W_{min}, N_g \,.\, pitch) \tag{4a}$$

where W_{min} is the minimum width of the gate and N_g is the number of nanotubes under the gate [19].

So, by varying both the length and width of the transistor, we are able to reduce the driver RC delay and hence, increase the speed of the circuit.

We use CNTFETs for constructing the driver and load circuits for sub-threshold operation of CNT interconnects. Recent work on CNTFET device fabrication shows that they are ideal for sub-threshold operation [33, 34]. Scaling of channel length and contact length of the device to as low as 15 and 20 nm, respectively, was found to be feasible without any short channel effects (SCE) and drain induced barrier lowering (DIBL) effects. Further, the drain current I_d for 15, 300 and 3 μm channel lengths is around 5, 3, and 1.5 μA, respectively, for an input voltage of 0.25 V [18]. The relation between the channel length and the total resistance, R_{tot} of the device can be given as

$$R_{tot} = \frac{h}{2e^2 M}\frac{L_{ch}}{L_{mfp}} + 2R_C \tag{4b}$$

where $h/2e^2$ is the quantum resistance per channel of a CNT, L_{ch} is the channel length, L_{mfp} is the MFP for phonon scattering, M is the number of modes per channel, $M = 2$ for a CNT and R_C is the contact resistance. This is because, the contact resistance is dependent on the length of the nanotube-metal contact and the diameter of the CNT in a CNTFET given by

$$R_C = \frac{\rho_C}{L_C \times d_{CNT}} \tag{4c}$$

For sub-threshold operations, it is necessary that the contact resistance must be as low as possible to maintain a good sub-threshold swing. So, the contact length L_C must be increased to get a lower R_C. For around 50 nm contact length, the contact resistance will be around 10k Ω as modelled in ref. 18.

The shortest channel length of 15 nm showed highest room temperature conductance of $0.7G_0$ (where G_0 is the conductance of a CNT given as $2e^2/h$) and transconductance of 40 μS. The channel resistance was measured from 9 to 11 kΩ which is closer to the nanotube quantum resistance of 6.45 kΩ. So, we take advantage of these effects of nanoscale CNTFETs and use them in our driver circuit design.

The inverter is made by VS-CNTEFT model library provided by Stanford University [35]. By varying the channel lengths of n-CNTFET and p-CNTFET, we are able to modulate its channel resistance and identify the point where maximum sub-threshold current flows through the driver circuit. Fig. 1 shows the sub-threshold current for different transistor channel lengths of the CNTFET-based inverter circuit. It can be seen that the current is maximum at 15 nm channel length which is in good agreement with ref. 18. Even though the current reduces in the order of 0.1 μA for higher lengths, it is always better to have maximum possible current in the circuit so that there is least propagation delay. Further, the devices have a very small inverse sub-threshold slope of only 90 mV/decade, which means that the devices can switch faster. Further analysis of threshold current variations at different channel lengths (100 nm<L_{ch}<3000 nm) can be found in [33].

Now, we perform SPICE analysis of a SWCNT bundle interconnect driven by a CNTFET-based inverter. The equivalent circuit model of the CNT interconnects considered here is described in Section 5. Fig. 2*a* shows the driver-interconnect-load model for our simulation setup. A 0.3 V pulsed voltage is applied to the inverter. The output voltage at the load side of the interconnects is plotted in Fig. 2*b*. It can be seen that the output waveform switches completely from V_{dd} to 0 V, which is a major step towards high-speed operation of sub-threshold currents. In order to capture the rising and falling trend of the output, we have used input waveforms with very short rise time or fall time which is 0.001 times smaller than time period. However, the delay of the circuit is still higher at 70 ns for high-speed operation of the

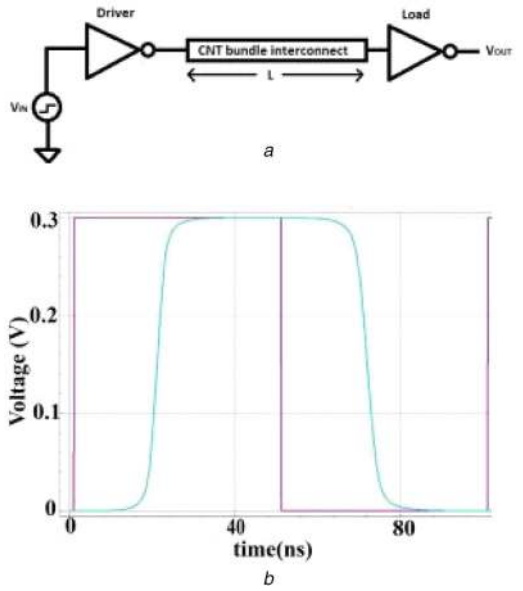

Fig. 2 *Inverter-wire-inverter model considered as case-1 in this paper*
(a) Driver-interconnect-load model, ***(b)*** Transient input and output waveform

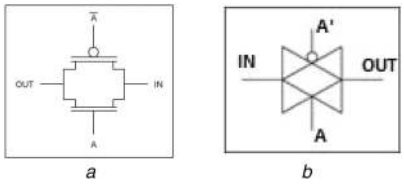

Fig. 3 *Transmission gate*
(a) Circuit connection, ***(b)*** Circuit symbol

circuits. The circuit worked at around 500 MHz which is roughly half of the speed at which current circuits work.

So, to overcome the speed and delay issues, we propose to use new driver circuits that are made of transmission gates and inverters. Ultimately, we take advantage of scaling of the channel length of the devices as well as using of transmission gates in the driver circuits of the sub-threshold interconnects.

4 Proposed circuit models

4.1 CNTFET-based transmission gate model

Transmission gates (T-gates) are used in many applications like fast analogue switch, logic gates, analogue multiplexer in ADCs, control logic in programmable FPGAs etc. Particularly, their high speed switching action which is a result of good pull-up/pull-down capability is utilised here to speed up sub-threshold circuits. Typically, a transmission gate is made up of two transistors, an nFET and a pFET, connected in parallel as depicted in Fig. 3*a* and its circuit symbol is shown in Fig. 3*b*. The gates are connected to complementary inputs, while the source takes the input signal and drain gives the output. If the nFET is fed with logic 1 and pFET with logic 0, the T-gate is ON, thereby passing the input signal to the output. For reverse logic, the T-gate is OFF.

We construct the T-gates using CNTFET libraries described in [35]. Various parameters of the model that we use in our work are enlisted in Table 1. From our analysis in the previous section, we take the channel length of the pFET of the inverter, pFET and nFET of the T-gate are 15 nm when the current is maximum.

4.2 Driver-interconnect-load models

We follow a driver-interconnect-load (DIL) model that describes the circuits made of inverters and T-gates as drivers and loads for CNT bundle interconnects. Throughout, our main motivation is to use the T-gate as a driver to pull-up the signals to V_{dd} during ON state and to pull-down the signals to 0 V during OFF state. In this

Table 1 Parameters from VS-CNTFET library [35]

Parameter	Value
sub-threshold V_{DD}	0.3 V
inverter nFET Channel length (L_{ch})	10–24 nm
chirality of CNTs	(19,0)
no. of CNTs in channel(N_g)	3
diameter of each CNT	1.5 nm
gate capacitance for L_{ch} = 18 nm	3.6 aF
I_{on}/I_{off} for nFET	1.9×10^4
I_{on}/I_{off} for pFET	2.8×10^4
width of metal gate (W_{gate})	6.4 nm
CNT-metal contact resistance (R_C)	10 kΩ
gate capacitance (C_{gate})	78 aF
inverter pFET length	15 nm
t-gate nFET and pFET length	15 nm

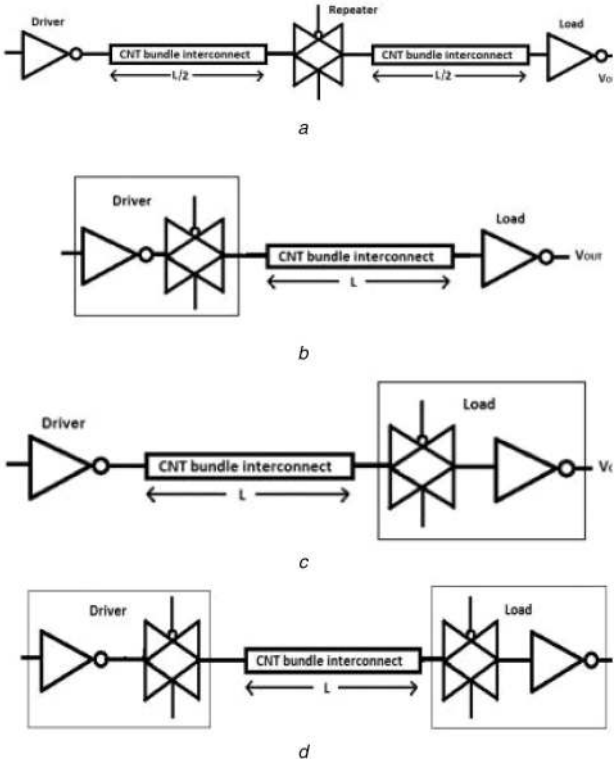

Fig. 4 *Different DIL models considered here*
(a) Case 2: INV – wire - T-Gate - wire- INV model, ***(b)*** Case 3: INV - T-Gate – wire - INV model, ***(c)*** Case 4: INV - wire - T-Gate - INV model, ***(d)*** Case 5: INV – T-Gate – wire –T-Gate -INV model

work, we consider different cases of using T-gates along with the inverters in driver and load circuits as shown in Fig. 4.

In case 1, we use a standard inverter as driver and load as shown in Fig. 2*a*. We take this circuit as our reference for comparison purposes. The rest of the cases are shown in Figs. 4*a*–*d*. Case 2 is intended to use the T-gate to drive the sub-threshold signals from the centre of the wire, i.e. we use it as a buffer at 500 μm length. Next, in case 3, we use a T-gate just after the inverter so that both the inverter and T-gate can act as the driver when combined. In case 4, T-gate is placed before the load inverter. This is to study the effect of signals at the load when a T-gate is used at the load side. In case 5, we use two T-gates, one after the driver and another before the load, so that the signals at both driver side as well as load side can be analysed. The driver and load resistance is set by selecting the channel length of the n-CNTFET and the p-CNTFET. We choose the channel length of both nFET and pFET to be 15 nm so that the channel resistance is minimum [18].

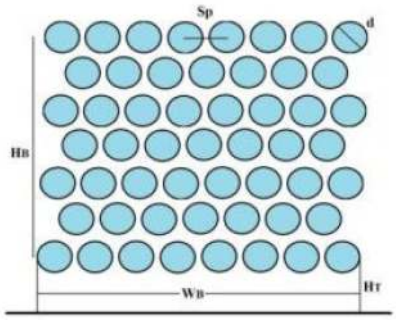

Fig. 5 *SWCNT bundle interconnect model*

Normally, sub-threshold signals are slow in transitioning from low to high and vice versa as the RC charging time of the interconnect is much larger than the signal transition time at high frequencies. This is the main limitation of sub-threshold circuits when they operate at high frequencies. Nevertheless, we use the fact that device and interconnect scaling can be done simultaneously with voltage scaling to achieve better speed.

5 SWCNT bundle interconnect model

Single-walled carbon nanotubes (SWCNTs) are found to be good candidates as interconnects for VLSI circuits [36].

However, owing to its high resistivity of 6.45 kΩ/μm, researchers are forced to think of using bundles of SWCNTs so that the overall interconnect resistance is reduced. We use an equivalent single conductor transmission line model (ESC-TL) here to describe the conducting behaviour of SWCNT bundle interconnects. The transmission line equations of the voltage and current through an SWCNT bundle interconnect as depicted in Fig. 5 can be given as

$$\frac{\partial V(z,t)}{\partial z} + L\frac{\partial I(z,t)}{\partial t} + RI(z,t) = 0 \tag{5}$$

$$\frac{\partial I(z,t)}{\partial z} + C\frac{\partial V(z,t)}{\partial t} = 0 \tag{6}$$

Considering an individual CNT in a SWCNT bundle, the number of conducting channels that contribute to its electrical conduction is given as

$$N_i = \begin{cases} aTD_i + b, D_i > d_T/T \\ 2, D_i < d_T/T \end{cases} \tag{7}$$

where T is temperature in kelvin, D_i is the diameter of the ith shell, $a = 3.87 \times 10^{-4}$ nm^{-1}K^{-1}, $b = 0.2$, and $d_T = 1300$ nmK.

The interconnect resistance is dependent on its effective MFP λ_{eff} (MFP) as explained by Rai et al. (2017) [23–25]. The factors that affect λ_{eff} are the optical phonon and acoustic phonon scattering mechanisms, which have different scattering MFPs at different ambient temperatures. The MFP due to acoustic phonons can be given as [22–27]

$$\lambda_{AC} = \lambda_{AC.300}\left(\frac{300}{T}\right) \tag{8}$$

where $\lambda_{AC.300}$ is the acoustic phonon MFP at 300 K which is roughly 1.6 μm. The second contribution to λ_{eff} is the optical phonon scattering. So, both optical absorption ($\lambda_{OP.abs}$) and optical emission ($\lambda_{OP.ems}$) need to be considered which can be given as [22–27]

$$\lambda_{OP.abs} = \lambda OP.300\left(\frac{N_{OP}(300)+1}{N_{OP}(T)}\right) \tag{9}$$

$$\lambda_{OP.ems} = \frac{1}{\lambda_{OP.ems}^{fld}} + \frac{1}{\lambda_{OP.ems}^{abs}} \tag{10}$$

$$\lambda_{OP.ems}^{fld}(T) = \frac{\hbar\omega_{OP}}{e.Vdd}l + \frac{N_{OP}(300)+1}{N_{OP}(T)+1}\lambda_{OP.300} \tag{11a}$$

$$\lambda_{OP.ems}^{abs}(T) = \lambda_{OP.abs}(T) + \frac{N_{OP}(300)+1}{N_{OP}(T)+1}\lambda_{OP.300} \tag{11b}$$

where $\lambda_{OP.ems}^{abs}$ is the optical emission MFP after absorption, $N_{OP}(T) = (1/[\exp(\hbar\omega_{OP}/K_BT) - 1])$, $\lambda_{OPems}^{fld}(T)$ is the former optical emission MFP event, $\hbar_{OP}$ is the optical energy (0.18 eV) and $\lambda_{OP.300}$ is the spontaneous optical emission at 300 K which is roughly 15 nm. So, the effective MFP λ_{eff} can be given as

$$\frac{1}{\lambda_{eff}(T)} = \frac{1}{\lambda_{AC}} + \frac{1}{\lambda_{OP.abs}} + \frac{1}{\lambda_{OP.ems}} \tag{12}$$

Considering these facts, the MFP and temperature-dependent resistance of a CNT bundle can be given as

$$R_b(T) = \frac{R_{\text{SWCNT}}}{n_B} = \frac{R_c + R_Q}{n_B}l < \lambda_{eff} \tag{13a}$$

$$R_b(T) = \frac{R_{\text{SWCNT}}}{n_B} = \frac{R_c + R_S}{n_B}l > \lambda_{eff} \tag{13b}$$

$$R_Q = \frac{h}{4e^2}; R_S = \frac{h}{2N_ie^2}\left[\frac{l}{\lambda_{eff}(T)}\right] \tag{14}$$

where n_B is the total number of CNTs in a bundle. The temperature-dependent expressions of the ESC inductance of a CNT bundle can be given as

$$L_{ESC}^b(T) = \frac{L_m + (L_k/N)}{n_B} \tag{15}$$

where L_m and L_k are the magnetic and kinetic inductances of an isolated CNT. They can be given by the expressions

$$L_m = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right); L_k = \frac{h}{2e^2\upsilon_f} \tag{16}$$

Similarly, the effective capacitance of a CNT bundle placed on a ground plane is the series combination of the electrostatic and quantum capacitances of the CNT bundle.

The relevant expressions are:

$$C_{ESC}^b(T) = \left(\frac{C_E^b \times C_Q^b}{C_E^b + C_Q^b}\right) \tag{17}$$

$$C_E^b = n_W \times \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{y}{d}\right)}; C_Q^b = n_B \times \frac{2Ne^2}{h\upsilon_f} \tag{18}$$

where n_W is the number of CNTs along the width of the bundle given in (20), h is Plank's constant, v_f is the Fermi velocity, e is charge of electron, y is the separation between CNT and ground plane and d is the diameter of the CNT. The electrostatic capacitance of the bundle is calculated by considering only the outer CNTs in the bundle as the inner CNTs are not capacitively coupled to the substrate due to the shielding effect of the outer CNTs. Table 2 gives the values of the ESC parameters computed from the above equations.

For 20 nm technology node, the width of the interconnect is 34 nm. Considering a square bundle of CNTs, the height is also 34 nm. The total number of CNTs in the bundle is computed from the following equations.

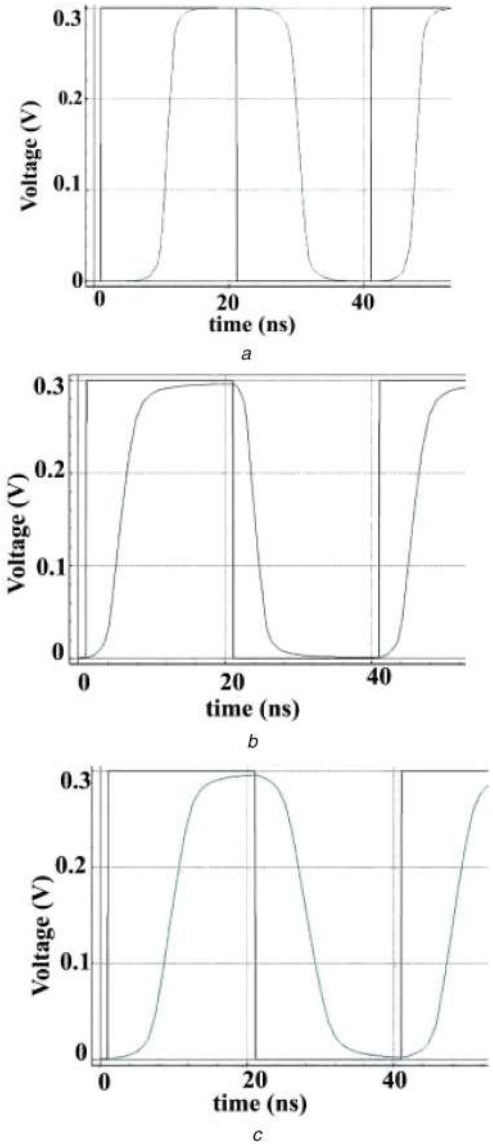

Fig. 6 *Input (maroon colour) and output (blue colour) waveforms of 500 μm, L_{ch} = 15 nm for inverter and T-gate*

(a) Case-1: Inv- Wire- Inv, ***(b)*** Case-3: Inv- T-gate- Wire- Inv, ***(c)*** case-4: Inv- Wire- T-gate- Inv

The number of CNTs along the width (W) is n_W and the number of CNTs along the height (H) of the bundle is n_H. Each CNT is having a diameter d of 1 nm. Then, the total number of CNTs can be found as

$$n_{CNT} = \begin{cases} n_W n_H - (n_H/2), & n_H \text{ is even} \\ n_W n_H - [(n_H - 1)/2], & n_H \text{ is odd} \end{cases} \quad (19)$$

where n_{CNT} is the total number of CNTs in the bundle and

$$n_W = \left\lfloor \frac{W_B - d}{S_p} \right\rfloor \text{ and } n_H = \left\lfloor \frac{H_B - d}{S_p} \right\rfloor \quad (20)$$

S_p is the centre to centre distance of adjacent tubes and is 1.34 nm here, considering the van der Vaal's gap δ of 0.34 nm. So, the total number of CNTs in our CNT bundle interconnect is 564.

6 Analysis of proposed driver/load circuits

6.1 Simulation results

First, we perform transient analysis of the proposed DIL circuit models using Silvaco SmartSPICE software.

Table 2 Interconnect parameters from equivalent single conductor model

Parameter	Value, per μm
R_{ESC}	11.436 Ω
$L_{k.ESC}$	14.18 pH
$C_{Q.ESC}$	225.6 fF
$C_{e.ESC}$	7.3157 pF

We developed the net-list codes for each case of driver/load configurations. V_{dd} is set to 0.3 V. A rise time and fall time of 0.1 ns is set. The time duration of ON state of the input signal is fixed at 20 ns and the time period is 40 ns. Fig. 6 shows the waveforms for 500 μm interconnect length.

It can be seen from Fig. 6*a* that the delay is higher for an inverter-driven wire. Whereas as we use a T-gate at the driver side as in case 3, the delay is substantially reduced while maintaining the same swing, as seen from Fig. 6*b*. Whereas when we used the T-gate at the load side, the same speed enhancement as in the previous case is not observed as can be seen in Fig. 6*c*. It also must be noted that these simulations are carried out for a CNTFET channel length of 15 nm that is used to construct T-gates and inverters. The main reason behind the delay reduction in case 3 and case 4 is due to the pull-up and pull-down action of the T-gate, which is absent in case-1.

Case 2, where, the T-gate is used as a repeater and case 5 where T-gates are used at both driver and load sides, are not appropriate for 500 μm interconnects. So, we skipped the waveforms for those cases here.

Next, we carry out simulations for 1000 μm interconnects for cases 1 to 5 whose waveforms are shown in Fig. 7. The delay is highest for case 1 and least for case 5 followed by case 3. In case 5, the T-gates at both driver as well as load side pulls up and down the waveform effectively. As a result, full swing is not achieved during ON state as the RC charging time is more than the time period of the input pulse. On the other hand, the delay is still lesser for case 3 due to the pull-up of the input signal by the T-gate. Here, a better ON state and OFF state are also maintained. For case 2 and case 4, the delay is higher than case 3 and case 5. This is because, in case 2, the T-gate at the centre of the interconnects cannot effectively pull-up the signal immediately after it enters the interconnect. For case 4 also, the T-gate at the load side cannot effectively pull-up the signal at the input side. Hence, increase in delay.

6.2 Temperature-independent performance analysis

The performance of sub-threshold circuits is based on its operating speed, power dissipated by the circuit components and the reliability of the signals that pass through the circuit. The most important factor that limits the speed of a sub-threshold voltage driven circuit is its current density. At smaller V_{dd}, the current is smaller as compared to nominal V_{dd}-driven circuits. Hence, we reduce the resistance and the capacitance of the driver and load circuits by adjusting the transistor length.

For an interconnect length of 500 μm, we compare the performance of cases 1, 3, and 4. From Fig. 8, we can observe that the delay is least for case 3. Case 4 has lesser delay than case 1. So, the best option is using T-gate at the driver side rather than in load side at 500 μm. This can be done at the expense of slight increase in power dissipation. The inverter and T-gate transistor length is 15 nm.

For a 1000-μm-long CNT bundle interconnect, we found that the propagation delay for different cases of driver and load circuitry. Also, we vary the transistor length of the inverter from 10 to 24 nm, Fig. 9*a* shows the propagation delay for different cases from 1 to 5.

As expected, the delay is lesser for cases 2, 3, and 5 where T-gates are used. Hence, the very reason for using T-gates in sub-threshold circuits is to reduce delay. Particularly, in cases 2 and 3 where we used T-gates as drivers, the delay is least for 15-nm channel length of the inverter (L_{inv}) where the current is maximum.

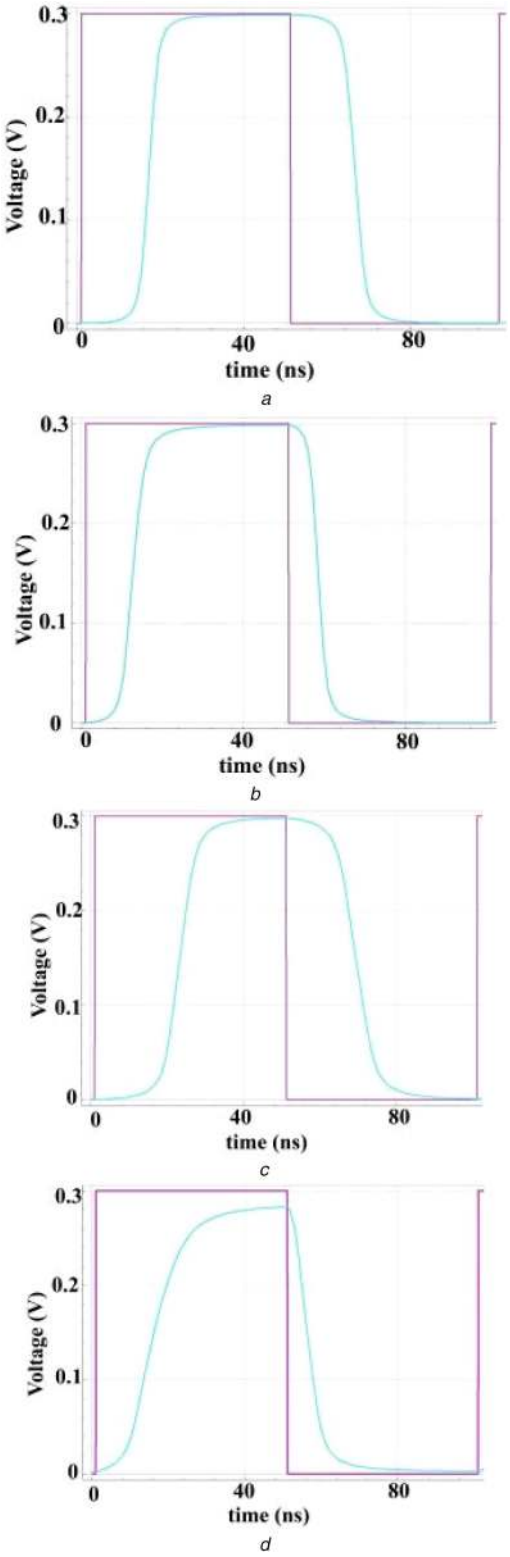

Fig. 7 *Input (maroon colour) and output (blue colour) waveforms of 1000 μm long wires, L_{ch} = 15 nm*
(a) Case-2, ***(b)*** Case-3, ***(c)*** Case-4, ***(d)*** Case-5

Delay increases as the length also increases in cases 2 and 3. The delay improvements for case 3 with respect to cases 1, 2, 4, and 5 are 83, 1.5, 82, and 2%, respectively.

In case 5, the delay is almost constant for all lengths. This is due to the fact that the T-gates at the driver side and load side are shielding the changes in the resistance of the inverter transistors in the driver as well as the load. This is very important as the process variations in the inverter circuitry is taken care by the T-gates, while maintaining lesser propagation delay.

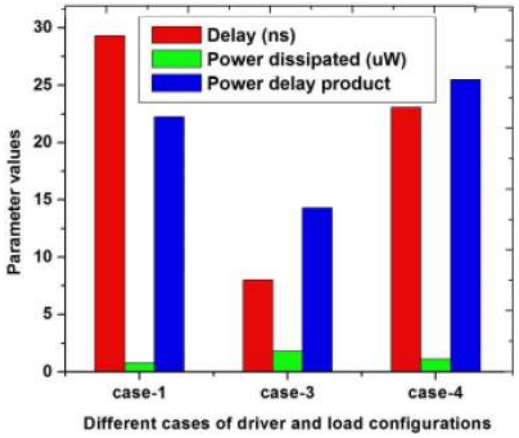

Fig. 8 *Comparison of parameters for cases 1, 3 and 4 for interconnect length of 500 μm*

The power dissipated by the circuits is shown in Fig. 9*b*. Due to the high resistance of the transistors at L_{inv} = 10 nm, the power dissipated by all the circuits is very high compared to other lengths.

For case 1, the power dissipation analysis did not converge in a solution for L_{inv} = 20 nm in the SPICE simulations. Further the power dissipated in case 5, where T-gates are placed at driver side and load side, is highest. The power required by the load side T-gate to pull-up and pull-down the signal is very high as the output from the driver inverter is not passed through a T-gate immediately. However, we found that the power dissipation for lengths other than 10 nm, is 2, 1, 0.8, and 2.2% higher in cases 2, 3, 4, and 5, respectively, when compared to case 1. Obviously, this is due to the T-gates in the circuits.

Next, the power delay product (PDP), which is a figure-of-merit for electric circuits, is calculated as depicted in Fig. 9*c*. Overall, T-gate circuits have smaller PDP than inverter-based circuits. This shows the dominating nature of the propagation delay rather than the power dissipation, on the performance of CNT interconnects. In each case, the PDP is higher for 10 nm length. Also, the PDP is highest in case 4 where T-gate is used at load side. The variation in PDP of case 4 is mainly due to the changes in the power dissipation at various lengths.

6.3 Temperature dependent performance analysis

Ambient temperature at which sub-threshold interconnects operate in ICs can be as high as 350 K [22–28]. This, in turn, can affect the OP and AC phonon MFP and hence, the resistance of the wire is as discussed in Section 5. So, their performance in terms of propagation delay and power dissipation is analysed in this Section. However, as we have found that case 2, case 3, and case 5 have less delay, power dissipation, and PDP, we take these cases as the best case for sub-threshold operation of interconnects. Hence, we do temperature-dependent analysis for these cases only with L_{ch} of 15 nm. The interplay between temperature and the channel length of the CNTFET can lead to more complex behaviour of carriers in the channel and we have not considered such analysis here. Nevertheless, we feel that 15-nm channel length is a good estimate even at higher temperatures as the carrier lifetime and mobility will decrease as the channel length increases with temperature. Since we are applying a voltage of 0.3 V which is still higher than the low bias voltage of 0.16 V, both acoustic and optical phonon scattering mechanisms are dominant and are considered for the resistance calculations.

From Fig. 10, we can notice the increase in the resistance of the interconnects due to the increased phonon scattering and reduced MFP. The kinetic inductance is dependent on the number of conducting channels which is again dependent on temperature as given by (3). So, as the number of conducting channels increases with temperature, the inductance decreases as per (15). The magnetic inductance is negligible and is temperature independent. The quantum capacitance is again dependent on temperature and

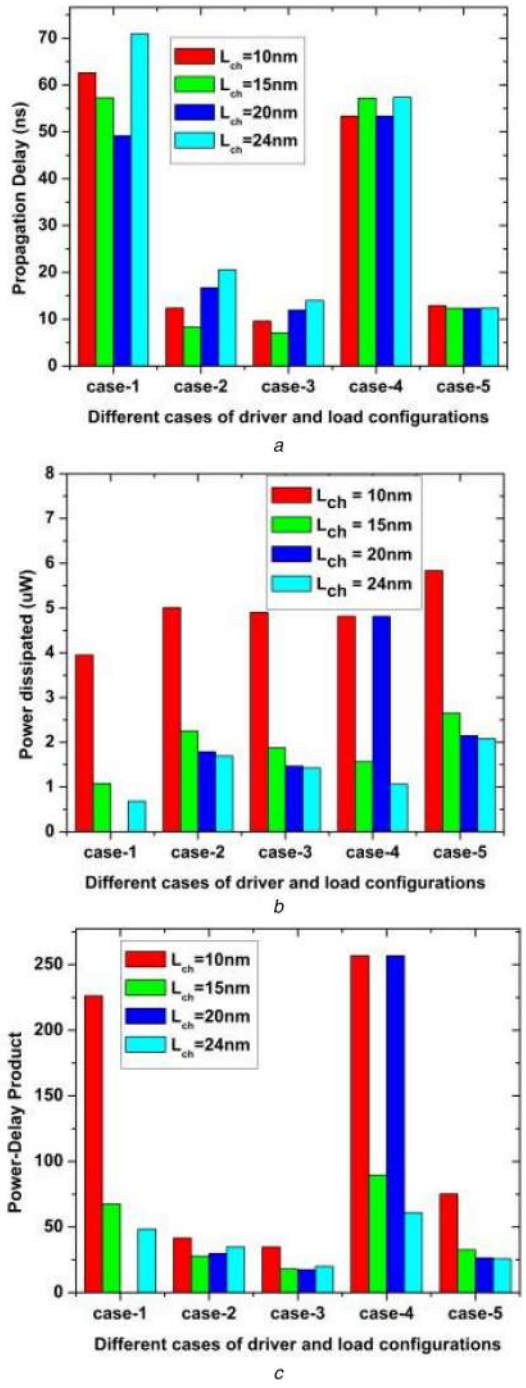

Fig. 9 *Output values for different cases as a function of different CNTFET channel lengths*
(a) Propagation delay, ***(b)*** Power dissipated, and ***(c)*** Power-delay product

the number of conducting channels. So it increases as the number of conducting channels increase due to temperature.

After incorporating the temperature-dependent resistances, capacitance, and inductance in the SPICE simulator, we have found out the propagation delay which increases with increase in temperature as shown in Fig. 11*a*. As a consequence, the power dissipated by the circuits also increases with temperature as shown in Fig. 11*b*. Among the three cases considered, the delay and power dissipation is least for case 3 compared to case 2 and case 5. As explained in the previous section, the main reason for the better performance of case 3 is due to the pull-up and pull-down action of the T-gate at the input side of the interconnect which drives the signals properly. This means that the high speed performance of sub-threshold CNT interconnects at increased temperatures is possible with higher power dissipation.

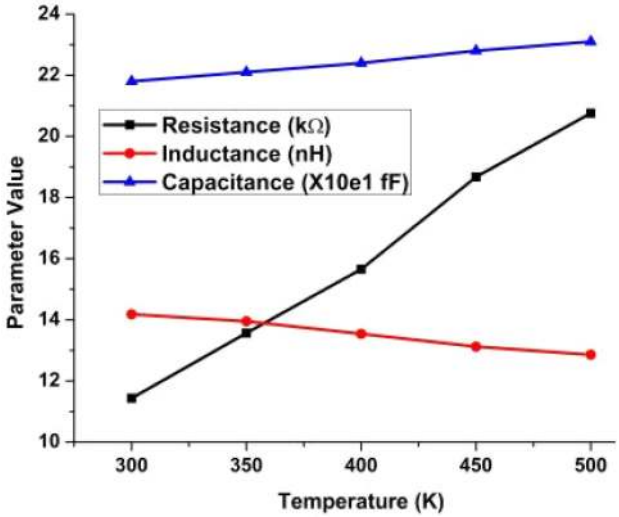

Fig. 10 *Resistance, inductance and capacitance vs. temperature*

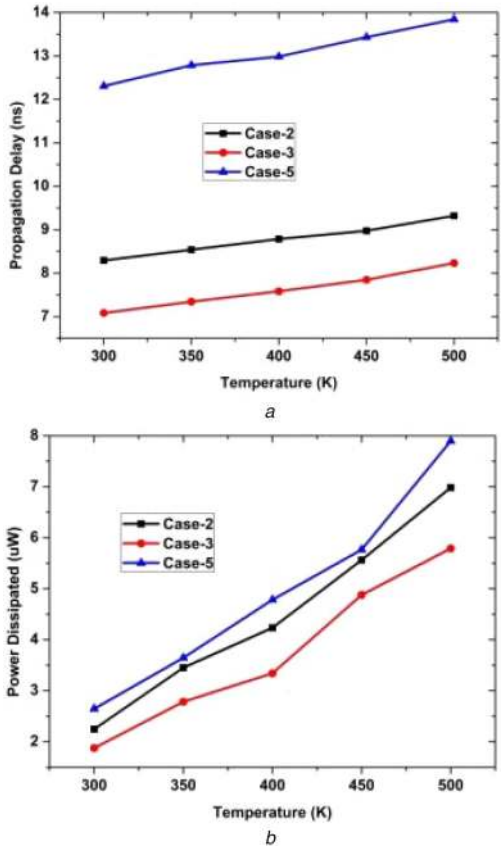

Fig. 11 *Temperature dependent performance of the best cases*
(a) Propagation delay, ***(b)*** Power dissipated

7 Conclusions

This paper has discussed two approaches for enhancing the speed of SWCNT bundle interconnects at sub-threshold operating voltages. Both the approaches of (a) scaling down of the channel length of the CNTFETs used in the driver circuits and (b) designing of new driver/load circuits using transmission gates and inverters made of CNTFETs showed good enhancement in the sub-threshold operation of SWCNT bundle interconnects. In the first approach, the channel length of the CNTFETs was scaled down to 15 nm, which yielded higher current in the interconnects to the tune of 5 μA. This approach was found to be attractive as the short channel effects and drain-induced barrier lowering are absent at such small channel lengths. In the second approach, we had designed driver circuits using CNTFET-based transmission gates and inverters. The T-gates played a vital role in reducing the switching time and

hence, enhanced the speed of the circuits. The overall path delay was substantially reduced compared to traditional approaches. Analysis of the circuits for 500 and 1000 μm long SWCNT bundle interconnects showed that the propagation delay was enhanced by 83% for case 2 where T-gate is used at the middle of the interconnect, compared to inverter-driven interconnects.

Further, the power dissipated is 1 to 5% higher for the cases where T-gates are used. Analysis of the PDP showed that the performance of SWCNT bundle interconnects is more dependent on the propagation delay than the power dissipated by them. Finally, temperature-dependent analysis shows that the propagation delay and power dissipation increase drastically at high temperatures, which show the limitations of the operation of sub-threshold interconnects at high temperatures.

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