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High step-up isolated efficient single switch DC-DC converter for renewable energy source

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KEYWORDS

Single switch DC-DC converter;
High step-up;
Clamp circuit;
Reverse-recovery;
PSIM

Abstract In this paper, an isolated high step-up single switch DC-DC converter for renewable energy source is proposed. In the proposed converter high step-up voltage is obtained by single power switching technique that operates low duty cycle with isolated transformer inductors and switched capacitors and power diodes. The disadvantage of conventional converters is that it has high duty ratio and high voltage stress on power devices with less efficiency. The proposed converter eliminates the switching losses and recycles the leakage energy which includes reverse recovery energy of the power diode by using passive clamp circuit. To achieve high output voltage gain, the isolated transformer primary terminal and secondary terminal are connected in series during switching operation. PSIM software has been used for simulation. Simulation circuit is analyzed at $40V_{dc}/400V_{dc}$, 200 W and this operation is validated by implementing in the hardware model at $12V_{dc}/120V_{dc}$, 60 W.

1. Introduction

In the recent years, the high step up dc-dc converters have played a vital role in renewable energy applications, such as PV systems, fuel energy systems, DC-back up energy system for UPS, grid system, high intensity discharge lamp and automobile applications. In order to connect them to the grid, the voltage level is adjusted according to the electrical network standards in the countries [13]. Earlier the environmental issues have accelerated the use of more efficient and energy saving technologies in renewable energy systems [14]. The boost converters are needed for increasing low dc voltage to high dc voltage. The conventional boost converters are not preferred, because with high voltage duty ratio it causes severe losses in power devices and high voltage stress across the switching devices, which generate high conduction losses and resulting in the increase in complicity. To eliminate the high duty cycle, capacitor switching technology is used [7]. These types of converters are used to reduce the voltage stress on power devices, but while turn on the switch more current pulse is passing through the power devices, thus causing damage. To avoid these disturbances, a small inductor is introduced in circuit and it avoids the sudden damages to power devices and diode reverse recovery problem is alleviated. The advantageous that switched capacitor method reduces power devices voltage stress but the disadvantage is the diodes that create a

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large current path which causes the conduction loss. To rectify this, active switch method adopted to increase the voltage gain and efficiency.

In active switch method the leakage energy is recycled via coupled inductor without wasting the energy. When switch is turned off, the leakage energy is recycled and improves the efficiency of the converter, thus choosing a low resistor value. Instead of active clamp circuit passive lossless circuit, is used [5]. The active clamp circuit shows better performance but in passive clamp circuit reduces the circuit complexity when compared to active clamp circuit. The passive lossless circuit is a simple design with a switched capacitor, coupled inductor obtain high voltage gain, non-isolated applications and high efficiency. By using the switched capacitor voltage stress is reduced on power devices and further voltage gain is increased.

The conventional boost converters are not able to provide high voltage gain [1]. High voltage gain with high efficiency can be achieved by the intergraded boost flyback converter system [2]. The investigation of high-efficiency clamped voltage dc-dc converter with reduced reverse-recovery current and switch-voltage stress and designed by the way of the combination of inductor and transformer to increase the corresponding voltage gain [3]. To reduce high device stress and large transformer size a high efficient pulse width modulation resonant single switch isolated converter proposed [12]. Here the proposed converter utilized the PWM which provided by the digital signal processor. The voltage clamped technology is used to reduce the switch voltage stress so that it can select the fast recovery diode in the output terminal for alleviating the reverse-recovery current and decreasing the switching and conduction losses [4].

When the implementation of passive lossless clamp circuit instead of an active clamp circuit to recycle the leakage energy simpler and easier to design [5,6], a switched capacitor circuit can achieve any voltage ratio, allowing for a boost of the input voltage to high values [7]. Isolated high boost dc-dc converters are suitable for renewable energy source. To achieve high output voltage gain the flyback converter output terminal and boost converter output terminal are connected serially with the isolated inductors with less voltage stress on controlled power switch and power diodes [8,9].

High boost isolated dc-dc converter with closed loop control can provide high voltage regulation control suitable for renewable energy source [11]. Further, this work can be proposed for the efficiency optimization and digitally controlling of the DC-DC converter over wide ranges of operating conditions [10].

The overall performance of the renewable energy system affected by the efficiency of step-up DC-DC converters, which are the key parts in the system power chain. The comparison and discussion of different high efficiency DC-DC step-up topologies performed [13]. And comparison of the synchronous-rectified Push–Pull converter with LLC DC to DC converter was deeply analyzed [14]. High power high efficiency boost DC-DC converters for the use in photovoltaic, fuel cell systems are discussed in view of power losses and efficiency [15].

In this paper, an isolated high step-up single switch DC-DC converter is proposed and implemented. In the proposed, converter high step-up voltage is obtained by single power switching technique operating low duty cycle with isolated transformer inductors and switched capacitors and power diodes. The proposed converter eliminates the switching losses and recycles the leakage energy. The isolated transformer primary terminal and secondary terminal are connected in series during switching operation. The output of the boost converter and isolated switched-capacitor cell are connected in series for high-step-up with a low turn-on ratio which has already been discussed [16]. PSIM software has been used for simulation. Simulation circuit is analyzed at $40V_{dc}/400V_{dc}$, 200 W and this operation is validated by implementing in hardware model at $12V_{dc}/120V_{dc}$, 60 W.

2. Proposed circuit diagram

The proposed isolated high boost converter with switched capacitor and single power switch is shown in Fig. 1. The passive lossless clamped circuit is proposed of a clamped capacitor (C_c) connected across IGBT switch is used to reduce the voltage stress. The V_c is the clamped capacitor voltage. The circuit is also connected with clamped diode (D_c). The clamp circuit recycles the energy stored in the leakage inductance. The voltage gain is obtained by significant value by providing a switched capacitor (C_s) and secondary inductor L_s and freewheeling diode (D_F). The switched capacitor voltage is given by V_{sc}. D_r is the regenerative diode the current flow through this diode is I_{dr}. The topology is modeled with an ideal transformer with corresponding turns ratio (N) equal to $n2/n1$. L_m is the magnetizing inductor L_k is the leakage inductance. Hence here the fast recovery diode used the capacitance effect of the depletion layer of the diodes neglected even reverse-recovery interval. The circuit is operated in six operating modes as explained below. The key operating waveforms are sketched in Fig. 2. V_{ce} and i_c are switch collector to emitter voltage and current. I_s - is the isolated transformer with secondary current. The clamp diode current is named as I_{dc} and clamp capacitor current named as I_c. V_F and I_F are the output freewheeling diode forward voltage and forward current.

3. Principle of operation

3.1. Mode I

Refer to the circuit shown in Fig. 3. in mode-I ($t_o - t_1$) switch(S) is turned ON state, the diode D_F and D_c are

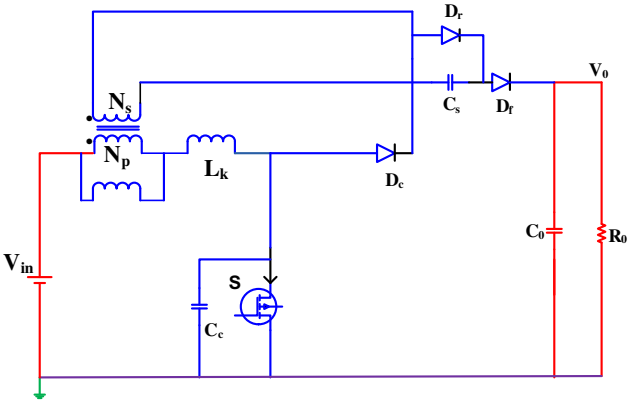

Figure 1 Proposed isolated high boost DC-DC converter.

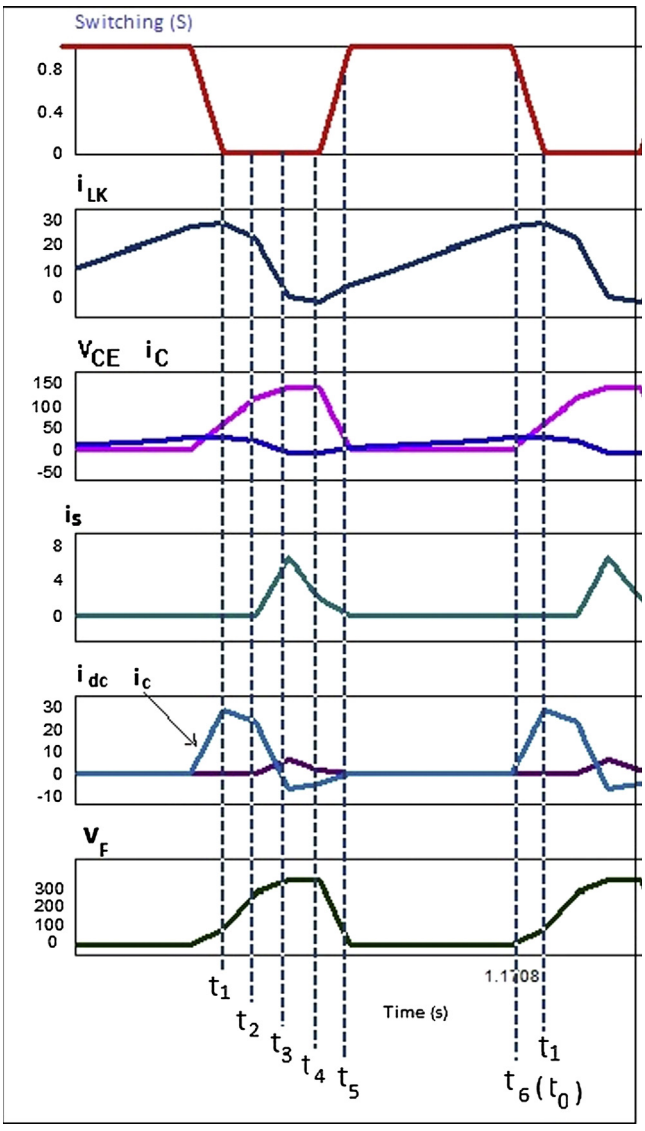

Figure 2 Proposed converter operating waveforms.

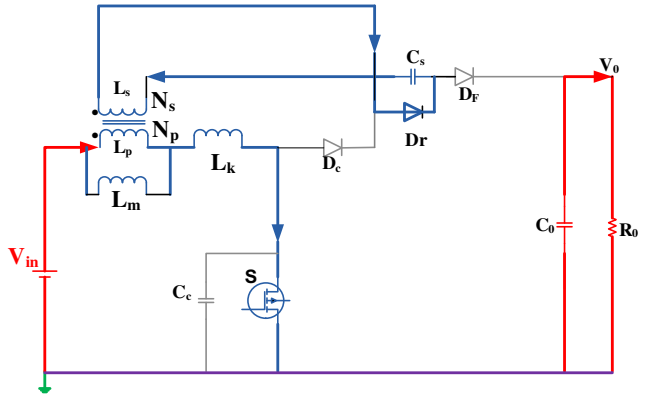

Figure 3 Proposed converter Mode 1 operation circuit.

operating in reverse bias and turn OFF, the magnetizing inductor (L_m) is charged by source (V_{in}) and the magnetizing current i_{lk} linearly increases the L_k resonate with switched capacitor C_s, through the

L_s and L_p inductors are connected via diode D_r. The current flow through the secondary winding is controlled by leakage inductor L_k and i_{lk} is given by,

$$\frac{V_{in(t_1)} - V_{in(t_0)}}{L_m + L_p} \approx i_{c(t_1)} - I_{c(to)} \approx i_{Lk(t)} \tag{1}$$

$$\frac{V_{in}(t_1 - t_0)}{L_m + L_p} \approx i_{c(t_1)} - I_{c(t_o)} \approx i_{Lk(t)} \tag{2}$$

The voltage equation is given by

$$V_{in} = V_{LK(t_0 - t_1)} + \frac{V_{CS}}{N} \tag{3}$$

$$V_{LK(t_0 - t_1)} = \frac{2L_K f_s I_o N}{D^2} \tag{4}$$

3.2. Mode II

The current path for mode-II ($t_1 - t_2$) is shown in Fig. 4. When switch is turned off at t_1 the I_c is started to decrease. Switching voltage is clamped to the capacitor voltage, then L_k resonate with switching capacitor (C_s) and clamped capacitor (C_c) so that the current through the leakage inductor i_{lk} linearly decreases through the secondary winding. L_k is discharged by the clamped capacitor voltage V_c.

$$\frac{V_C(t_2 - t_1)}{L_k} \approx I_{Lk(t_1)} - i_{Lk(t_2)} \tag{5}$$

$$\frac{V_C(t_1 - t_2)}{L_k} - I_{Lk(t_1)} \approx i_{Lk(t)} \tag{6}$$

3.3. Mode III

During mode-III ($t_2 - t_3$) Fig. 5 the secondary winding current down to zero, then the switching capacitor C_s employs throughout this period, the voltages of switching capacitor and clamped capacitor stay simultaneous, then switching capacitor is resonate with leakage inductor, and switching capacitance decreases, but at the same time leakage inductor current i_{lk} decreases. The secondary transformer current (I_s) is started raising. D_F and D_c carry the same current.

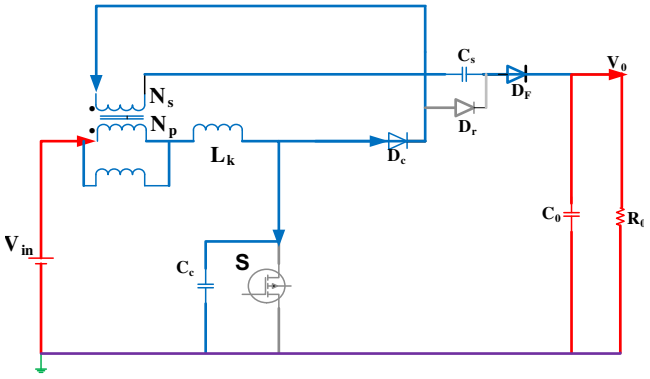

Figure 4 Proposed converter Mode 2 operation circuit.

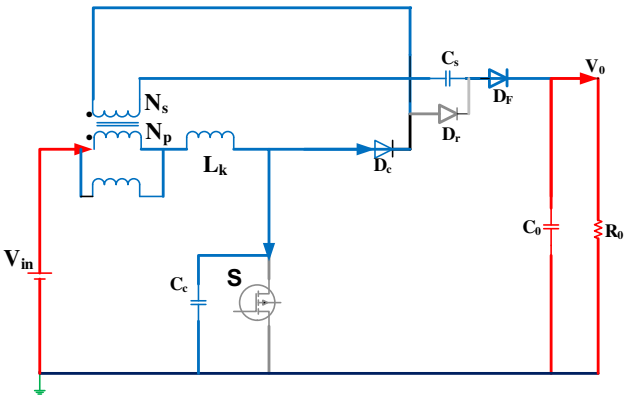

Figure 5 Proposed converter Mode 3 operation circuit.

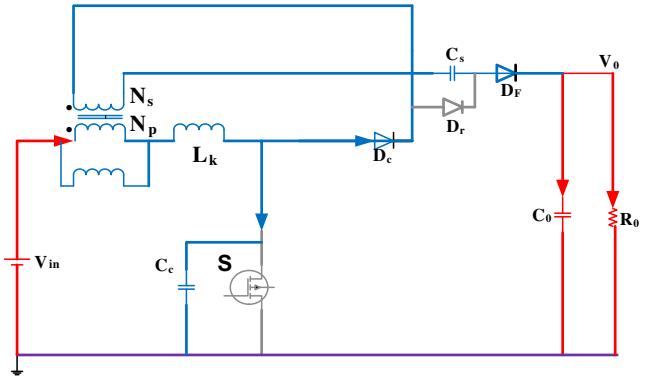

Figure 6 Proposed converter Mode 4 operation circuit.

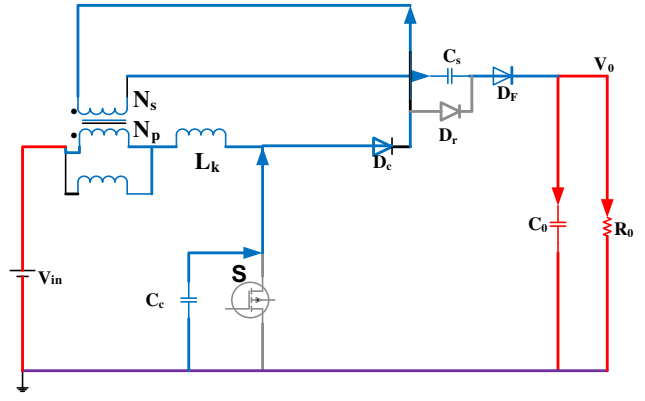

Figure 7 Proposed converter Mode 5 operation circuit.

$$\frac{V_o - V_c(t_3)}{L_k} \approx I_{Lk(t_2)} - i_{Lk(t_3)} \tag{7}$$

$$I_{Lk}(t_2) - \frac{V_o - V_c(t_3)}{L_k} \approx i_{Lk}(t) \tag{8}$$

3.4. Mode IV

Mode-IV ($t_3 - t_4$) is shown in Fig. 6. Here the switch is being turned off, the voltage across the switching capacitor is high

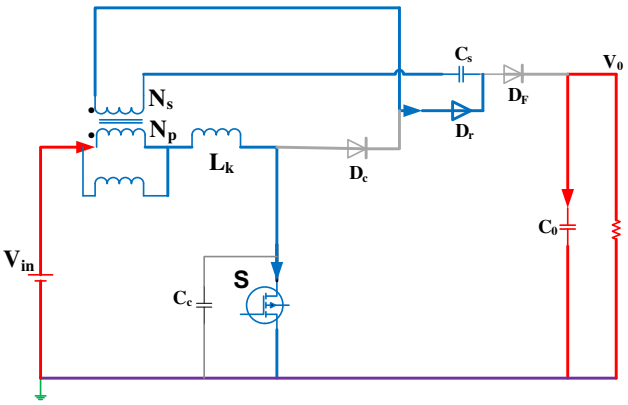

Figure 8 Proposed converter Mode 6 operation circuit.

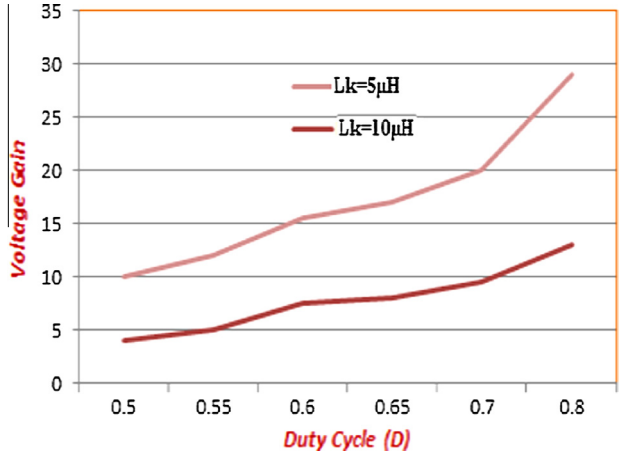

Figure 9 Leakage inductance and voltage gain relationship.

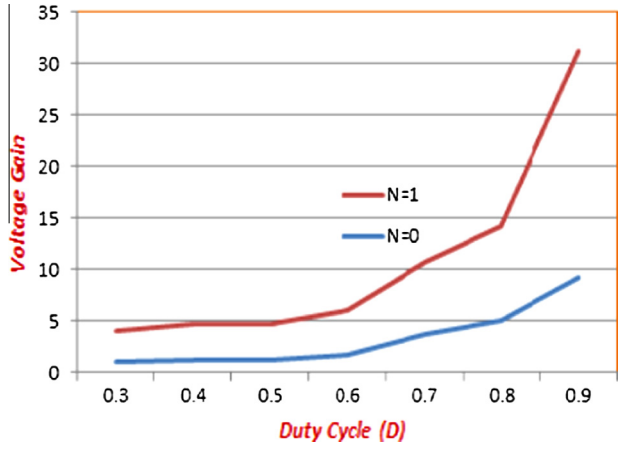

Figure 10 Voltage gain with different turns ratio.

and then the diode D_F is operated. The magnetizing inductor (L_m) releases the stored energy and sends its energy to load, and the parasitic capacitance of all the diodes is thus neglected as shown in Fig. 6. The isolated transformer secondary current I_s - is the maximum at this stage. In this mode L_k decreases

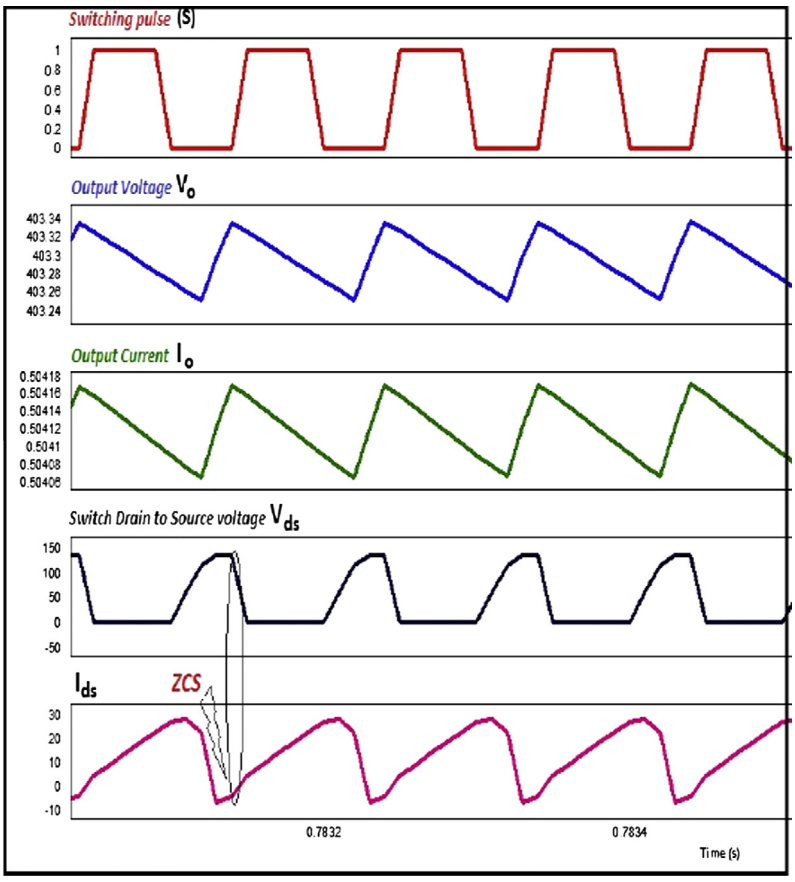

Figure 11 Waveforms of the proposed converter at rated input voltage (40 V).

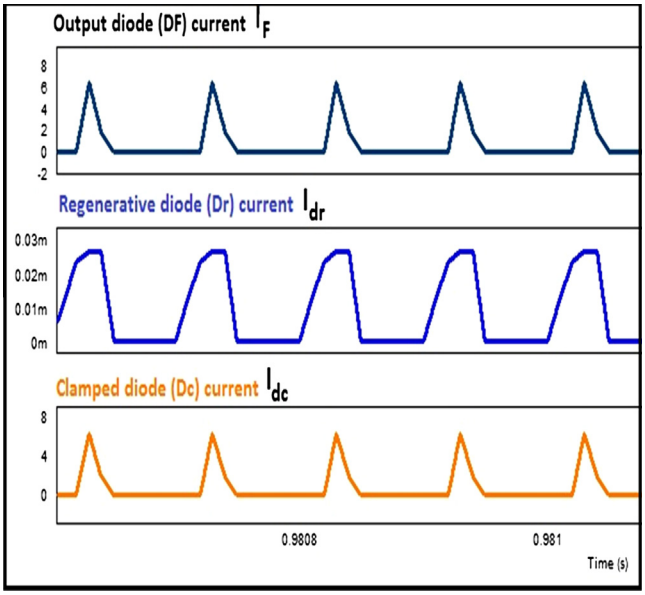

Figure 12 Diode currents during switching operations.

through the coupled inductor and the equation of minimum i_{lk} value is given by

$$\frac{V_o - [V_{Sc} + V_c](t_3 - t_4)}{NL_m} + I_{Lm}(t_3) \approx i_{Lm}(t) \tag{9}$$

Table 1 Simulated values.

S. No.	Parameters	Specification
1	DC voltage input	40 V
2	DC voltage output	403 V
3	Output power (max)	200 W
4	Switching Frequency	10 kHz
5	Output current	0.50 A
6	Output voltage ripple	0.3 V
7	Output current ripple	0.4 mA
8	Turns ratio (N)	1:2

Here $N = \frac{n2}{n1} \approx 1$

$$\frac{[L_p + L_m](t_3 - t_4)}{NL_p} i_{Lm(t_3)} \approx i_{Lk(t)} \tag{10}$$

The voltage equation from t_1 to t_4 is given by

$$V_o = (V_{cc} + V_{cs} + N) \times (V_{cc} - V_{LK(t_1 - t_4)} - V_{in}) \tag{11}$$

3.5. Mode V

Fig. 7 shown mode-V ($t_4 - t_5$) switch leakage inductor (L_k) current falls to zero, the magnetizing inductor is discharged linearly. Secondary inductor passes energy to the load through the converter hence I_s decreases. Small charge in magnetizing current is equal to i_{Lm} as given below.

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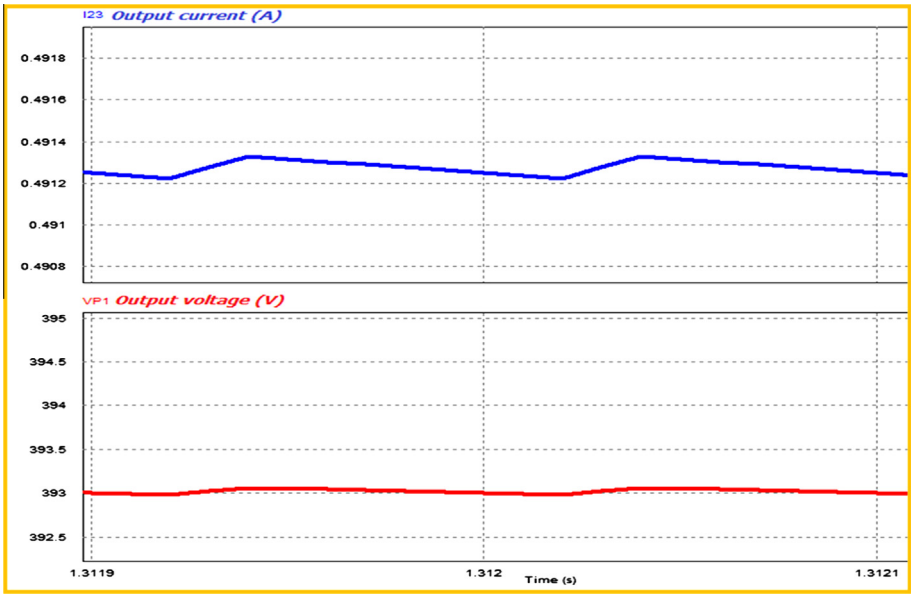

Figure 13 Measured output current and voltage when input = 37 V.

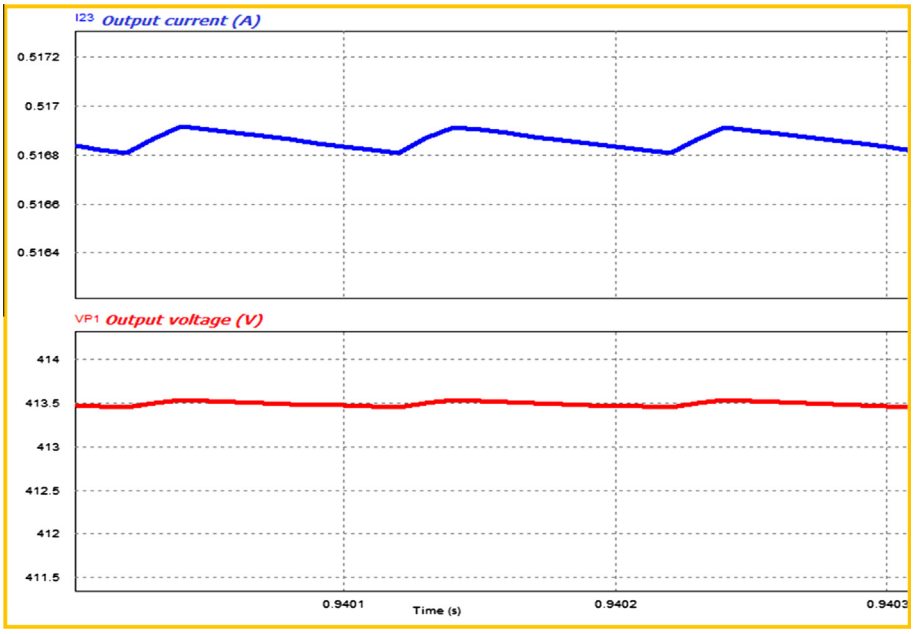

Figure 14 Measured output current and voltage when input = 41 V.

$$\frac{V_o - [V_{Sc} + V_c](t_4 - t_5)}{N_{Lm}} + I_{Lm(t_4)} \approx i_{Lm}(t) \tag{12}$$

3.6. Mode VI

In Fig. 8, the switch is turned ON ($t_5 - t_6$), the leakage inductance increases from zero, the switch is turned on by the ZCS condition V_{ce} completely zero, the leakage current is controlled by leakage inductor and the equations are given by

$$\frac{V_{in} + [V_o - V_{sc}(t_5) - V_c(t_5)]}{L_k}(t_5 - t_6) \simeq i_{LK(t)} \tag{13}$$

The leakage inductance and the voltage gain relationship are shown in Fig. 9 with switching frequency 10 kHz and with unity turns ratio. As the leakage inductance increases, the voltage gain of this converter decreases.

$$\frac{V_{in} + [V_o - V_{sc} - Vc]}{iLk} = Lk$$

4. Performance analysis

Analysis performed by considering clamped capacitor and switched capacitors are constant and current through the

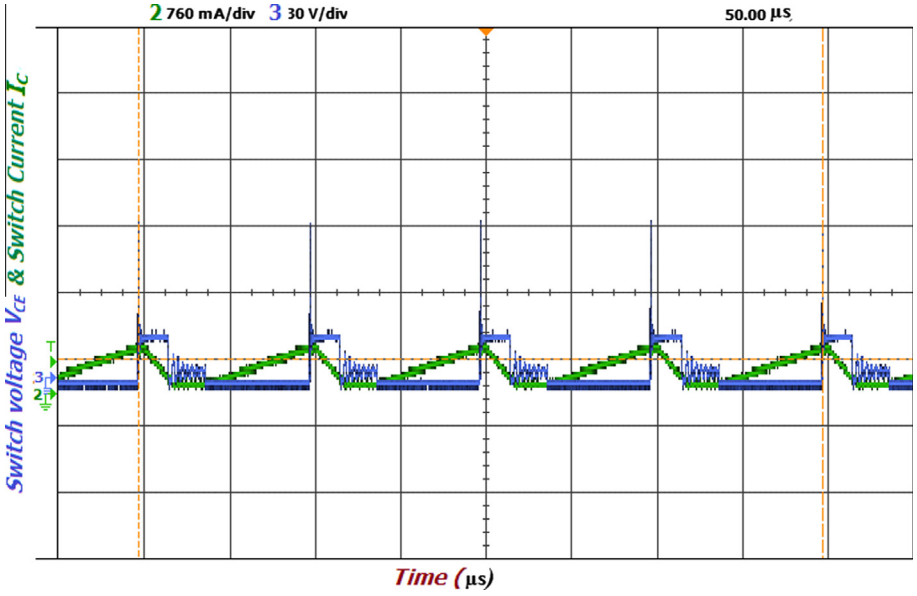

Figure 15 Switch voltage VCE and switch current (ZCS).

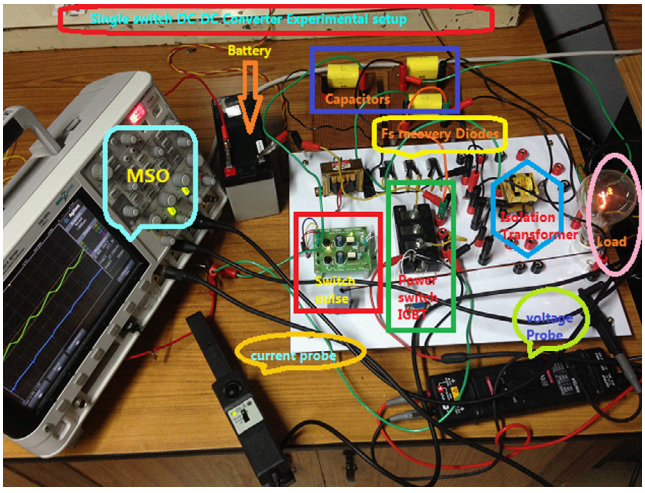

Figure 16 Hardware model: proposed DC-DC converter.

magnetizing inductor (L_m) also constant. When the switch is turned on, the L_m is charged by the input voltage is given by,

$$V_{lm} = V_{in} \tag{14}$$

Switched capacitor voltage (V_{sc}) can be given by

$$V_{sc} = N \times V_{in} \tag{15}$$

When switch is turned off the L_m is discharged and voltage is expressed by,

$$V_{Lm} = \frac{V_o}{N+1} - V_{in} \tag{16}$$

The voltage gain can be obtained from inductor volt-second balance principle

$$V_{GN} = \frac{V_o}{V_{in}} = \frac{N+1}{1-D} \tag{17}$$

$$V_o = \left(\frac{N+1}{1-D}\right) V_{in} \tag{18}$$

The voltage gain increases greatly when the turns ratio (N) increases. Extreme duty cycle can be designed to optimize the load regulation performance to the proposed isolated high boost DC-DC converter. $N = 0$ is the conventional converter. The voltage gain of the proposed converter is increased greatly by using a proper turns ratio design. The voltage stress of the switch and clamp diode can be written as,

$$V_{stress} = \frac{V_{in}}{1-D} \tag{19}$$

In the circuit design the turns ratio design plays an important role. By using this, the voltage stress (V_{stess}) of the switch is found out and duty ratio is obtained, it is given by

$$N = \left[\frac{(1-D) \times V_o}{V_{in}}\right] - 1 \tag{20}$$

The ratios of different turns are given in Fig. 10 which shows the relationship between the power device voltage stresses.

Both these capacitors are used as DC voltage source and the aim was to reduce the ripples in the capacitors. The relationship between the output power and voltage ripple is given by

$$C = \frac{P_o}{V_o \times \Delta V_c \times f_s} \tag{21}$$

$$P_o = V_o \times \Delta V_C \times C \times f_s \tag{22}$$

In the above equation, ΔV_c is voltage ripple on the capacitor C_c or C_s. ΔV_c it assumed as 2%.

The proposed dc-dc converter is defined as low loss converter. The efficiency of the converter is the ratio of the output power to the input power. The input power is the sum of the output power and the losses of the individual device.

$$P_{mos} = P_{sw(cond)} + P_{sw(off)} \tag{23}$$

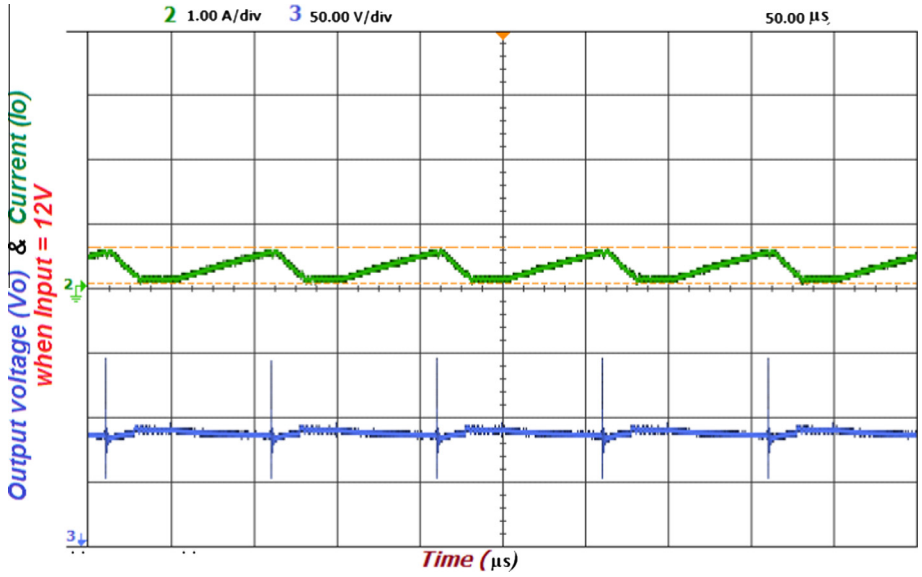

Figure 17 Measured output current and voltage when input = 12 V.

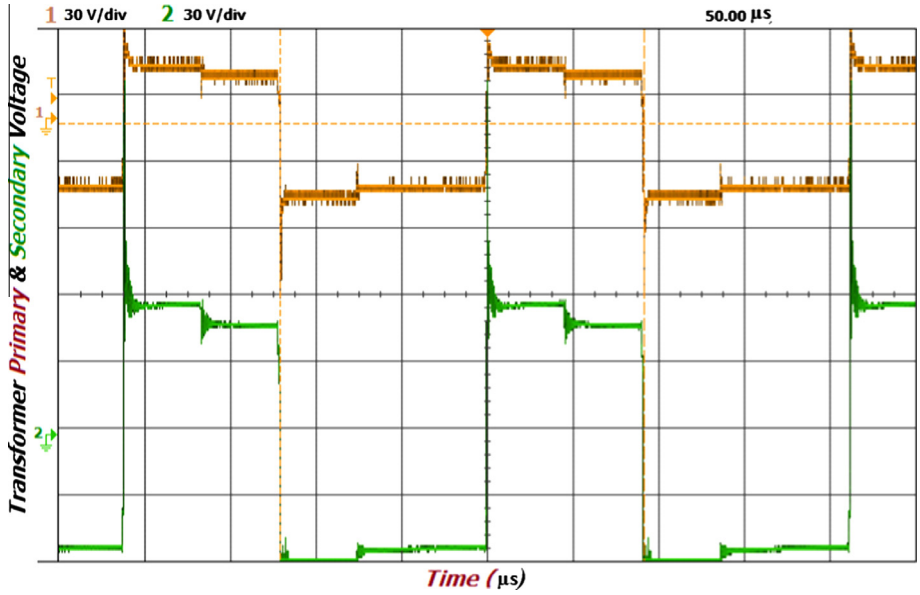

Figure 18 Switching transformer primary and secondary voltages.

$$P_i = P_o + P_{switch} + P_{diode} + P_{others} \quad (24)$$

Thus the efficiency expression is

$$\eta = \frac{P_o}{P_o + P_{switch} + Pdiode + P_{others}} \quad (25)$$

4.1. DC-DC converter design considerations

The main equations to design the proposed DC-DC converter are presented with an appropriate example, considering the following specifications.

Power output: 60 W.
Voltage input: 12 V.
Voltage output: 120 V.
Switching frequency: 10 kHz.
Turns Radio: $N = 2$.

4.1.1. Switch duty-cycle

The nominal duty-cycle is defined by

$$D = \frac{V_o - (N+1)V_{in}}{V_o} \quad (26)$$

4.1.2. Switch stress

The maximum voltage in the single power switch is equal to the

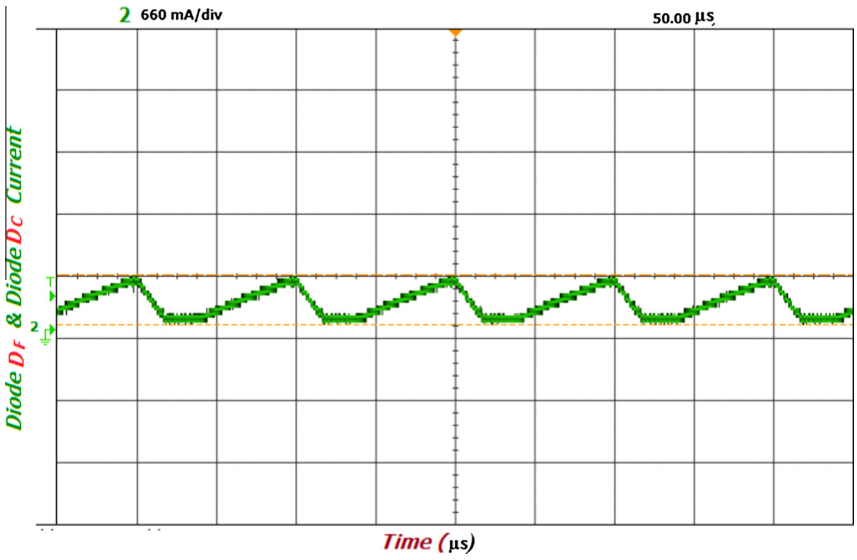

Figure 19 Diodes DF & Dc measured current.

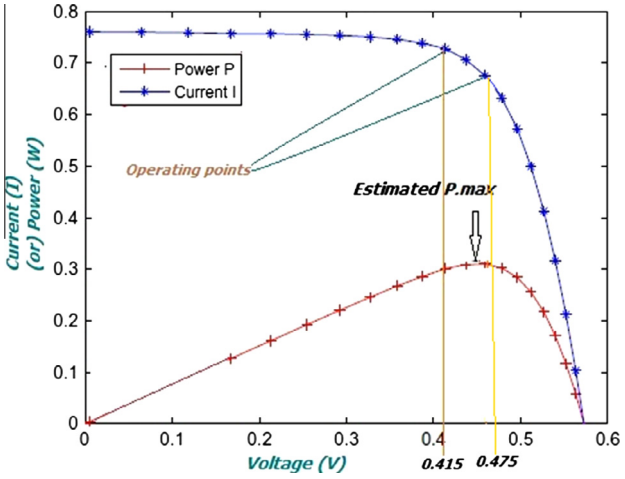

Figure 20 Solar cell *I-V* and *P-V* curve.

$$V_{stress} = \frac{V_{in}}{1-D} \tag{27}$$

Practically measured stress on the power Switch = 30 V as shown in the Fig. 15.

4.1.3. Switch loss

The RMS current can be determined approximately by Eq. (28), where the current ripple in the input inductance is not considered. The energy transference form of the capacitance does not change significantly the switch current waveform.

$$I_{switch(rms)} = \frac{P_{in}}{V_{in}} \times \sqrt{D} \tag{28}$$

The switch conduction loss is calculated by Eq. (29),

$$P_{sw(cond)} = I^2_{switch(rms)} \times R_{DSon} \tag{29}$$

The switch turn off loss is reduced in the proposed converter because the turn-on occurs with ZCS. The power loss of the turn-off switching is equal to the area of the switch voltage (V_{stress}) and switch current (I_{switch}). The transitions at the switching instant are multiplied by the switching frequency. Considering the single switch current equal to 5 A at the switching instant and turn-off time (t_{off}) equal to 50 ns, the turn-off power loss is calculated by

$$P_{sw(off)} = \left(\frac{1}{2} \times V_{stress} \times I_{switch} \times t_{off}\right) f \tag{30}$$

4.1.4. Diodes conduction loss

It is assumed that the average current in all diodes is equal to the output current in the proposed structure. The conduction losses of all diodes given are below by considering a conduction-threshold voltage equal to V_{TD} = 1.2 V

$$P_{diode} = 2 \times \frac{P_o}{V_o} \times V_{TD} \tag{31}$$

4.1.5. Calculated efficiency

The expected proposed converter efficiency can be determined by Eq. (25) based on the losses calculated. An example of the design procedure is given below.

Primary current I_p = 8 A rms.
Primary voltage V_p = 60 V rms.
Switching frequency = 10 kHz.
Turns ratio = N_p/N_s = 2.

Maximum and minimum temperatures T_m = 100 °C and T_a = 40 °C.
Transformer volt-ampere rating is given by
$S = Vp \times Ip$ = 480 *V-A*
Core material, shape, flux density, primary turns and secondary turns are given by
For high operating frequency suggests that a ferrite core be used. A double-E core is chosen for the core shape.
The performance factor curves for ferrite materials at 10 kHz given in the reference [18]. Let copper fill factor K_{cu} = 0.3, the maximum core flux density B = 0.17T, core area A_c = 1.5cm^2

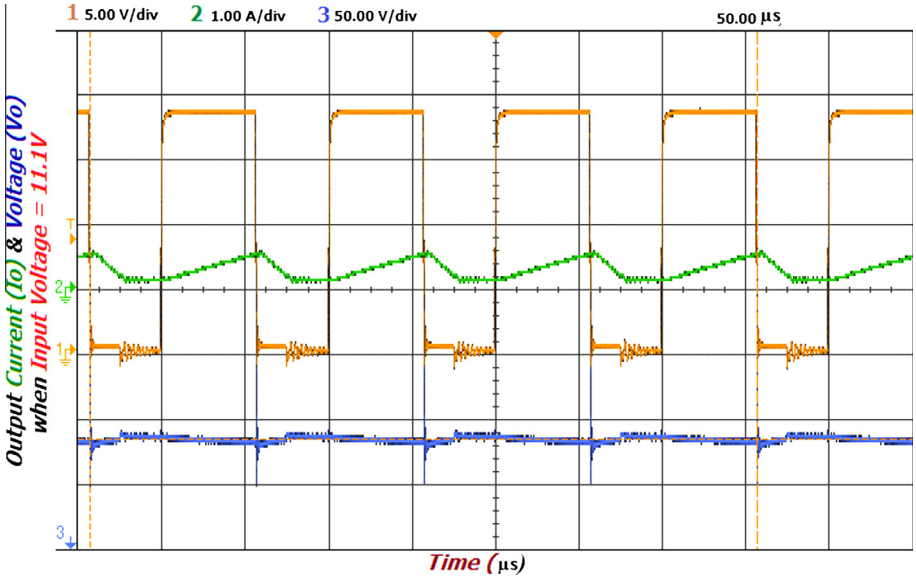

Figure 21 Measured output current and voltage when input = 11.1 V.

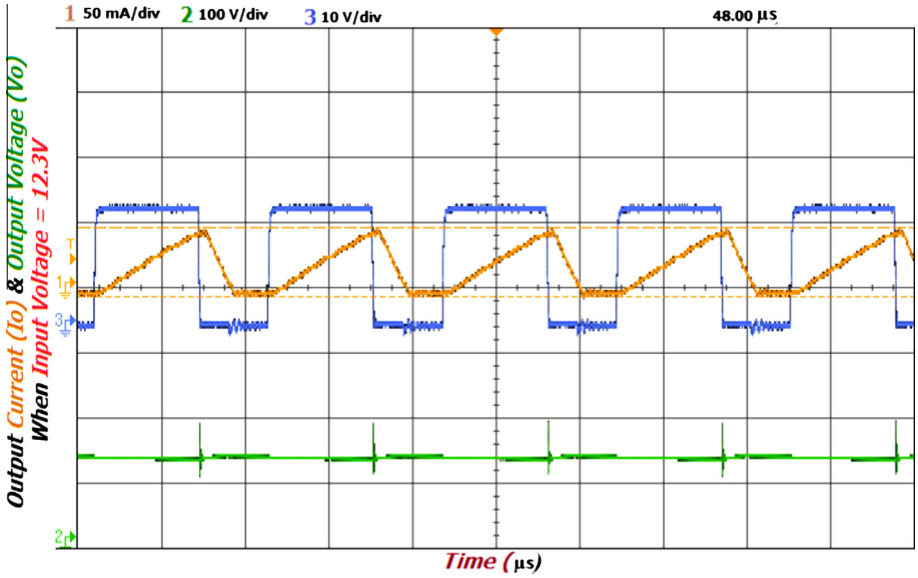

Figure 22 Measured output current and voltage when input = 12.3 V.

Table 2 Experimental values.

S. No.	Parameters	Specification
1	DC voltage input	12 V
2	DC voltage output	120 V
3	Output power (max)	60 W
4	Switching frequency	10 kHz
5	Output current	0.50 A
6	Output voltage ripple	2 V ± 5%
7	Output current ripple	0.4 mA

$$Np = \frac{\sqrt{2}Vp}{6.28fA_cB} = 53\,\text{turns}$$

$$N_s = \frac{N_p}{n} = 27\,\text{turns}$$

5. Results

5.1. Simulation results

The proposed high boost DC-DC converter is simulated using PSIM software and output voltage and output gain are described before implementing. The switching frequency, input voltage 10 kHz, 40V_{dc} are respectively used for simulation. Step-up output voltage obtains 403V_{dc}. The voltage gain K_o equals to 10. This is matched with the theoretical value given in Eq. (17). Full load rating 200 W is used in the simulation. At rated input voltage, the gate pulse (S), output voltage (V_o), output current (I_o) and controlled switch collector to emitter voltage (V_{CE}) and collector current (I_C) are shown in the Fig. 11. The output currents I_F, I_{dr}, I_{dc} of power diodes

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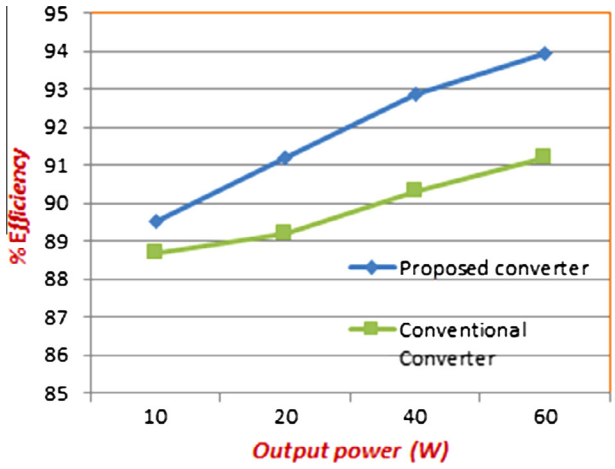

Figure 23 % Efficiency vs output power (watts).

Table 3 Performance comparison.

Topology	Conventional converter	Proposed converter
No. of active switch	1	1
No. of diodes	1	3
Voltage gain	$1/(1-D)$	$(N+1)/(1-D)$
Reverse recovery problem	Serious	Small
Soft switching performance	Hard switching	ZCS
Conduction losses	Large	Medium
Switching losses	High	Low
Voltage stress on power switch	V_o	$V_{in}/(1-D)$

Table 4 Hardware and Simulation parameters.

Parameters	Specifications simulation	Specifications hardware
Input voltage	40 V	12 V
Output voltage	400 V	120 V
IGBT	Ideal	CM100DU12H
Diode	Ideal	BY329X
Capacitors	$C_s = C_c = 6.25$ uF $C_o = 180$ uF	$C_s = C_c = 20$ uF $C_o = 50$ uF
Isolation transformer	Turns ratio = 1:2 $L_m = 96.8$ uH	Turns ratio = 1: 2 $L_m = 19.4$ uH
Load	200 W	60 W
Driver IC		FOD3180

D_F, D_r, and D_c are shown in Fig. 12. The output voltage is lifted up to 403 V. Hence, it is realized with the theoretical output voltage (V_o) given in the Eq. (18). Table 1 provides the simulated parameters and their specifications.

Fig. 13 and 14 are output voltage and current measurements for the different input DC voltages at 37 V and 41 V respectively.

5.1.1. Soft switching

Fig. 11 shows the voltage between collector to emitter of the IGBT power switch and current through the switch reaches zero before the gate pulse (S) is applied to controlled switch. Then the voltage starts increasing trough the switch. This ensures ZCS of the switch which is depicted in the arrow point in the Fig. 11. ZCS does not affect the switching loss that arises from the power switch output capacitance and it may not influence the loss induced by diode reverse recovery, hence ZCS is of no help in the improvement of converter efficiency. The practically measured switch stress (V_{CE}) and current (I_C) are shown in Fig. 15. The measured maximum switch voltage equals to 30 V. The main switch voltage is clamped to that of the clamp capacitor by the clamp diode, when the switch is turned off. From the waveforms, it can be seen that ZCS turn on condition is achieved for the active switch, which reduces the switching losses.

5.2. Experimental results

A 60 W prototype of the proposed converter is built to verify the theory. The hardware prototype model is shown in Fig. 16.

The hardware prototype is validated with simulated design. The proposed model 60 W with 12 V DC input and 120 V DC output. The measured full load output voltage $120V_{dc}$ and full load current 0.5 A are shown in Fig. 17. The experimental results of the isolated transformer primary and secondary winding measured voltage are shown in Fig. 18.

The voltage on the clamp diode D_c, the voltage on the freewheeling diode D_F are illustrated in Fig. 19. Both the values are equal at the measured interval. The input to the prototype model is given $12V_{dc}$ from the available DC source and the controlled switch is controlled through the DSP 28335 controller.

The fixed DC source validated to renewable source by considering single solar cell measurement. As per the parameter given in the reference [17] the I-V and P-V curves are plotted as shown in the Fig. 20. For study 57 mm diameter silicon solar cell under 1 Sun (1000 W/m^2) at 33 °C the voltage and current are measured. From this available experimental data MPP is roughly estimated.

The solar cell open circuit, short circuit and maximum power point data are $V_{oc} = 0.5727$ V, $I_{sc} = 0.7605$A, $I_{mp} = 0.6755$A and $V_{mp} = 0.4590$ V. MPP pointed between two steady operating points. These operating points the voltages are 0.415 V and 0.475 V. These values are per solar cell. For the practical case from the 12 V DC source the load operating points are validated with different input voltages. These voltages are based on percentage variation in the single solar cell. The calculated variable voltage ranges are 11.1 V, 12 V and 12.3 V. IGBT is used, because prototype model is constructed for low switching frequency. The output waveform is observed by using Mixed Signal Oscilloscope and measured. The measured input and output voltage waveform are shown Figs. 21 and 22.

Figs. 21 and 22 are output voltage and current measurements for the different input DC voltages at 11.1 V and 12.3 V respectively.

The control signal is generated from the programmed DSP controller. Depending on the desired output voltage, the controller generates control signals. The experimental results show that the output voltage can be boosted upto the voltage gain 10 when it turns ratio (N) equal to 1:2. Thus, the proposed boost converter can be interfaced to the inverter grid at the user end. The experimental results are tabulated in Table 2.

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The efficiency of the hardware model system is calculated at 4 different loads. By using the measured output power the efficiency of the proposed DC-DC converter curve plotted is shown in Fig. 23. The theoretical efficiency equation is given in Eq. (25). The practical calculated efficiency of the proposed model at full load is 94%.

Due to the limitations in the power hardware setup, the prototype was intended only to verify the operational concept.

5.3. Performance comparison

The performance comparison between the conventional boost converter and the proposed converter are shown in the Table 3. The proposed converter has two more diodes compared with conventional boost converter, an additional capacitor. The proposed converter conventional ratio is higher than that of the conventional boost converter with the same duty-cycle. Hence, the conventional converter hard switching causes the ringing in the output voltage waveform which affects the performance of the converter. Based on the performance, the hardware model efficiency and the conventional converter efficiency plotted, which shown in Fig. 23. It shows the efficiency lying below the proposed converter efficiency curve.

The values and specifications of the proposed converter simulation and hardware model comparisons is given in the Table 4 for complete reference.

The Figs. 13 and 14 are simulation voltage and current values of different voltage input values. This can be compared with reduced scale (3.33%) hardware prototype model voltage current reading measured as shown in the Figs. 21 and 22. The percentage variation (7.5% reduction and 2.5% rise, an explanation given in the Section 5.2.) in the voltages are similar in the both cases.

6. Conclusion

This isolated high boost converter with switched capacitor and magnetizing inductors is used to get the high voltage gain. The transformer isolation can be accomplished and it provides better significant influence on efficiency of whole energy condition system. An application of fast recovery diodes eliminates the reverse recovery problems. Thus allows quick diode turn-off without significant power losses. The leakage inductor of the clamp circuit achieves ZCS condition. High boost voltage operation can reduce stress on active switch. The passive lossless clamp circuit helps to recover the leakage energy of the diode and clamped capacitor to get high efficiency at high power value. All these features improve the circuit efficiency effectively. Complete analysis of the operations and the performances of the proposed converter are presented in this paper. A prototype of the converter was built and tested for validation of operation and performance of the proposed converter.

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