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Abstract: This paper presents the impact of parameter fluctuation due to process variation on radio frequency (RF) stability performance of double gate tunnel FET (DG TFET). The influence of parameter fluctuation due to process variation leads to DG TFET performance degradation. The RF figures of merit (FoM) such as cut-off frequency (f_t), maximum oscillation frequency (f_{max}) along with stability factor for different silicon body thickness, gate oxide thickness and gate contact alignment are obtained from extracted device parameters through numerical simulation. The impact of parameter fluctuation of silicon body thickness, gate oxide thickness and gate contact alignment was found significant and the result provides design guidelines of DG TFET for RF applications.

Key words: DG tunnel FET; radio frequency; stability factor; numerical simulation
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1. Introduction

In recent years, tunnel FETs have received much attention because of their lower I_{off}, and lower subthreshold slope as compared to conventional MOSFET hence they can be used for mobile electronic applications which require low-standby-power (LSTP) operation active devices as reported by ITRS[1]. Tunnel FETs act as field effect transistors but use band-to-band tunneling. When the device turns on, the carriers tunnel through the barrier so that current can flow from source to drain. When the device is off, the presence of the barrier keeps the off-current extremely low, hence leakage current reduces drastically. High-k gate dielectric increases I_{on} of tunnel FET and is also added with the bottom gate to double the current[2]. Many works were carried out on the fabrication and dc characteristics of tunnel FET[3−5]. Recently, DG TFET received attention for analog and RF applications[6, 7]. RF stability is one of the decisive parameters in amplifier design which needs greater attention. RF stability performance of DG MOSFET, FinFET and SNWT have been studied[8−10]. The small signal modeling and RF stability performance of double gate tunnel FET has been reported[11]. The impact of parameter fluctuation such as gate oxide thickness, gate contact alignment and silicon body thickness on DC characteristics of DG TFET were found significant[12, 13]. It is important for device engineers to adopt careful design procedures to avoid the impact of process variations on device performance. In this paper, for the first time the impact of parameter fluctuation due to process variation on RF stability performance of DG TFET is investigated.

2. Device structure and simulation

Figure 1 shows the schematic of DG TFET of physical channel length (L_{ch}) of 50 nm[2], silicon body thickness (t_{si}) of 10 nm and gate oxide thickness (t_{ox}) of 3 nm[2]. The device has a p^+ source region, an intrinsic p-type channel region, and n^+ drain region with uniform doping concentration of 1×10^{20}, 1×10^{17} and 5×10^{18} cm^{-3} respectively. The source-to-intrinsic and intrinsic-to-drain junctions are considered to be abrupt. We have used the non-local band-to-band tunneling (BBT) model to analyze the performance of DG TFET and this model is already validated for this device[2]. In order to model the interface trap along with the presence of high impurity atom in the channel and to model the concentration, parallel and perpendicular dependent Shockley–Read–Hall recombination model and CVT model are used in numerical simulation[14].

The DG TFET channel length considered for this work is 50 nm, hence inclusion of quantum effects is essential to analyze the electrical behavior of this device. We have used quantum simulation and set quantum tunneling mesh in 2D device simulator Silvaco Atlas using QTX.MESH and QTY.MESH keyword in the tunneling region to accurately calculate the charge across the tunneling region. In order to model the tunneling behavior of DG TFET, in the model statement we have set QTUNN.DIR = 1 which implies that tunneling occurs in a lateral direction between source and drain. The work function of gate electrode is chosen as 4.17 eV and gate leakages are ignored in simulations. The threshold voltage (V_t) and sub threshold slope for the DG TFET are obtained from DC characteristics shown in Figure 2 and found to be 0.65 V and

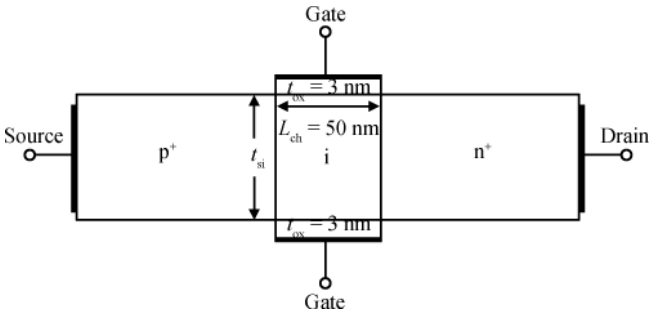

Figure 1. Schematic structure of DG TFET.

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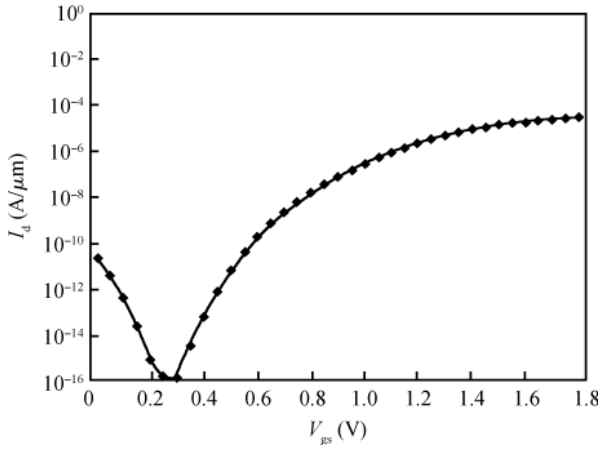

Figure 2. I_d–V_g characteristics of DG tunnel FET.

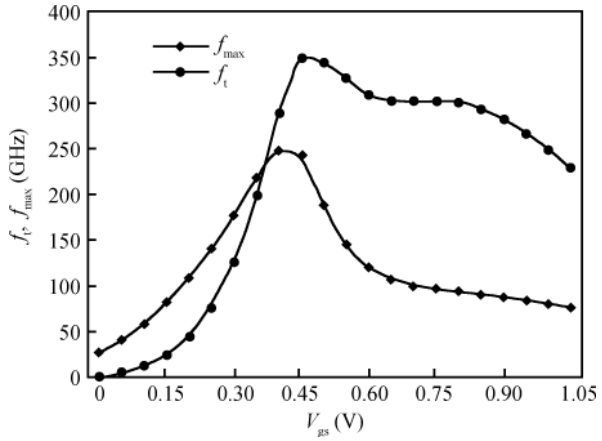

Figure 3. Extracted f_t and f_{max} as a function of V_{gs} for $V_{ds} = 1$ V.

38 mV/decade respectively. The small signal AC analysis is performed to obtain intrinsic and extrinsic parameters of DG TFET. The f_{max}, f_t and stability factor are extracted using device simulation.

3. Radio frequency stability performance of DG TFET

The cut-off frequency f_t is evaluated as the frequency for which magnitude of short circuit gain drops to unity. The f_t is expressed as

$$f_t = \frac{g_m}{2\pi C_{gg}}, \tag{1}$$

where g_m is transconductance and C_{gg} is total gate capacitance.

The f_{max} is related to the capability of the device to provide power gain at large frequencies, and is defined as the frequency at which the magnitude of the maximum available power gain drops to unity. The f_{max} is expressed as

$$f_{max} = \frac{f_t}{\sqrt{4(R_s + R_g + R_i)(g_{ds} + 2\pi f_t C_{gd})}}, \tag{2}$$

where g_{ds} is drain-to-source conductance and R_g, R_s and R_i is gate, source and channel resistances respectively.

Figure 3 shows extracted f_t and f_{max} as a function of gate voltage. The value of f_t decreases as the total gate capacitance increases and this is more significant in short channel DG TFET. The f_t is extracted when current gain is unity $|Y_{21}/Y_{11}| = 1$ and it is found to be 350 GHz. Similarly f_{max} is calculated when maximum available power gain drops to unity and found to be 250 GHz.

From Equation (1), it is observed that f_t increases as transconductance increases and for DG TFET, f_t is higher because of higher transconductance. This shows the capability of DG TFET operating at higher frequency. f_{max} is lower for short channel DG TFET as g_{ds} and R_g increases.

The stability factor is calculated using Y-parameters at different frequency of operation for the DG TFET. The stability factor (K), gives an indication whether a device is conditionally/unconditionally stable. DG TFET is unconditionally stable at any operating frequency above a critical frequency (f_k). Unconditionally stable means that the transistor will not begin to oscillate independently from the value of the signal source and load impedances or from any additional passive termination networks at the transistor's input (gate) and output (drain)[15]. At operating frequency below f_k however, the transistor is conditionally stable and certain termination conditions can cause oscillation. It must satisfy the condition $K > 1$ for a device to be unconditionally stable[16].

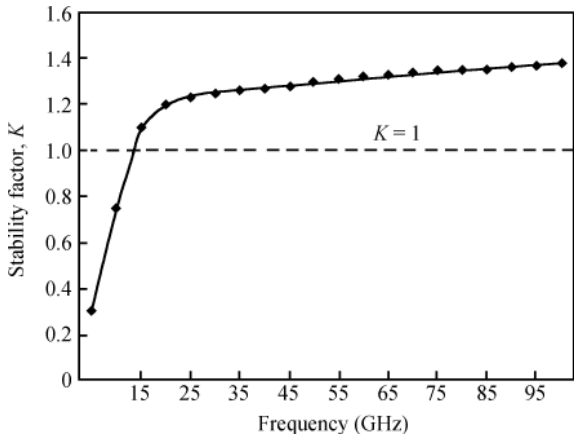

Figure 4. Extracted stability factor as a function of frequency.

The stability factor in terms of Y-parameter can be expressed as[17]

$$K = \frac{2\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12} - Y_{21})}{|Y_{12} - Y_{21}|}. \tag{3}$$

Figure 4 depicts the extracted stability factor for the structure shown in Figure 1 over the frequency range of 100 GHz and it is found that $K > 1$ from 11 GHz onwards. This infers that the device is unconditionally stable from 11 GHz. When the device is unconditionally stable over the wide frequency range, it indicates that additional stabilization circuits are not required for radio frequency integrated circuit (RFIC) which can reduce the circuit design complexity.

4. Impact of parameter fluctuation on RF stability performance

In the following sections, the variations of silicon body thickness, gate oxide thickness, gate contact alignment and

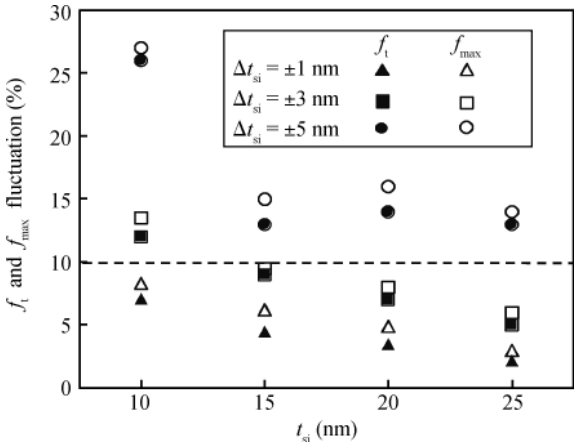

Figure 5. Impact of silicon body thickness variation on f_t and f_{max}.

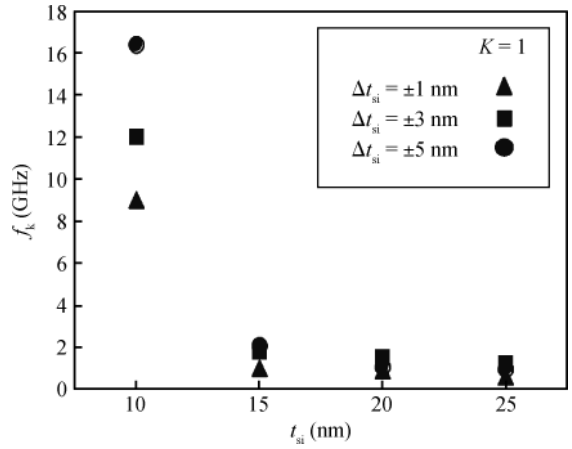

Figure 6. Impact of silicon body thickness variation on f_k.

gate length are studied with respect to RF stability performance of DG TFET.

4.1. Silicon body thickness

The silicon body thickness (t_{si}) becomes important when devices are fabricated on thin substrates to achieve better gate control and to reduce capacitive effects. Figure 5 shows the fluctuation of f_t and f_{max} for variation in t_{si} of DG-TFET. The silicon thickness variation (Δt_{si}) is considered as ±1, ±3, and ±5 nm for thickness from 10 to 25 nm. The impact of Δt_{si} at ±1 and ±3 nm is around 10% of f_t and f_{max} fluctuation ($\Delta f_t/f_t$ and $\Delta f_{max}/f_{max}$). The f_t and f_{max} fluctuation increases as Δt_{si} reaches ±3 nm which is predominant for smaller t_{si}. At silicon body thickness of 20 nm and above, the f_t and f_{max} fluctuation is less as compared to smaller t_{si}, however to take advantage of the double gate it is suggested to keep t_{si} as 15 nm and restricting Δt_{si} within ±3 nm for better RF performance.

The critical frequency (f_k) for various silicon body thicknesses is shown in Figure 6. It is evident that for silicon thickness of 10 nm the f_k fluctuated for Δt_{si} of ±1, ±3, and ±5 nm. The impact of Δt_{si} is less for large silicon thicknesses. However, ultra-thin body reduces bulk capacitive effects. Hence to achieve stability of DG TFET at smaller frequency, it is suggested to have t_{si} around 15 nm and to keep Δt_{si} within ±3 nm.

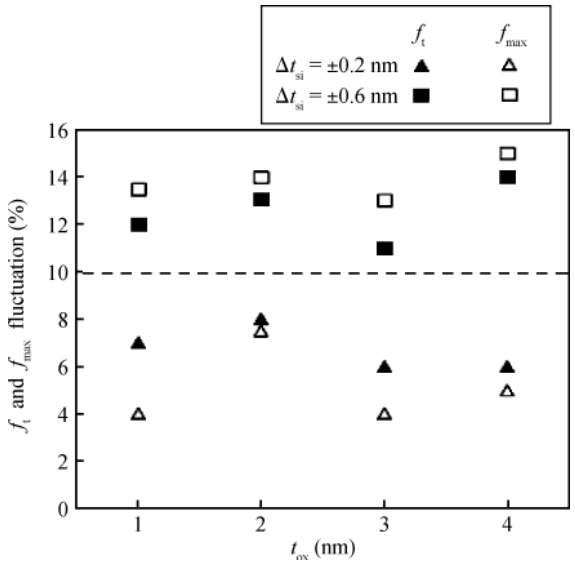

Figure 7. Impact of gate oxide thickness variation on f_t and f_{max}.

4.2. Gate oxide thickness

In short channel devices, the impact of gate oxide thickness on device performance cannot be ignored. The gate oxide provides capacitive coupling between gate and channel which control the drain current of DG TFET. The gate oxide thickness variation (Δt_{ox}) can cause fluctuation in DG TFET DC characteristics[13]. Figure 7 shows the impact of gate oxide thickness variation on f_t and f_{max}. The f_t and f_{max} fluctuations are less than 10% for Δt_{ox} of ±0.2 nm, however, as Δt_{ox} increases to ±0.6 nm, the fluctuation is higher because gate capacitance varies with different oxide thickness. The RF performance of DG TFET will not be affected if Δt_{ox} is within ±0.2 nm. Hence, it is suggested to control the process variation by better oxidation process and to keep Δt_{ox} less than ±0.2 nm.

Figure 8 shows the critical frequency for different oxide thicknesses (t_{ox}). The f_k fluctuation for smaller oxide (at t_{ox} = 1 nm) thickness is less compared to larger oxide (at t_{ox} = 4 nm) thickness for Δt_{ox} of ±0.2 nm and ±0.6 nm. When t_{ox} is 1 nm the DG TFET is unconditionally stable at critical frequency of 0.5 GHz, this shows the thinner gate dielectric is preferable to operate DG TFET for better stability under RF range.

4.3. Gate contact alignment

In DG TFET, controlling the source-intrinsic region leads to an increase in device speed and reduced fringing field, this can be achieved through gate contact alignment (L_{gca}). Figure 1 shows self-aligned gate structure, the top and bottom gate of DG TFET can be underlapped or overlapped on the source-intrinsic region to improve RF performance. Figure 9(a) shows overlap gate structure, and Figure 9(b) shows underlap gate structure.

Figure 10 shows the impact of gate contact alignment variation (ΔL_{gca}) on f_t and f_{max} for underlap (negative alignment values) and overlap (positive alignment values) structures. For

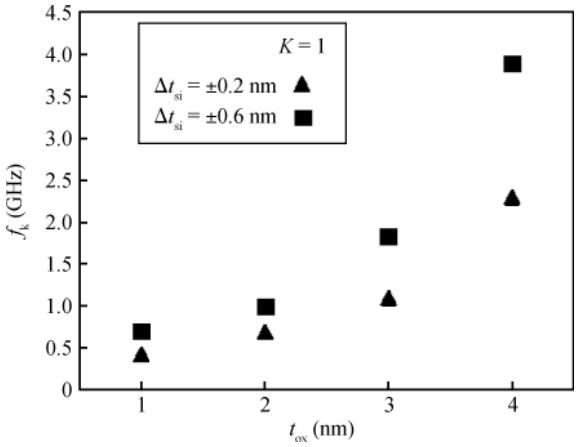

Figure 8. Impact of gate oxide thickness variation on f_k.

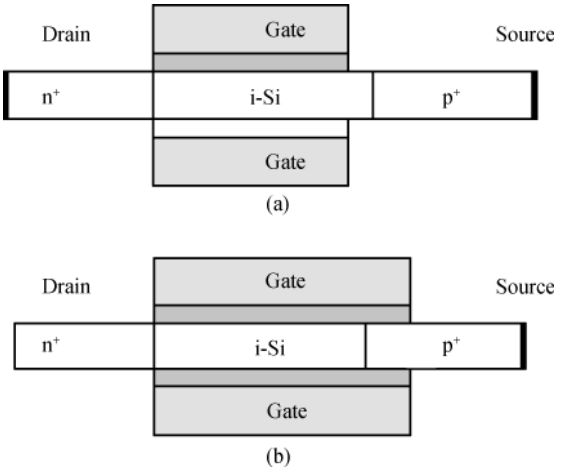

Figure 9. (a) Overlap and (b) underlap gate contact alignment.

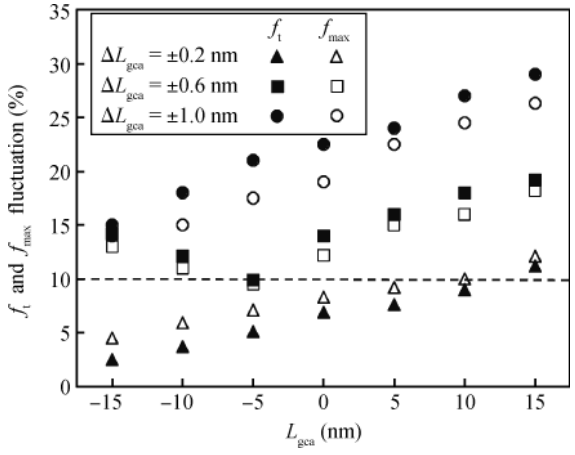

Figure 10. Impact of gate contact alignment variation on f_t and f_{max}.

ΔL_{gca} of ± 0.6 nm, the f_t and f_{max} fluctuation crosses 10% and fluctuation is more for both underlap and overlap structures as ΔL_{gca} increases. It is recommended to keep the L_{gca} as $+5$ nm of channel length and ΔL_{gca} less than ± 0.2 nm to obtain better RF performance of DG TFET.

The critical frequency is plotted for various L_{gca}, and shown in Figure 11. It is found that the K value reaches 1

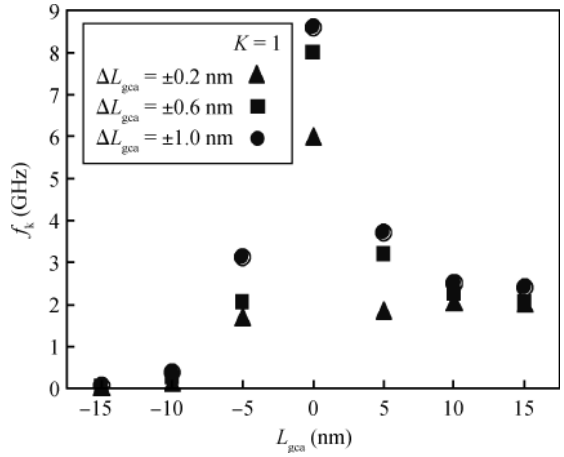

Figure 11. Impact of gate contact alignment variation on f_k.

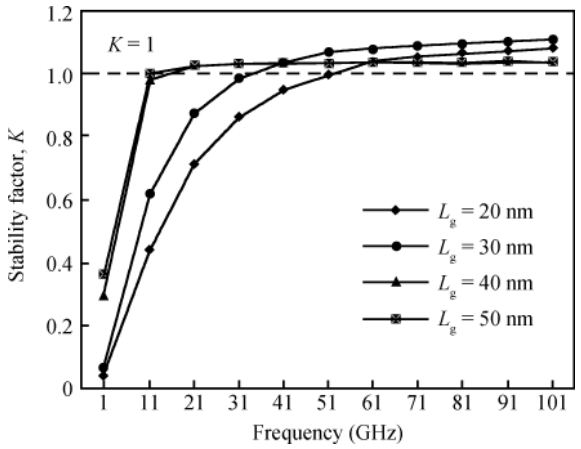

Figure 12. Stability factor as a function of frequency for different channel length.

at lower frequencies for gate underlap structure as compared to gate overlap. The gate contact alignment at -10 nm and -15 nm shows good stability performance. But these alignments cannot provide good DC characteristics[12, 13] and also fabricating the device with negative gate contact alignment is difficult. Therefore we suggest that the optimal position for gate contact alignment should be $+5$ nm for gate overlap for better stability performance.

4.4. Gate length

Figure 12 shows stability factor for various channel length. The curves show an increase in f_k as L_g increases. It is evident that as the channel length scaled, gate capacitance decreases thereby f_t increases. However, as f_t increases f_k will increase[9]. Hence at smaller channel length the stability is reached at higher f_k than at larger channel length.

5. Conclusion

The RF stability performance of DG TFET is presented using numerical simulation. The intrinsic and extrinsic parameters are extracted through ac analysis. The results shows

good RF stability performance at 50 nm channel length but the impact of process variation is also found obvious on RF stability performance at this length. From the result we can observe that variation within ± 3 nm on silicon body thickness, ± 0.3 nm on oxide thickness and for gate contact alignment of $+5$ nm shows good RF stability performance.

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