IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 13, 2017, accepted November 13, 2017, date of publication December 11, 2017,
date of current version February 14, 2018.

Digital Object Identifier 10.1109/ACCESS.2017.2775203

Implementation and Comparison of Symmetric and Asymmetric Multilevel Inverters for Dynamic Loads

C. DHANAMJAYULU AND S. MEIKANDASIVAM
School of Electrical Engineering, Vellore Institute of Technology, Vellore 632014, India
Corresponding author: C. Dhanamjayulu (dhanush403@gmail.com)

ABSTRACT This paper implements and compares a symmetric hybridized cascaded multilevel inverter and an asymmetric multilevel inverter utilizing a switched capacitor unit for 17 level inverters. The symmetric hybridized multilevel inverter topology consists of a modified H-bridge inverter, which results in an increase in the output voltage to five level from the three level by using a bi-directional switch at the midpoint of a dual-input dc source. In the proposed asymmetric multilevel inverter, dc sources are replaced with the switched capacitor unit, which in turn boosts the output voltage and produces twice the voltage levels at the loads. The proposed topology with the staircase modulation technique has been verified using MATLAB–SIMULINK, and the results are experimentally executed with prototype models, which are interfaced with dSPACE RTI 1104. The results of the proposed topologies are experimentally obtained for steady state, and the performance of the same is tested under different resistive and inductive load disturbance conditions. The results substantiate that these multilevel inverter topologies are better stabilized during load disturbance conditions with low total harmonic distortion, a lesser number of switches, and increased output voltage levels, and these topologies well suit for renewable energy applications.

INDEX TERMS Multilevel inverter (MLI), staircase pulse width modulation technique (SPWM), switched capacitor unit (SCU), total harmonic distortion (THD), high output voltage levels.

I. INTRODUCTION

The multilevel inverters have been developed and utilized for higher voltage levels [1]. In achieving higher voltage levels and power levels, cascaded multilevel inverters (MLI) are proven to be more flexible than conventional topologies. Its modularity property can be used to increase the power output of the inverter. Cascaded MLIs are constructed by linking in series output terminals of several H-bridge inverters [2], [3]. It is hence evident that this configuration supports high power levels with the use of low voltage rating components in inverters. In case of a fault in any one of the inverter cells, it can be easily and quickly replaced because of its modularity property. In order to maintain reliability in inverter output in the event of a fault in any inverter cell [4], a suitable control strategy can be used to bypass the faulty cell without disturbing the load [5], [6]. With advancements in multilevel inverters, the need for the design of new modulation methods for the same is increasing. As a result, many modulation schemes have been introduced. Based on converter topology and its domain of application, each modulation technique has its own advantages and disadvantages. The classification of modulation strategies for multilevel inverters has been proposed in [7] based on the difference in high or low-frequency switching. High power applications utilize a frequency up to 1 kHz. The PWM switching is also suitable for Hybrid cascaded MLI [8]. This facilitates charging and discharging time for storage elements used in multilevel inverters. PWM methods based on the carrier are classified into level shifted and phase shifted modulation schemes. Level shift modulation techniques are mostly employed in various applications to generate high-quality output waveforms. In such techniques, carriers which can be used are triangular, saw-tooth and constant DC magnitude waveforms. The reference waveforms which can be used in PWM schemes are sinusoidal, sinusoidal injected with third harmonic and trapezoidal voltage waveforms. Currently, selective harmonics elimination which is also known as fundamental frequency switching has gained attention among researchers, [9]–[15]. The cascaded MLI can be operated in both symmetric and asymmetric configuration. In the

symmetric configuration, the magnitude of input DC sources is equal, due to which a number of output levels are less in addition to utilizing more number of switches with increased total harmonic distortion (THD). In contrast, asymmetric MLI input DC sources are unequal due to which different voltage levels can be generated. By combining such voltage levels more levels can be generated with a lesser number of switches with a consequent reduction in THD [16]–[19].

In this research, two different 17 level symmetric and asymmetric multilevel inverters topologies are proposed, in the symmetric configuration, a new single phase hybridised cascaded multilevel inverter is proposed with stair-case modulation technique while the asymmetric multilevel inverter configuration is developed with switched capacitor unit. In addition, the comparison analysis between the inverter topologies are also taken up for detailed study.

II. PROPOSED SYMMETRIC HYBRIDESED CASCADED MLI TOPOLOGY

The hybridised H-bridge circuit topology utilized as a part of the development and implementation of the 17-level symmetric inverter is, as shown in Figure.1. The operation of appropriate topology can be interpreted in terms of two-stages. In the first stage, the output levels $+$V1, 0, $-$V1 is delivered by the association of bidirectional switch to the second leg on H-bridge while in the second stage, the output levels $+2$V1, 0, -2V1 are generated. The generated five-level output voltage using symmetric basic hybridised cascaded MLI topology is depicted in Figure.2. The switching states representing the status of the basic MLI are given in Table 1.

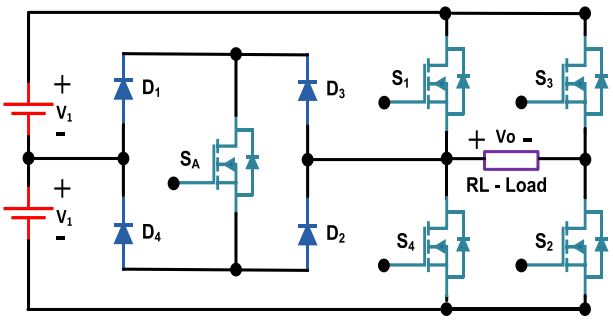

FIGURE 1. Basic Hybridised H-bridge topology.

TABLE 1. State table of proposed basic hybridised MLI.

Output voltage levels	Switching States				
Switches	S_1	S_2	S_3	S_4	S_A
+2 V	1	1	0	0	0
+1 V	0	1	0	0	1
0 V	0	1	0	1	0
0 V	1	0	1	0	0
-1 V	0	0	1	0	1
-2 V	0	0	1	1	0

A. CALCULATION OF CIRCUIT PARAMETERS

The following section discusses the choice of the number of sources, switches, and output voltage levels. In the symmetric

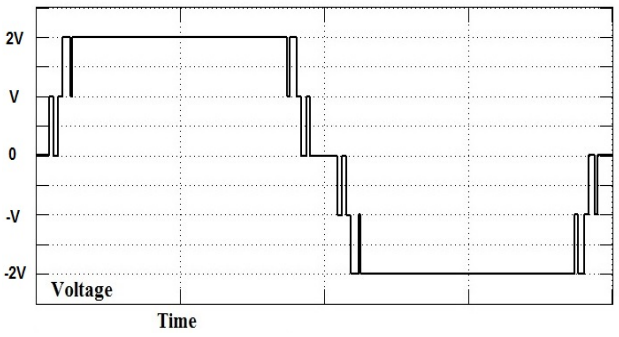

FIGURE 2. Five level output voltage waveform.

hybridised and asymmetric multilevel inverters, the values of the dc sources are unequal so that number of output levels can be generated using a number of switches. It is assumed that the kth cell and pk are the same DC sources.

In the proposed symmetric hybridised multilevel inverter the input DC sources are equal and the inverter equations can be written as follows

$$V_{d1} = V_{d2} = \cdots\cdots = V_{dk} = V_d \tag{1}$$

The number of levels that can be determined is as follows where m is the no cell and n is the number of dc sources in each cell

$$N_{Levels} = 2mn + 1 \tag{2}$$

The switches can be estimated as

$$N_{switch,k} = 2p_k + 1 \tag{3}$$

The maximum output voltage can be estimated as

$$V_o = mnV_d \tag{4}$$

For the proposed asymmetric multilevel inverter the input DC sources are unequal and the equation can be written as

$$V_{d1} = V_1 = V_d \tag{5}$$

Then, the k_{th} cell dc voltage source magnitude is given by

$$\begin{aligned} V_{dk} &= (2p_1 + 1).(2p_2 + 1) \cdots (2p_{k-1} + 1).V_d \\ &= V_d . \prod_{j=1}^{k-1} (2p_j + 1) \end{aligned} \tag{6}$$

Where k_{th} is the number of cells and p_k is the number dc voltage sources in the k^{th} cell.

The number of output voltage levels can be estimated as

$$\begin{aligned} N_{Levels} &= (2p_1 + 1).(2p_2 + 1) \cdots (2p_m + 1) \\ &= \coprod_{j=1}^{m} (2p_j + 1) \end{aligned} \tag{7}$$

The maximum output voltage estimated is as follows

$$V_o = \frac{[(2p_1+1).(2p_2+1)\cdots(2p_m+1)]-1}{2}.V_d$$
$$= \frac{\left[\prod_{j=1}^{m}(2p_j+1)\right]-1}{2}.V_d \quad (8)$$

The number of switches estimated is

$$N_{switch,k} = 2(p_k+1)$$
$$= \sum_{j=1}^{m} 2(p_j+1) \quad (9)$$

By using the aforesaid equations the number of switches, the number of voltage levels and the output voltage of proposed topologies can be determined.

TABLE 2. Switching state table of 17-level symmetric MLI.

V_O	1	2	3	4	5	6	7	8	0		-1	-2	-3	-4	-5	-6	-7	-8
S_1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_3	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_4	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S_5	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_6	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S_9	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{11}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S_{13}	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
S_{14}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{15}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
S_A	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
S_B	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
S_C	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
S_D	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

The proposed 17-level symmetric hybridized cascaded MLI is illustrated in Figure.3. In this topology, the operation of every H-bridge is similar to the basic Hybridised H-bridge topology as indicated in Figure. 1. In this symmetric inverter, pulses are generated using staircase modulation scheme for obtaining different output voltage levels. The pulses are generated individually and fed to the first, second, third and fourth stage respectively and finally, all the outputs of the individual stages are combined to obtain the required output voltage. The control states of the power switches are illustrated in Table 2. In this proposed topology, all the input voltage sources are fixed as

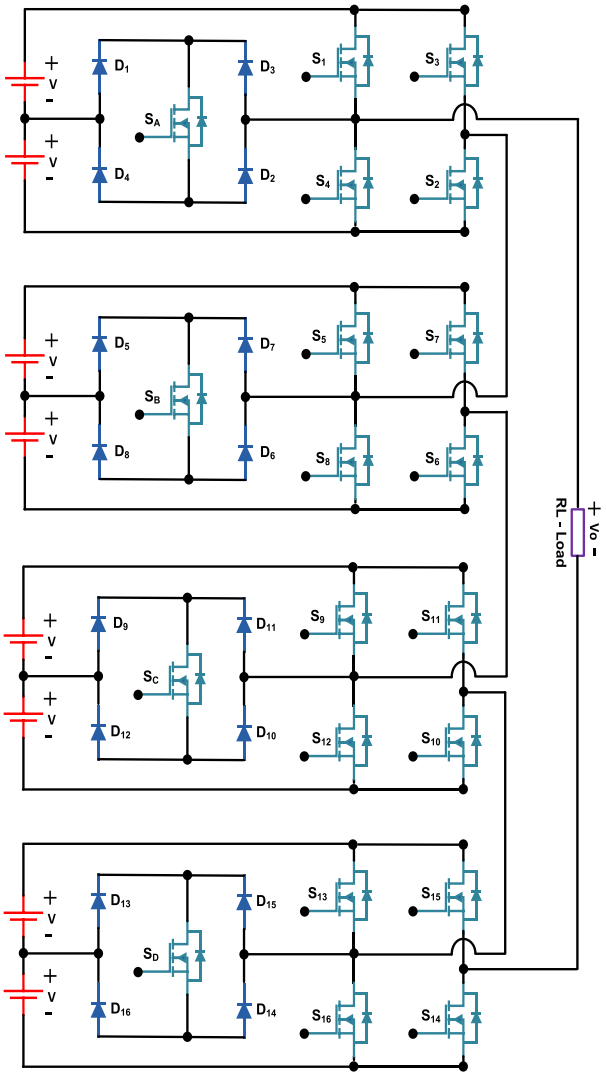

FIGURE 3. Proposed 17-level symmetric MLI.

V = 25 V for acquiring the maximum peak to peak voltage of 200 V at the load ends. The loads used for testing are 100 Ω resistor and 175 mH inductor respectively. The voltages at various stages, output voltage and current are shown in Figure.4.

III. PROPOSED ASYMMETRIC SWITCHED CAPACITOR MLI TOPOLOGY

The basic proposed switched capacitor topology is as shown in Figure.5 (a). The proposed topology consists of switched capacitor unit, diode, supply voltage and two switches. The switched capacitor doubles the input voltage at the load ends [20]–[22]. When the input voltage is applied to circuit the capacitor 'C' will charge through the S2 switch and discharge through S1, the proposed topology produces +V and +2V voltage levels at the load ends with a lesser number of switches. Figure.5 (b) shows the switching patterns for the switches S1 & S2, voltage across the capacitor during

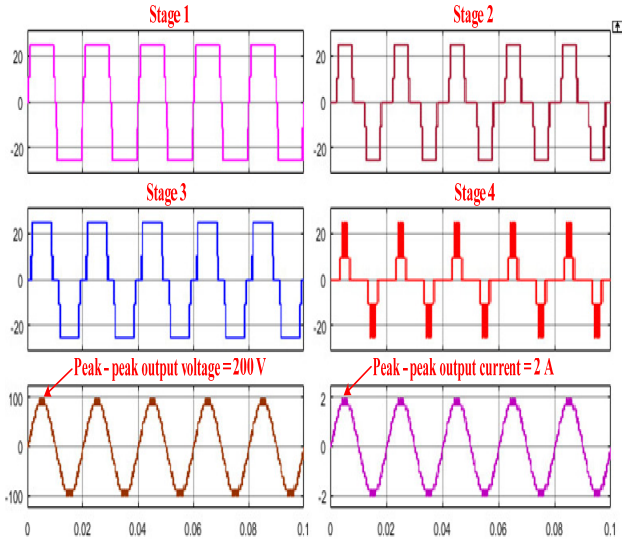

FIGURE 4. Individual stage output voltages, output voltage and current of 17-level symmetric MLI.

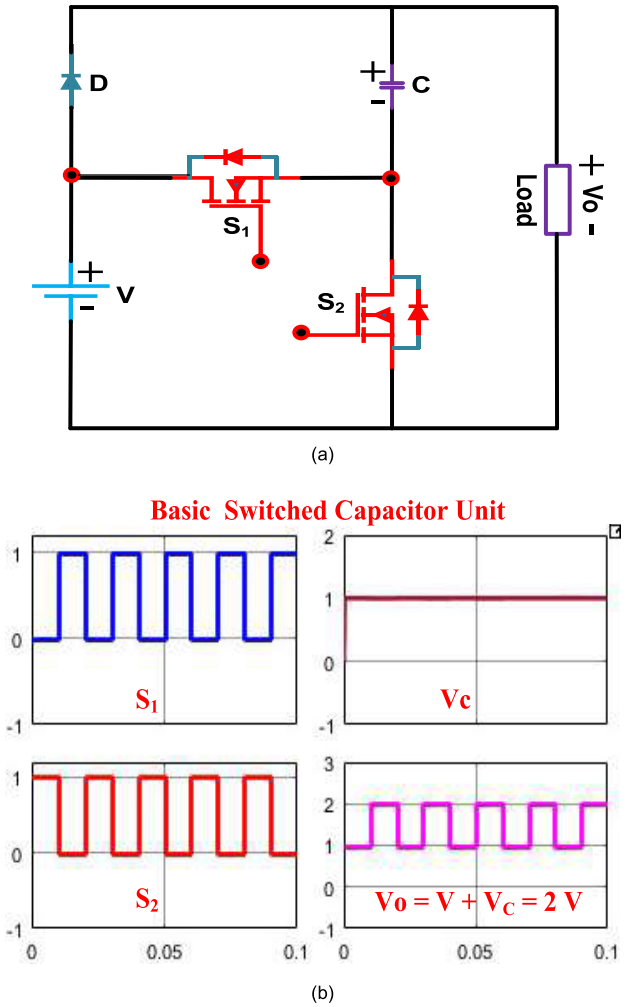

FIGURE 5. (a). Basic Proposed Switched Capacitor Unit Topology. (b). Waveforms of proposed switched capacitor unit topology.

ON & OFF period of the switch and the output voltage across the load, whenever the capacitor charges, the load voltage is equal to the input voltage and capacitor also charges to the input voltage i.e. 12.5 V. During discharge time, the load voltage is the sum of the input voltage and capacitor voltage which will be 25 V. The results show that the output voltage is doubled during capacitor discharge time. Using this topology more output voltage can be obtained for multi-levels with the minimum input voltage.

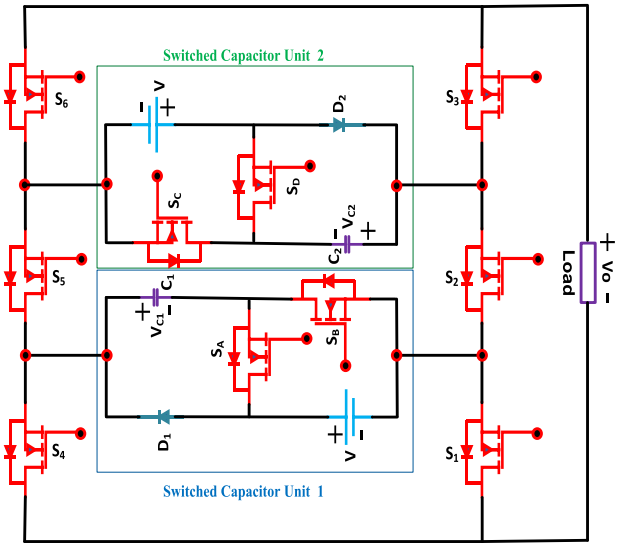

FIGURE 6. Proposed 17-level asymmetric Switched Capacitor MLI.

The proposed 17 level switched capacitor topology is shown in Figure.6. The proposed topology consists of two switched capacitor unit, having two capacitors, two diodes, two supply voltage sources and ten switches. The proposed switched capacitor units generate 17 levels at load end with 200 V (peak to peak). The pulses are generated individually and fed to the switched capacitor units and finally, all the outputs of the individual units are combined to obtain the required output voltage. The switching logic is as given in Table.3. For the proposed switched capacitor unit 1 and 2 waveforms and output voltage and current waveforms are shown in Figures.7(a),(b) & (c) respectively. The proposed 17 level inverter voltage expression and level voltages are presented in Table. 3.

IV. EXPERIMENATL RESULTS

The prototype hardware set-up for 17 level inverter systems has been implemented and tested experimentally. The proposed multilevel inverter prototype model is shown in Figure.18. The staircase modulation PWM technique is used to generate gate pulses and the same is implemented in MATLAB and the Simulink block sets are dumped into dSPACE RTI 1104 digital I/O ports. The digital I/O ports have 20 output pins for real-time interfacing application. The generated pulses from the dSPACE RTI 1104 is given to input as TLP 250 driver. The gate driver will boost the PWM pulse pattern from 5 V to 15 V because 15 V pulses will be more appropriate to turn on the power switches. The experimental

TABLE 3. Switching state table of 17-level asymmetric inverter.

V_O Level	S_1	S_2	S_3	S_4	S_5	S_6	S_A	S_B	S_C	S_D	Output voltage level expression	Output Voltage (V)
1	1	0	1	0	1	0	1	0	0	1	$4V+v_{c1}+v_{c2}$	100
2	1	0	1	0	1	0	0	1	0	1	$4V+v_{c2}$	87.5
3	0	0	1	1	1	0	0	1	1	1	$3V+v_{c2}$	75
4	1	0	1	0	1	0	1	0	1	0	$4V+v_{c1}$	62.5
5	1	0	1	0	1	0	0	1	1	0	4V	50
6	0	0	1	1	1	0	0	1	1	0	3V	37.5
7	1	0	0	0	1	1	1	0	0	0	$V+v_{c1}$	25
8	1	0	0	0	1	1	0	1	0	0	V	12.5
9	1	1	1	0	0	0	0	1	1	0	0	0
10	0	1	1	1	0	0	0	1	0	0	$-V_1$	-12.5
11	0	1	1	1	0	0	1	0	1	0	$-V-V_{C1}$	-25
12	1	1	0	0	0	1	0	1	1	0	-3V	-37.5
13	0	1	0	1	0	1	0	1	1	0	-4V	-50
14	0	1	0	1	0	1	1	0	1	0	$-4V-V_{C1}$	-62.5
15	1	1	0	0	0	1	0	1	0	1	$-3V-V_{C2}$	-75
16	0	1	0	1	0	1	0	1	0	1	$-4V-V_{C2}$	-87.5
17	0	1	0	1	0	1	1	0	0	1	$-4V-V_{C1}-V_{C2}$	-100

model specifications are given in Table.4. The results are validated at steady state, load disturbance conditions and also performed with resistive & inductive loads and THD which are shown in Figure.8, Figure.9, Figure.10, Figure.11, Figure.12, Figure.13, Figure.14, Figure.15, Figure.16 and Figure 17 respectively.

A. SYMMETRIC HYBRIDESED CASCADED MLI

The steady state testing has been performed with resistive load (unity power factor load) with 200 V peak to peak output voltage. The obtained output current is about 4 A, peak to peak. The RMS value of the output voltage and current obtained are 67.92 V and current 1.404 A respectively. The hardware results are shown in Figure.8. The prototype experimental results evidently show that with 17 levels in the output voltage the waveform visibly shows that the phase angle between load voltage and the load current is zero. After the completion of steady-state testing with a resistive load and an inductive load (lagging power factor load) with 200V, peak to peak output voltage. The output current noticed is around 3.5A, peak to peak. The attained RMS value of the output voltage and current are 67.91V and 1.15A respectively, the achieved hardware results are tabulated in Table.5 & 6. The experimental results are given in Figure.9. The waveform clearly shows the phase angle between load voltage and the load current is lagging. In certainty, loads rarely exist distinctly.

The loads will always occur as a combination of resistance and inductance. Usually, in any particular place, when a resistive load is being utilized an abrupt accumulation of inductive load in parallel to the resistive load or vice versa is likely to be identical. Even at these circumstances, the output voltage must stay in steady state and the same is as shown in Figure.10 and Figure.11 and THD is shown in Figure.12 respectively.

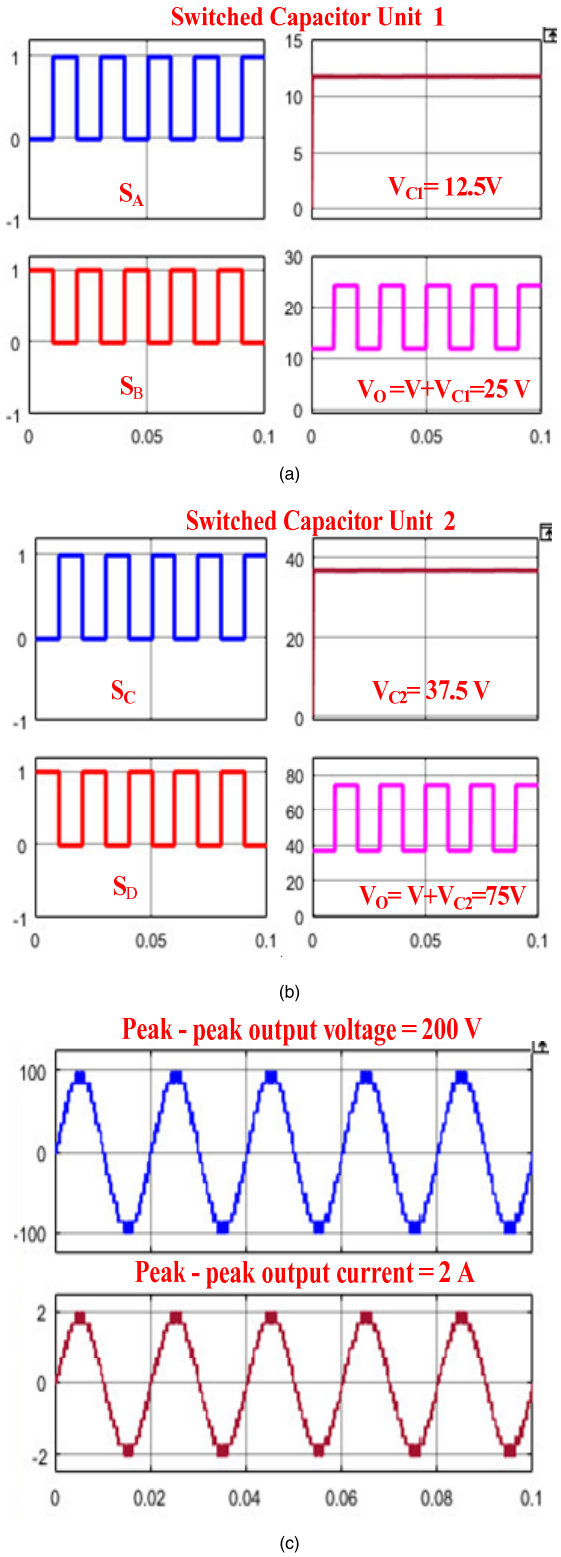

FIGURE 7. (a). Waveforms of proposed switched capacitor unit 1 for 17 level MLI. (b). Waveforms of proposed switched capacitor unit 2 for 17 level MLI. (c). Output voltage and current waveforms of 17-level asymmetric Switched Capacitor MLI.

B. ASYMMETRIC SWITCHED CAPACITOR MLI

The steady state testing has been performed with resistive load (unity power factor) with 200V (peak to peak)

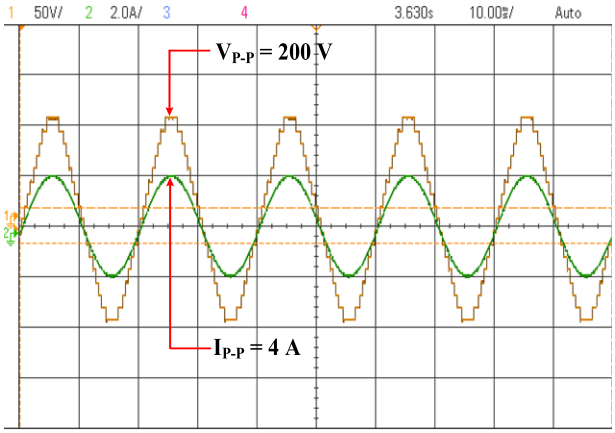

FIGURE 8. Steady-state voltage and current response of 17 level symmetric inverter with a resistive load.

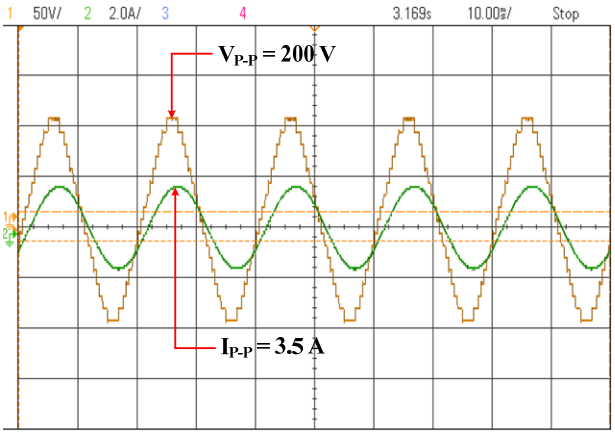

FIGURE 9. Steady-state voltage and current response of 17 level Symmetric inverter with inductive load.

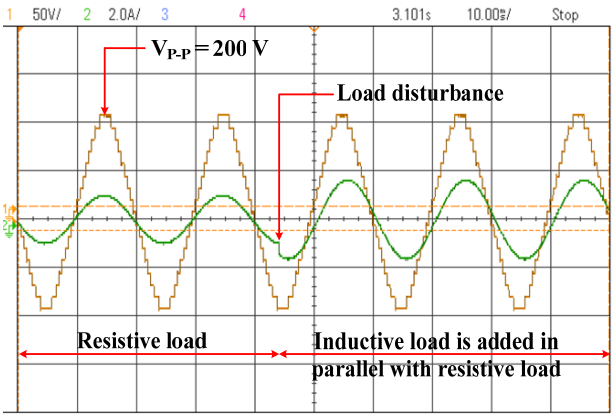

FIGURE 10. Unity power factor to lagging power factor load disturbance response of 17 level symmetric inverter.

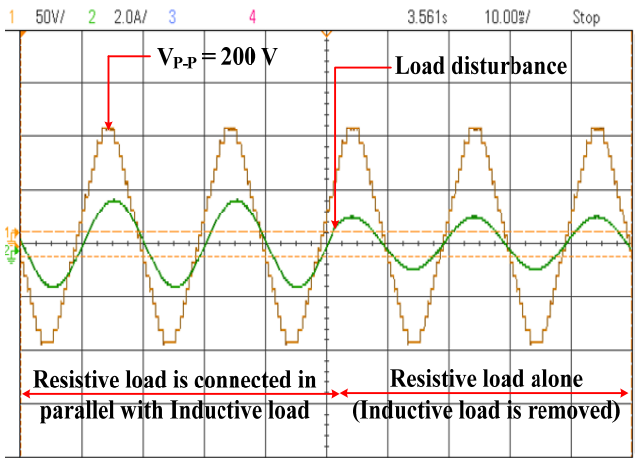

FIGURE 11. Lagging power factor to unity power factor load disturbance response of 17 level symmetric inverter.

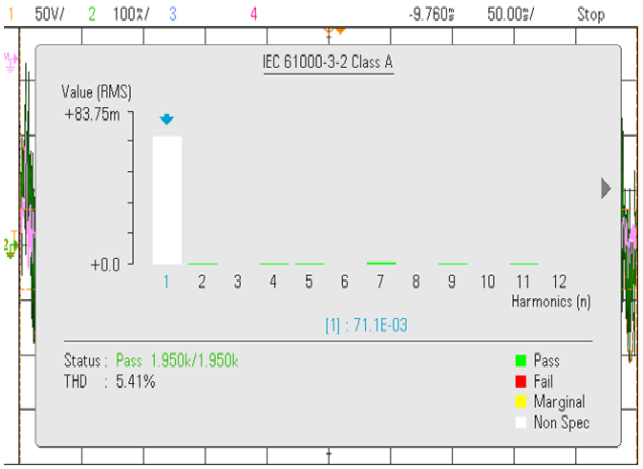

FIGURE 12. THD –17 level symmetric inverter.

TABLE 4. Experimental specifications.

Item	Specification
DC Sources	0-30V
MOSFETs	IRF 840
Diodes	IN914
Capacitors	100 µF
Controller	dSPACE RTI Controller, digital I/O ports
GATE Driver	TLP 250
R_{Load}	50 Ω,100 Ω
L_{Load}	175 mH

output voltage. The output current obtained is 2A peak to peak. The RMS value of the output voltage and current were obtained at 72.72V and current 0.7A respectively. The prototype results are shown in Figure.13. The experimental results clearly show that with 17 levels in the output voltage the phase angle between load voltage and the load current is zero. After the completion of steady-state testing with a resistive load, the inductive load has been introduced to the topology at 200V peak to peak output voltage. The output current obtained is about 3.6A peak to peak. The RMS value

TABLE 5. Comparison of proposed topologies.

Item	17 level Symmetric MLI	17 level Asymmetric MLI
DC Sources	8	2
Switches	20	10
Diodes	0	2
Capacitors	0	2

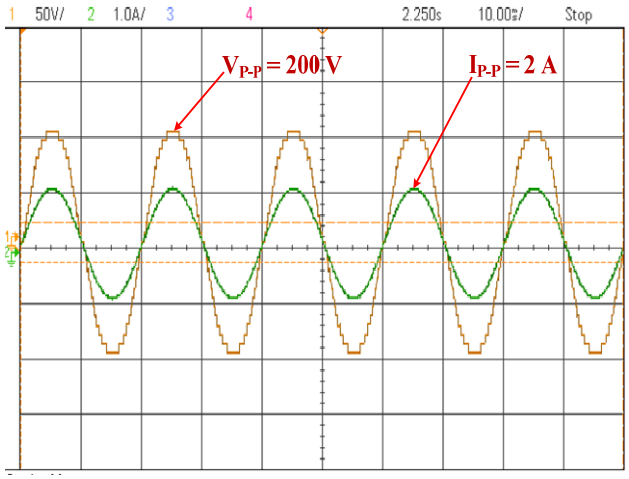

FIGURE 13. Steady state voltage and current response of 17 level asymmetric inverter with resistive load.

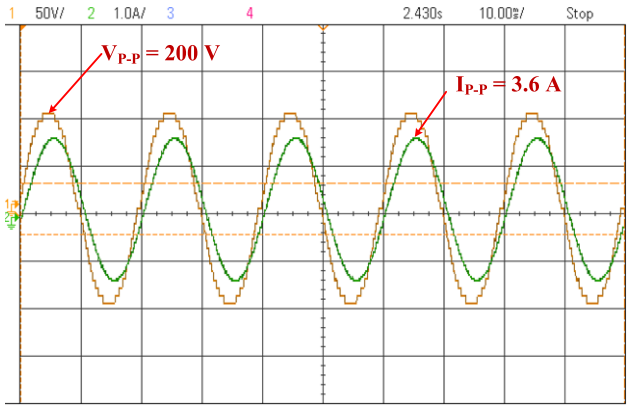

FIGURE 14. Steady-state voltage and current response of 17 level asymmetric inverter with inductive load.

of the output voltage and current is around 72.71V and current 1.06A respectively and the hardware results acquired are indicated in Table.5 & 6. The obtained experimental results are depicted in Figure.14. The results clearly show that with 17 levels the output voltage clearly shows that the phase angle between load voltage and the load current is lagging. They will continuously occur in a combination of resistive and inductive loads. Typically, in most applications, when a resistive load is being applied, an abrupt addition of inductive load in parallel to the resistive load or vice versa is very likely. Even at these conditions, the output voltage needs to stay in stable condition as shown in Figure 15, Figure 16 and THD is shown in Fig.17 respectively.

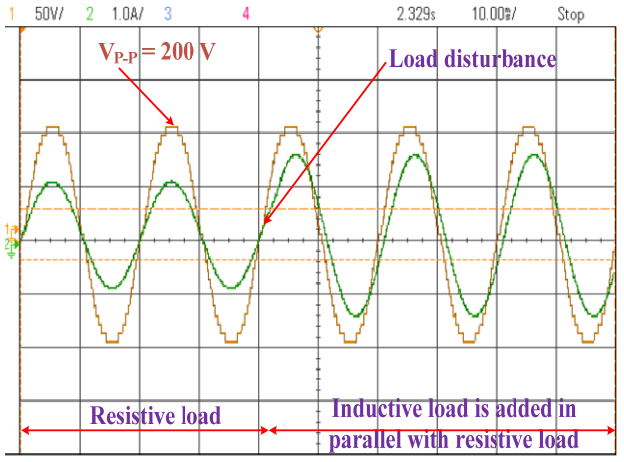

FIGURE 15. Unity power factor to lagging power factor load disturbance response of 17 level asymmetric inverter.

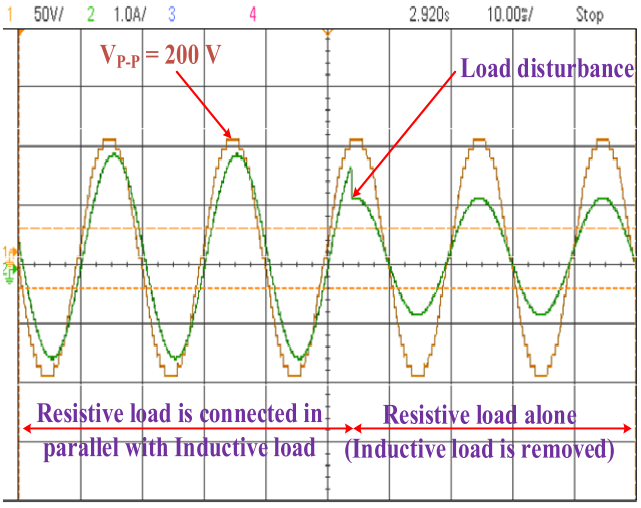

FIGURE 16. Lagging power factor to unity power factor load disturbance response of 17 level asymmetric inverter.

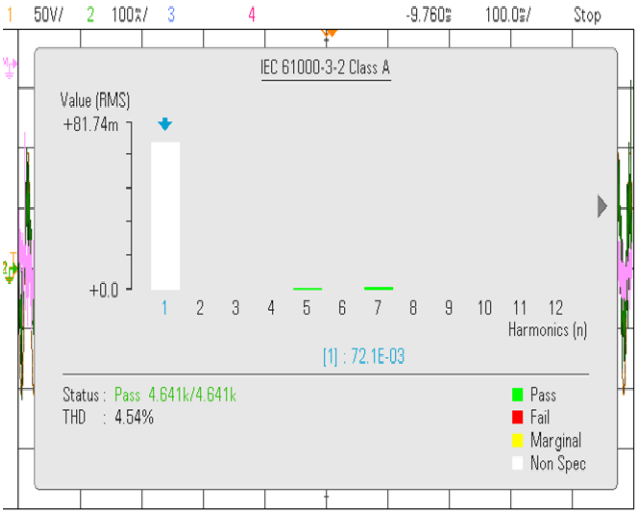

FIGURE 17. THD –17 level asymmetric inverter.

TABLE 6. Experimental output parameters.

Type of inverter configuration	Output Parameters							
	Type of Load	Output Peak-Peak voltage (Volts)	Output RMS voltage (Volts)	Output Peak-Peak current (Amps)	Output RMS Current (Amps)	Frequency (Hz)	Output Power (Watts)	THD (%)
17-level Symmetric	R -load	200	67.92	4	1. 404	50	95.35	5.41
17-level Symmetric	L -load	200	67.91	3.5	1.156	50	77.07	
17-level Asymmetric	R -load	200	72.72	2	0.7	50	50.9	4.54

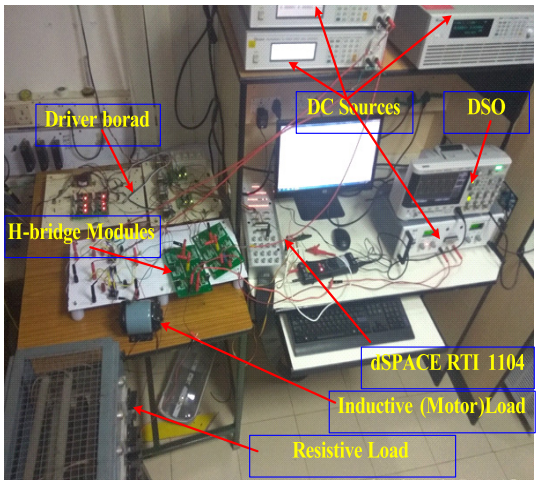

FIGURE 18. Experimental set-up proposed inverter.

V. CONCLUSIONS

This research presents the implementation and analysis of a 17 level symmetric and asymmetric multilevel inverters. The proposed 17 level inverter systems have been effectively tested with unity and lagging power factor loads. In case A, testing has been carried out under steady-state condition, load disturbance conditions and analysis of THD with 17 level symmetric inverter output were presented. It is inferred from case A results that the system is readily adaptive and maintains a stable output voltage with 5.41 % THD for the aforesaid conditions while in case B, a THD with 4.54 % has been achieved, which is on par with IEEE standards. During load disturbances, the proposed topology is suitable for sudden load variant applications also. Due to low THD, these topologies inherently utilize a lesser number of switches and a minimum number of dc input voltage sources; hence, the volume density of the proposed inverter is observed to have improved. From case A and B results it can be inferred that the proposed topology multilevel inverters are suitable for renewable energy-fed applications.

REFERENCES

[1] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6664–6671, Dec. 2014.

[3] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3109–3118, Nov. 2011.

[4] B. P. Reddy, M. R. A, M. Sahoo, and S. Keerthipat, "A fault tolerant multilevel inverter for improving the performance of pole-phase modulated nine-phase induction motor drive," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2017.2733474.

[5] H. M. Basri1 and S. Mekhile, "Digital predictive current control of multi-level four-leg voltage-source inverter under balanced and unbalanced load conditions," *IET Electr. Power Appl.*, vol. 11, no. 8, pp. 1499–1508, 2017.

[6] Y. Lei *et al.*, "A 2-kW single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570–8581, Nov. 2017.

[7] Y. Suresh and A. K. Panda, "Investigation on hybrid cascaded multilevel inverter with reduced dc sources," *Renew. Sustain. Energy Rev.*, vol. 26, pp. 49–59, Oct. 2013.

[8] C. I. Odeh and D. B. N. Nnadi, "Single-phase, 17-level hybridized cascaded multi-level inverter," *Electr. Power Compon. Syst.*, vol. 41, no. 2, pp. 182–196, 2013.

[9] M. F. M. Elias, N. A. Rahim, H. W. Ping, and M. N. Uddin, "Asymmetrical cascaded multilevel inverter based on transistor-clamped H-bridge power cell," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4281–4288, Nov./Dec. 2014.

[10] J. Dixon and L. Moran, "High-level multistep inverter optimization using a minimum number of power transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 330–337, Mar. 2006.

[11] S.-J. Park, F.-S. Kang, M. H. Lee, and C.-U. Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 831–843, May 2003.

[12] S. J. de Mesquita, F. L. M. Antunes, and S. Daher, "A high resolution output voltage multilevel inverter topology with few cascade-connected cells," in *Proc. 29th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 289–296.

[13] C. I. Odeh and D. B. N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," *IET Power Electron.*, vol. 6, no. 3, pp. 468–477, 2013.

[14] F.-S. Kang, S.-J. Park, S. E. Cho, C.-U. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[15] C. I. Odeh, D. B. Nnadi, and E. S. Obe, "Three-phase, five-level multilevel inverter topology," *Electr. Power Compon. Syst.*, vol. 40, no. 4, pp. 1522–1532, 2012.

[16] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156–1169, Feb. 2017.

[17] S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and H. M. Suryawanshi, "A fundamental frequency hybrid control technique based three phase cascaded multilevel inverter topology," *IEEE Access*, to be published, doi: 10.1109/ACCESS.2017.2727551.

[18] P. L. Kamani and A. M. Mulla, "Middle-level SHE pulse-amplitude modulation for cascaded multilevel inverters," *IEEE Trans. Ind. Informat.*, to be published, doi: 10.1109/TIE.2017.2742990.
[19] L. Wang, Q. H. Wu, and W. Tang, "Novel cascaded switched-diode multilevel inverter for renewable energy integration," *IEEE Trans. Energy Convers.*, to be published, doi: 10.1109/TEC.2017.2710352.
[20] S. R. Raman, K. W. E. Cheng, and Y. Yuanmao, "Multi-input switched-capacitor multilevel inverter for high-frequency ac power distribution," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2017.2742525.
[21] A. Taghvaie, J. Adabi, and M. Rezanejad, "A multilevel inverter structure based on a combination of switched-capacitors and DC sources," *IEEE Trans. Ind. Informat.*, to be published, doi: 10.1109/TII.2017.2710265.
[22] V. Pakala and S. Vijayan, "A new DC-AC multilevel converter with reduced device count," *Int. J. Intell. Eng. Syst.*, vol. 10, no. 3, pp. 391–400, 2017.

C. DHANAMJAYULU received the B.Tech. degree in electronics and communication engineering from JNTU University, Hyderabad, the M.Tech. degree in control and instrumentation systems from IIT Madras. He is currently pursuing the Ph.D. degree with the School of Electrical Engineering, Vellore Institute of Technology, Vellore, India. He is also an Assistant Senior Professor with the School of Electrical Engineering, Vellore Institute of Technology. His major interest areas are multilevel inverters, power converters, and active power filters and power quality.

S. MEIKANDASIVAM received the Bachelor's degree in electrical and electronics engineering in 2002, the Master's degree in power systems in 2005, and the Ph.D. degree from the Maulana Azad National Institute of Technology, Bhopal, India, in 2010. Since 2010, he has been an Associate Professor with the School of Electrical Engineering, Vellore Institute of Technology, Vellore.