Research Article
Implementation of Cascaded H-Bridge Multilevel Inverter using MATLAB-DSP (ezDSP28335) Interfacing

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Abstract: This study demonstrates, the generation of triggering signals using SPWM technique for a seven level H-Bridge cascaded inverter with the help of MATLAB-DSP (ezDSP 28335) interfacing without using EPWM block and presents the final output of the inverter. The focus is mainly on hardware implementation of Cascaded H-Bridge MLI using MATLAB-DSP interfacing. Generation of triggering signals using MATLAB-DSP interfacing has been explained briefly. Use of GPIO block in SIMULINK model makes the triggering signal generation easier and more efficient. The switching control signals required for triggering of switches are generated using MATLAB-DSP (ezDSP 28335) interfacing. This approach exploits the advantages of block programming in SIMULINK.

Keywords: Cascaded multilevel inverter, CCSV 3.3, DSP, MATLAB, RTW, SPWM

INTRODUCTION

The increasing number of sensitive loads on electrical utility requires high power quality. Also for medium voltage grid it is troublesome to connect only one power semiconductor switch directly (Tolbert *et al*., 1999; Tolbert and Peng, 2000). Multilevel Inverters (MLIs) have been developed to fulfill these requirements. Several topologies have been developed during the last two decades. Some of these topologies are:

- Cascaded H-Bridge MLI
- Diode clamped
- Flying capacitors

Multilevel inverter synthesizes stepped output voltage nearly equal to sine wave using single or multiple DC sources (Tolbert *et al*., 1999; Peng and Qian, 2003). Traditionally, the multi-pulse inverter comprising of several Voltage Source Inverters (VSIs) connected together through zigzag arranged transformers were used. But these transformers are expensive, inefficient, occupy large area and are prone to failure. Multilevel inverters were first introduced in 1975 as a solution to the above problem. The terms multilevel were first used for three level and further many topologies have been discovered. Three major topologies are:

- Cascaded H-Bridge MLI
- Diode clamped or Neutral clamped
- Flying capacitors or Capacitor clamped (Rodríguez *et al*., 2002; Sadigh and Barakati, 2012; Beser *et al*., 2008)

Among these three topologies mentioned above the Cascaded H-Bridge is simplest (Ali Khajehoddin *et al*., 2007). In this structure M-level output is synthesized using (M-1) /2 H-bridges. Each H-Bridge has its own isolated DC source. The cascaded single phase 7-level inverter as shown in Fig. 1 has ((7-1) /2 = 3) three H-Bridges with three isolated DC sources (Peng and Lai, 1997; Sujitha and Ramani, 2012). The Cascaded MLI:

- Eliminates the bulky transformers required in multi-pulse inverter
- Can generate almost sinusoidal waveform
- Has fast dynamic response

Due to its simple and modularized structure it can be made up to unlimited number of levels. This inverter has low cost, high performance, less electromagnetic interferences and higher efficiency than traditional multi-pulse inverter (Liu and Leng, 2012). It can reduce dv/dt stress; thereby electromagnetic compatibility problem can be reduced (Rokan *et al*., 2010).

In the recent years several strategies and control methods have been developed for switching the devices in the H-bridge (Peng and Qian, 2003; Lesan *et al*., 2009). Some of them are sinusoidal Pulse with Modulation (SPWM), Selective Harmonics Elimination (SHE-PWM), Space Vector Modulation (SVM) and others (Holmes and Lipo, 2013; Zafarullah Khan *et al*., 2009). Each method has its own benefits and short comings. This study demonstrates, the generation of triggering signals using SPWM technique for a seven level H-Bridge cascaded inverter with the help of MATLAB-DSP (ezDSP 28335) interfacing without
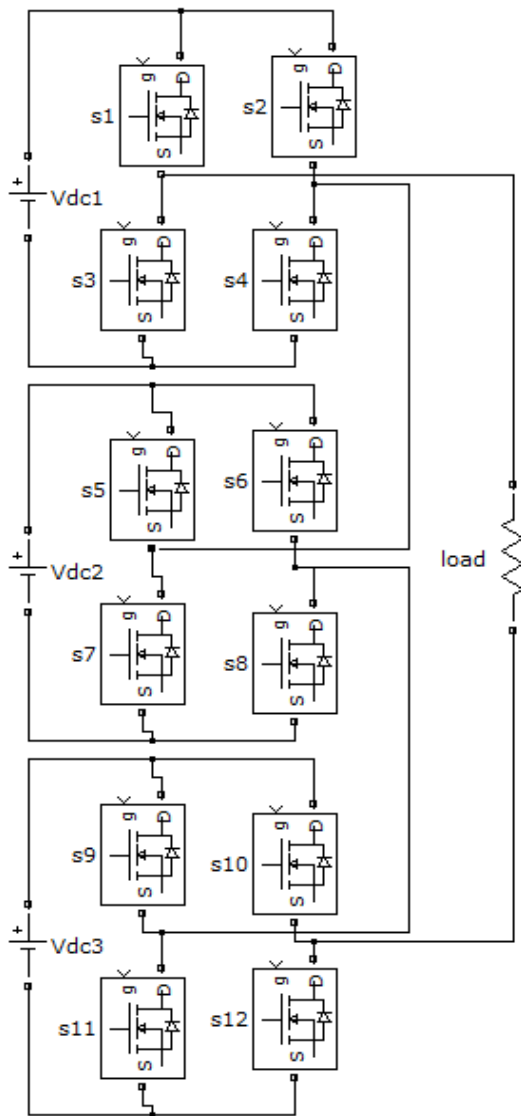
Fig. 1: Single phase 7-level inverter

using EPWM block. Further the Real Time Workshop (RTW), a SIMULINK add-on software, which automatically generates C and ADA codes from SIMULINK model, allows the integration of a simulation software to the development environment (Pop *et al*., 2004). The system designer can implement the algorithm using SIMULINK blocks and convert these blocks in to executable binary codes in C or Assembly language using RTW.

MATERIALS AND METHODS

SPWM generation using MATLAB-DSP interfacing: Generation of triggering signals using DSP for the control of voltage source inverters has helped substantially in the development of electric drives used in many industrial applications (Hercog *et al*., 2003). Although there are several ways of generating the

triggering signals using DSP, the one using MATLAB-DSP interfacing has its own advantages. SIMULINK is MATLAB add-on software which allows block programming. Hence, the system designer can simply use the blocks to implement the algorithms rather than giving more time in developing codes. Further the Real Time Workshop (RTW), a SIMULINK add-on software, which automatically generates C and ADA codes from SIMULINK model, allows the integration of a simulation software to the development environment. The system designer can implement the algorithm using SIMULINK blocks and convert these blocks in to executable binary codes in C or Assembly language using RTW. Subsequently these codes are executed in Code Composer Studio (CCSV 3.3), DSP software and downloaded in to the connected DSP processor. The outputs can be taken out from the pins available on the DSP processor board. In the case of signal generation for triggering H-bridge switches, Sine-wave Pulse Width Modulation (SPWM) can be generated easily using EPWM block available under the target preference blocks section in SIMULINK. But due to the limited number of EPWM pins, in EPWM output pins which are available in ezDSP 28335 board makes its unsuitable for the higher level H-Bridge application. Hence, another approach to generate SPWM for triggering 7-level H-bridge is described stepwise in the following section.

Triggering signal generation for single phase 7-level H-bridge:

Step 1: Connect the ezDSP 28335 processor to cc studio. Open MATLAB and type *ccsboardinfo* in the workspace and press enter. The connected DSP processor name will be displayed in the workspace.

Step 2: Connect the blocks as shown in Fig. 2.

Step 3: Change the sine wave block parameters, sine type to sample based. Give sample per period as 100 and sample time as 0.0002 for a 50 Hz signal. The amplitude of sine wave is kept 2.5. The repeating sequence stair is given parameters such as to give a discretized up-down triangle such as vector of output values is changed to (0 0.5 1 1.5 2 2.5 3 3 2.5 2 1.5 1 0.5 0) and sample time is changed to 0.00005 for approximately 1.5 kHz switching frequency. The resulting simulation output is shown in Fig. 3. Which shows the triggering pulse for the positive half cycle of a two level inverter.

The hardware output can be taken out from the GPIO0 pin (p8-9th pin and ground pin (p8-19th) of the DSP processor. Figure 4 shows the DSO output of the above simulation out of the DSP kit for both positive and negative half cycles of a two level inverter. For
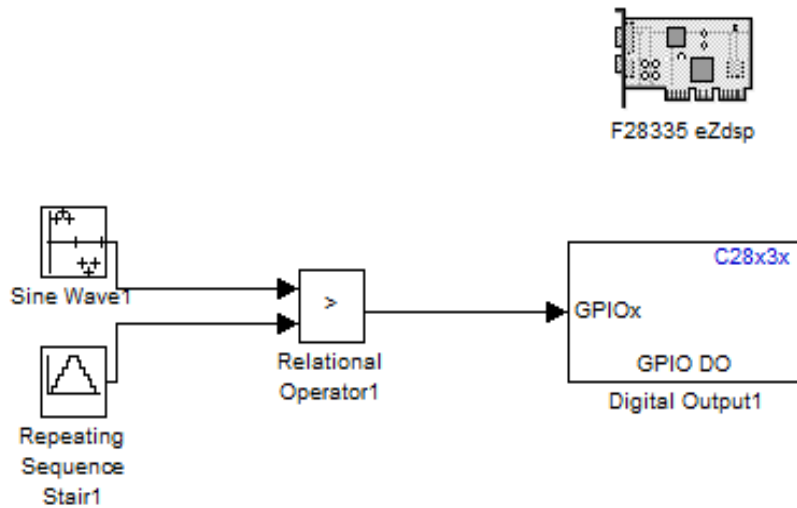
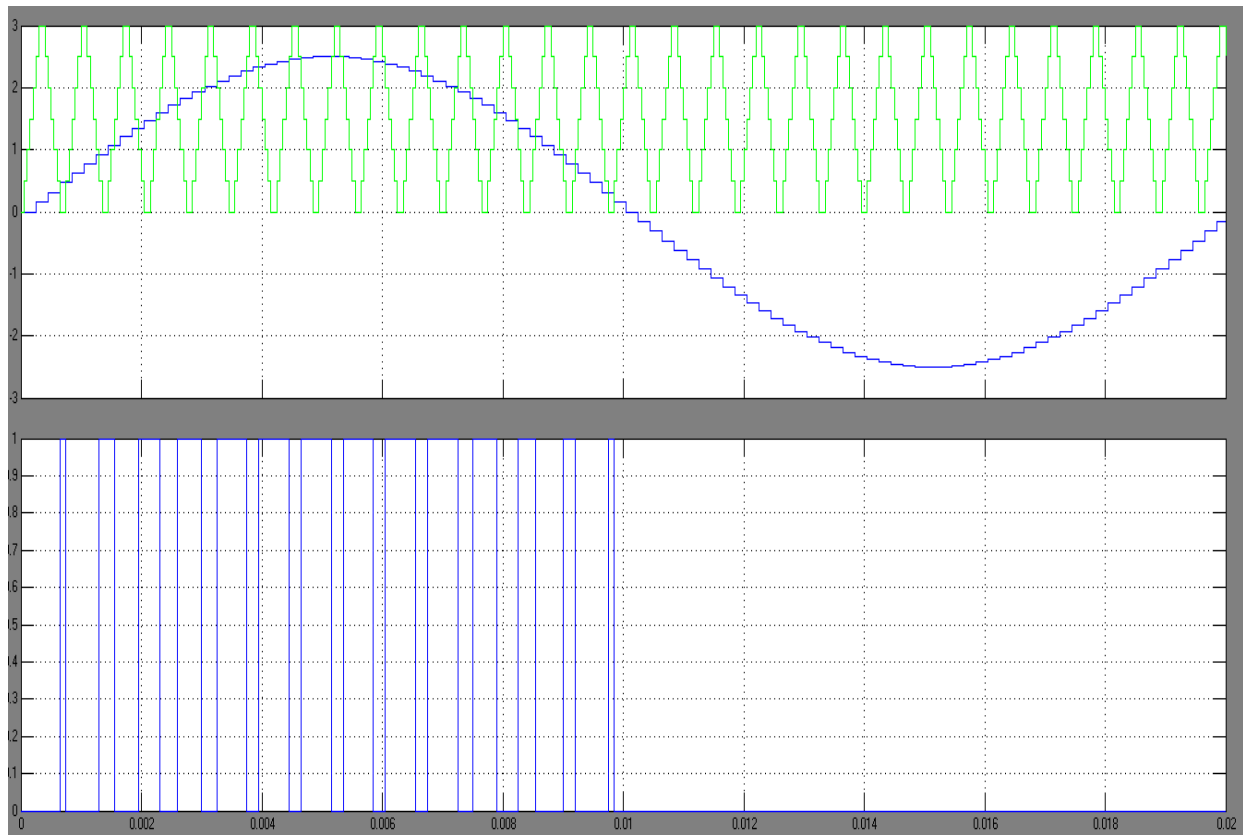Fig. 2: SIMULINK block diagram to generate SPWM

Fig. 3: Simulation output of 2-level positive cycle SPWM

getting the negative half cycle pulse, invert the sine wave input by adding a-1 gain block between the sine block and compare block and configure the digital output block for another output pin say GPIO1. Take the negative cycle output from the GPIO1 pin as given in the processor manual. Figure 5 shows the output of the 2 level H-bridge inverter resulting output of the signals of Fig. 4.

Step 4: For a 7-level inverter we need six pulses of different width and at different times to trigger the switches of three H-bridges connected in cascade as shown in Fig. 1. To get the correct sequence of switching, three shifted carrier waves are compared with sine wave (both for positive and negative cycles). For getting the shifted carrier waves the vector of output
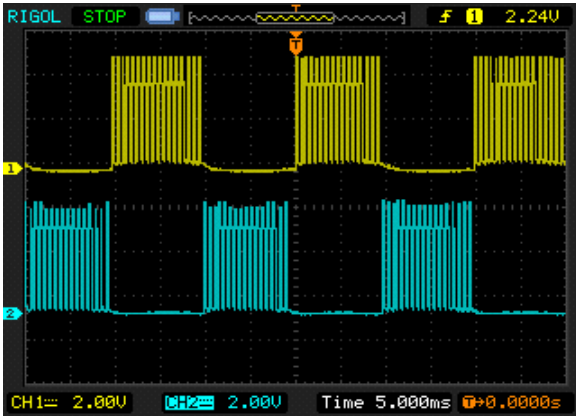
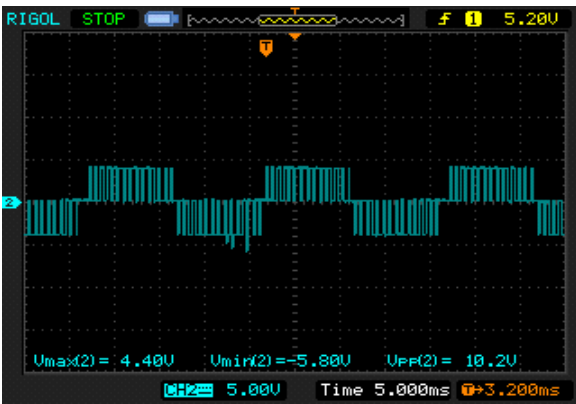Fig. 4: DSO output of 2 levels H-bridge inverter triggering generated in ezDSP28335 processor

Fig. 5: 2-level inverter hardware output

values parameter in repeating sequence stair block is changed to (0 0.2 0.4 0.6 0.8 1 1 0.8 0.6 0.4 0.2 0) for 1st signal and its complementary 4th signal for the negative cycle, (1 1.2 1.4 1.6 1.8 2 2 1.8 1.6 1.4 1.2 1) for 2nd signal and its complementary 5th signal for the negative cycle and (2 2.2 2.4 2.6 2.8 3 3 2.8 2.6 2.4 2.2 2) for 3rd signal and its complementary 6th signal for the negative cycle. The Digital output block is configured for six different pins say GPIOx (x = 0, 1, 2, 3, 4, 5).

Step 5: Build the model in SIMULINK. This will convert the model in to C and Assembly language code files. Automatically a project of the same name as that of SIMULINK model will be created in CC Studio and it is built and downloaded automatically in the DSP processor. Now, the simulation and the hardware output of the triggering signals for 7-level H-Bridges can be seen as shown in Fig. 6 and 7.

RESULTS AND DISCUSSION

The triggering signal output of DSP is used to trigger the switches in the H-bridges. The SIMULINK model for 7-level H-bridge, connected to the above generated signal, is shown in Fig. 8. As can be seen in the figure there are three bridges each consisting of four switches and have isolated DC supplies. The first and fourth signals from the top, shown in Fig. 6, are given
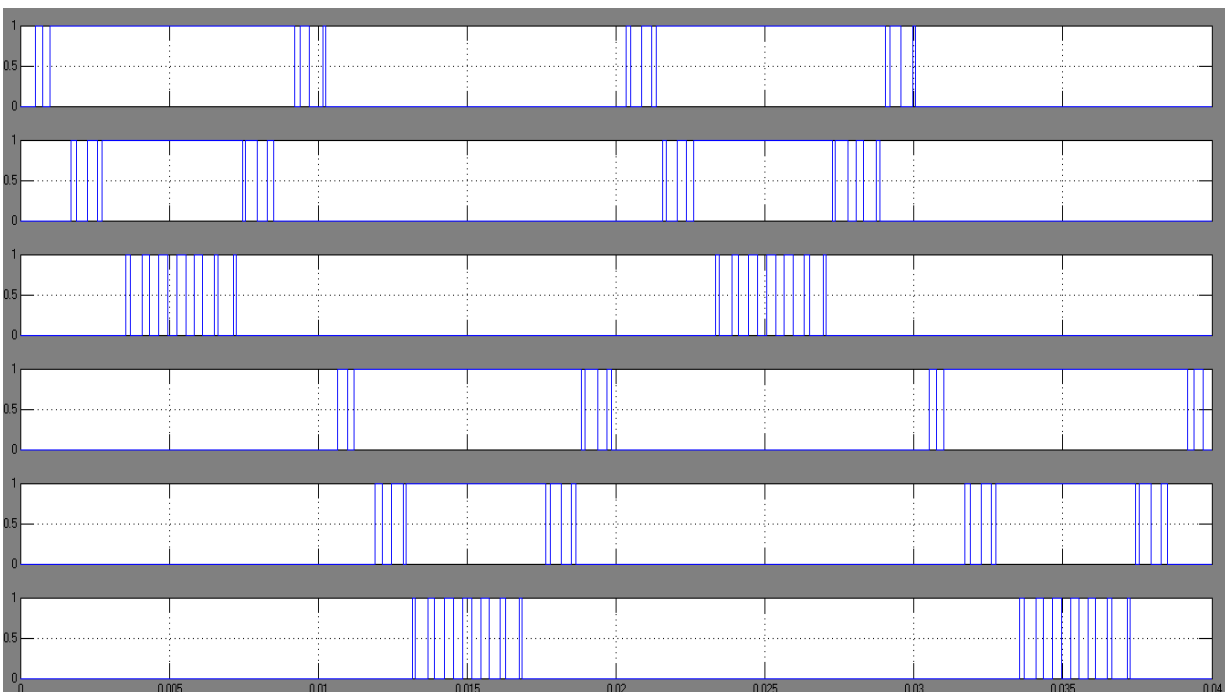

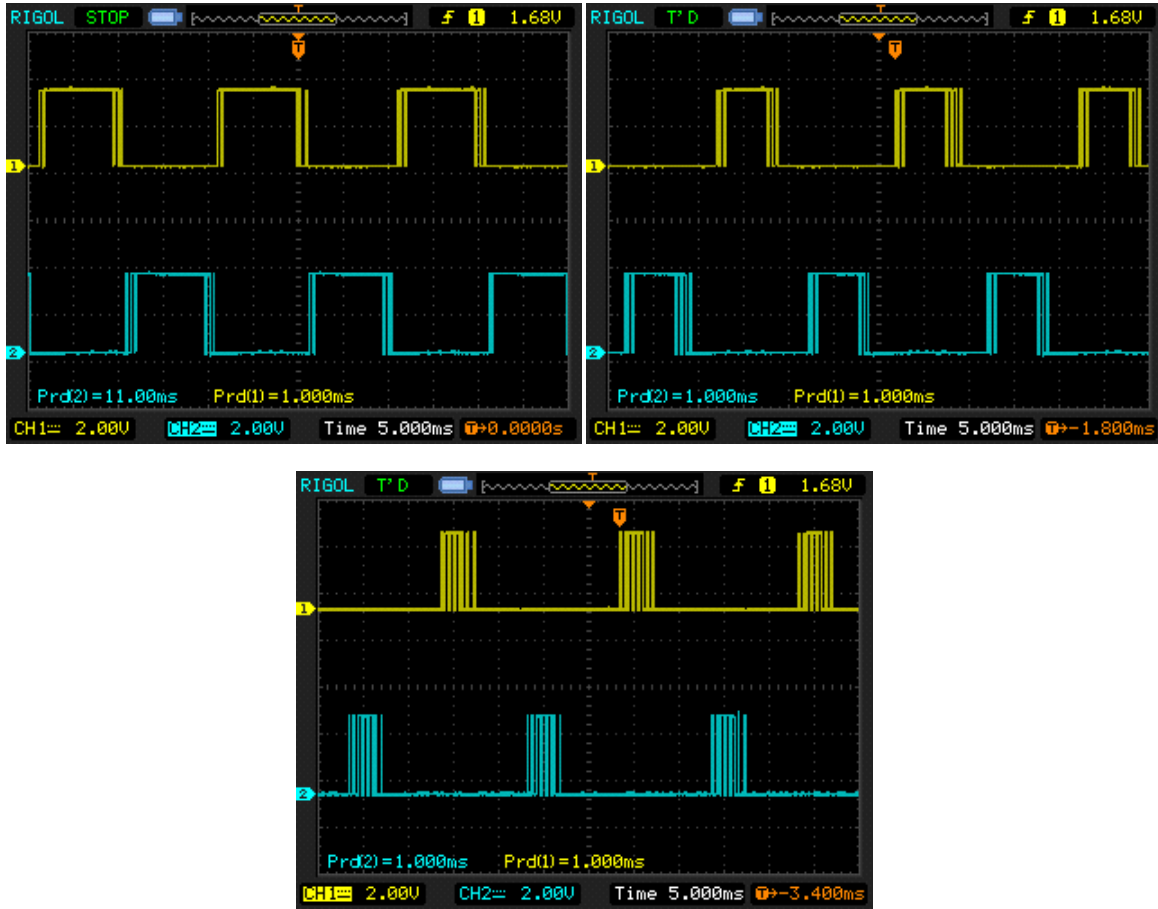Fig. 6: Simulation output of triggering signals

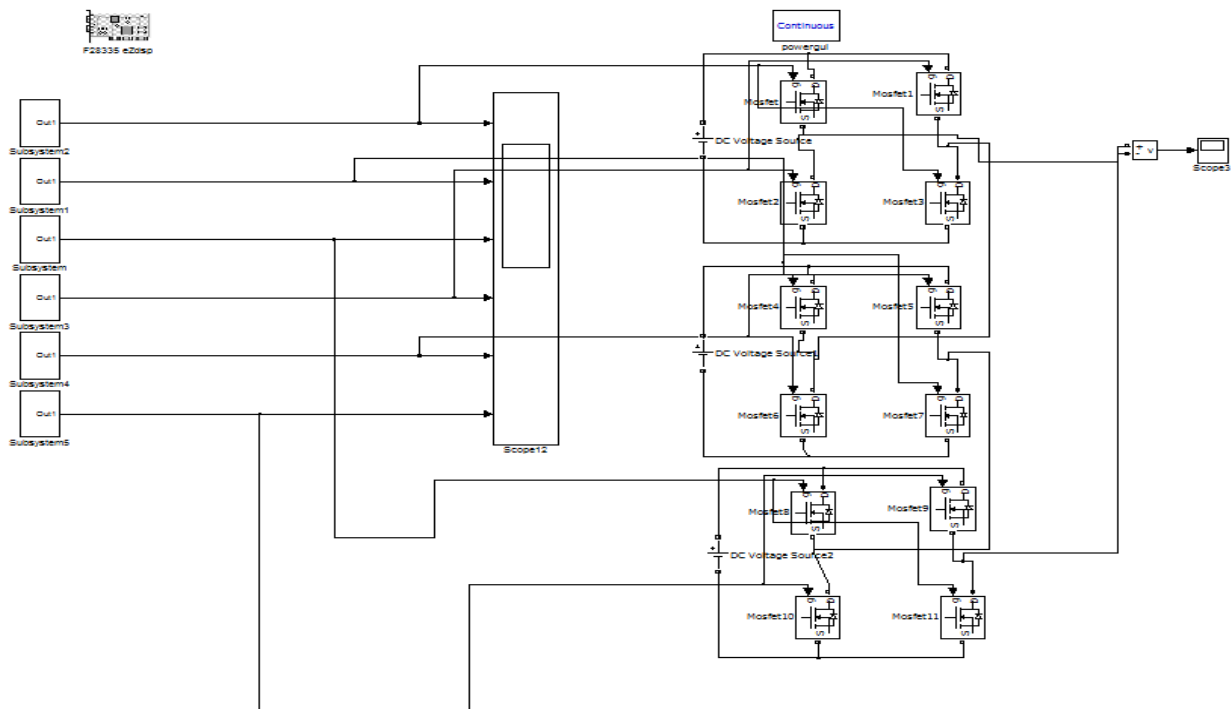Fig. 7: Hardware output of triggering signals for three H-bridges

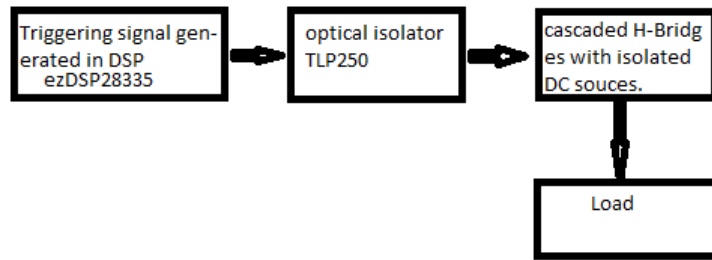Fig. 8: SIMULINK model for 7-level inverter

Fig. 9: Block diagram of the hardware connection

Fig.10: Hardware setup for 7-level cascaded H-bridge inverter using MATLAB-DSP interfacing
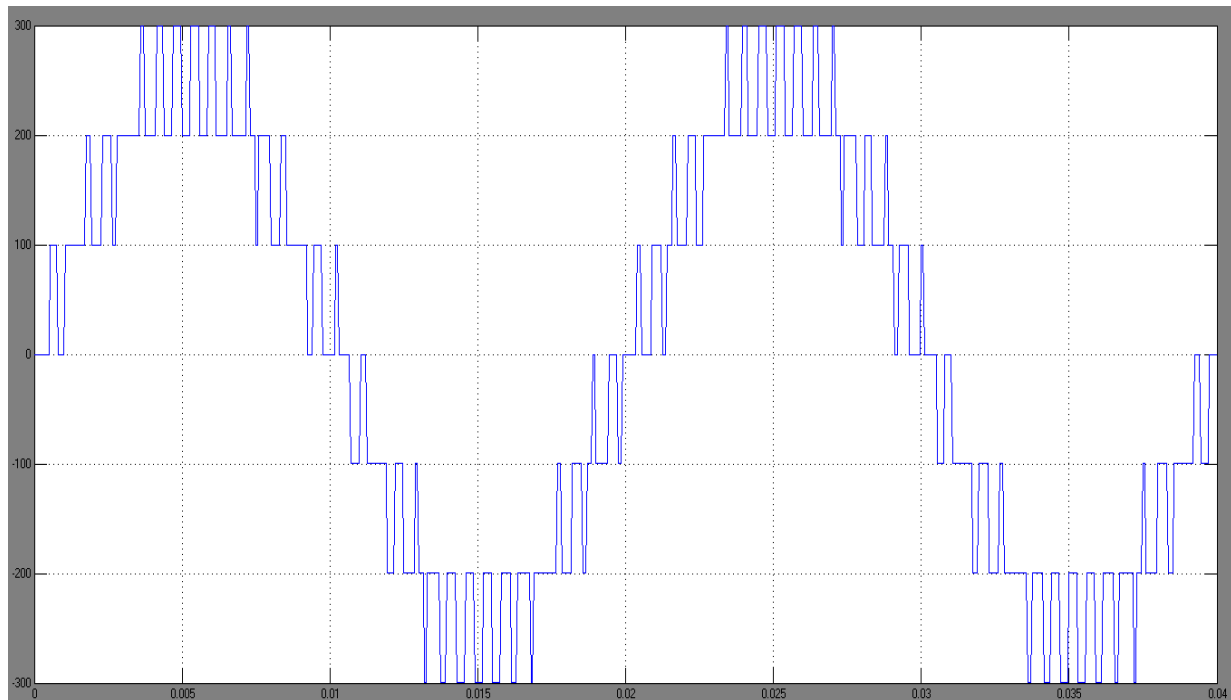

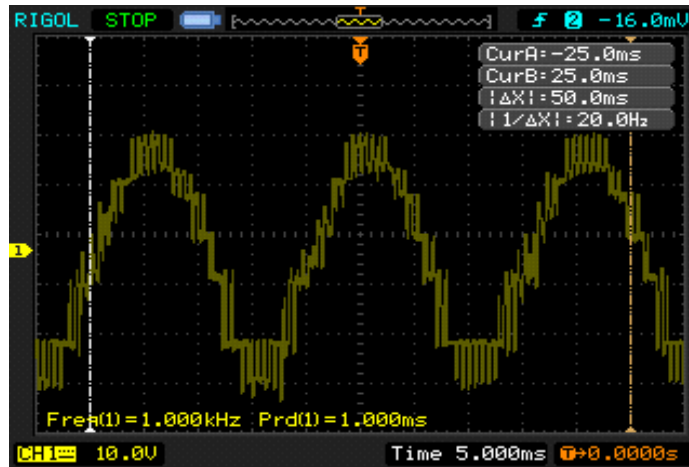Fig. 11: Simulation output of 7-level inverter cascaded H-bridges

Fig. 12: Hardware output of three H-bridge

to the prime and anti-diagonal switches respectively of the first bridge, second and fifth signals are given to the to the prime and anti-diagonal switches respectively of the second bridge, similarly third and sixth signals are given to the prime diagonal and anti-diagonal switches respectively of the third bridge. The individual outputs of the three bridges are connected in cascade.

The hardware connection of the simulation described above has similar structure except some small modification. A schematic block diagram of the hardware connection is shown in Fig. 9. The first block represents the triggering signals generation through DSP. The second block is the only modification in the hardware connection from that of in simulation. This is the isolation required to protect the low voltage part from the irregularities of the high voltage part. For this project we have used an IC TLP 250 as an isolator. This IC converts the signals from DSP kit in to optical signals and again the optical signals are converted back to the electrical form. Hence the low and high voltage sides are not electrically connected but optically isolated. The third and fourth blocks represent bridges and load similar to the SIMULINK model.

Figure 10 shows the hardware setup for the project. The picture has desktop and DSP kit for the MATLAB-DSP inter facing, the set of opto-couplers for isolation and bridges for the inverter circuit. Both the bridges and the opto-couplers are given supply from the Regulated Power Supplies (RPS).

The outputs of both the simulation model and hardware circuit is shown in Fig. 11 and 12 respectively.

CONCLUSION

Hardware implementation of Cascaded H-bridge MLI topology using MATLAB-DSP interfacing has been proposed. Easy modularization and packaging of this inverter solve the problem of conventional multi-pulse inverter, diode clamped and flying capacitor inverter. Generation of triggering signals using MATLAB-DSP interfacing has been explained briefly. Use of GPIO block in SIMULINK model makes the triggering signal generation easier and more efficient. Since it has many input/output ports it allows to go for higher levels. This inverter is suitable for electric vehicle drives, utility interface for renewable energy sources, voltage regulation and phase shifting, reactive power control and compensation, high quality power supply etc.

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