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Implementation of Health Monitoring System using Mixed Environment

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Abstract

Background: Research shows that the health care cost per capita have grown 2.4 percent faster than the gross domestic product (GDP) since 1970. The aim of this paper is to present a useful model of wireless system that can combine both hardware and software environments and it can also integrate with other technologies or infrastructure at a low cost, which can be used for the patient monitoring system. **Methods:** The biomedical sensor which is attached to the patient, will read analog data. The recorded data will be converted digitally by using Analog to Digital Converter (ADC) and a FPGA transmitter will be used to send this data to Phase Shift Keying (PSK) transmitter. The modulated data will be received by PSK receiver and another FPGA receiver will be used to get the data back on the system. For behavioural modelling Verilog hardware descriptive language is used to provide a high level abstraction and language constructions. And the Simulink software is used to provide a high-level mathematical modelling condition for digital communication system which can be used for the verification and algorithm development.The important modules implemented for the transmitter and receiver FPGA are bus interfacing, compression and the data framing. **Findings:** A short range wireless health monitoring wireless system is modelled by using a mixed software and hardware simulation environment.At all the stages of the hardware and software designs, different types of languages like Verilog HDL codes and MATLAB used to verify the operation of the modules. The behavioural HDL designed of the FPGA transmitter and receiver will be interfaced with the RF Simulink models of PSK transmitter and receiver by using System Generator (Sysgen) tool that acts as the converter simulator. A realistic design model of health monitoring system is implemented which can be used for future hardware design. Compression and framing are the two main operations used in the transmitter side. Data compression is implemented by Run-Length Encoding method and for data framing high data link control protocol has been used. The unique features of this models simulation are low cost, less complexity, low power dissipation and efficient data transmission. Finally the FPGA based healthcare system allows us to change the design configurations or up gradation of the system based on the requirements. **Conclusion:** In this paper distributed simulation approach is used for designing the health monitoring system which allows checking the specification of design at all the stages. Simulation by HDL and Simulink mixed models in not the objective of this work, but to prove that realistic design is possible for future health care system design.

Keywords: Field Programmable Gate Array (FPGA), Hardware Description Language (HDL), Health Monitoring System, Phase Shift Keying (PSK).

1. Introduction

The rising home health care cost is pushing any Nation to the brink on a multiple fronts. The soaring cost of medical care infers less money in the pocket which forces hard choices about needed care, balancing food and rent etc. But on the other hand, the advancement in wireless technology and internet are developing rapidly which opened some new opportunity for the health service to reconsider the traditional model of health monitoring system for patient care[1]. Research shows that in the next 25 years, the global population which are over the age of 65 years will be increased by 88%[2].

A number of researchesare going on towards the new generation of the wireless technology application in the field of medical science which lead to an improvement in

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the quality of patient care and also in the cost reduction[3]. Wireless telemetry is one of the best technologies of the wireless in health care. A wireless health monitoring device will be attached to the patient and physicians can monitor the patient from anywhere across the town. But this type of wearable health monitoring equipment has some critical features like long battery life, lightweight and small dimensions[4]. It also requires that the device should continuously monitor during the normal activity of patient and protect the privacy of user. This type of equipment must produce a high-quality signal, be easy to remove or wear, should be robust and suitable for all the environment conditions and users[5]. To achieve the described demands, a model is presented in this work and its key features are low power consumption, low complexity and efficient data transmission.

2. Co-simulation using System Generator (Sysgen)

Distributed simulation approach is used for the mixed simulation which will allow checking the specification of design at all the stages[6]. At all the stages of the hardware and software designs, different types of languages can be used like Verilog HDL codes and MATLAB.

The behavioural HDL designed of the FPGA transmitter and receiver will be interfaced with the RF Simulink models of PSK transmitter and receiver by using System Generator (Sysgen)[7] tool that acts as the converter simulator. Sysgen is a tool which is developed from the Xilinx in a Simulink environment of MATLAB; it provides the capability of designing or modelling and implementing a high performance Digital Signal Processing (DSP) system blocks in a FPGA. It will provide a high speed HDL co-simulation interface mechanism to the ModelSim simulator[8-11]. Verilog HDL is used to design both behavioural and hardware synthesisable blocks and Simulink software is used to design all the system-level blocks for wireless transmitter and receiver.

3. System Specifications

The block diagram of the health monitoring system is shown in Figure1. The recorded data from the sensor contains analog data which will be converted into digital signal by using Analog to Digital Converter (ADC) and a FPGA transmitter will be used to send this data to Phase Shift Keying (PSK) transmitter.

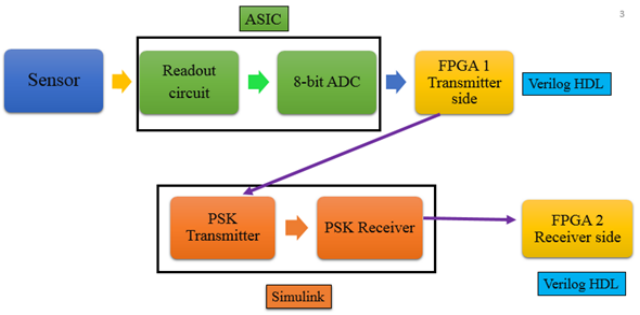

Figure 1. Block diagram of the system.

The modulated data will be received by the PSK receiver and another FPGA receiver will be used to get the data back the on the system. The Behavioural model of both the transmitter and the receiver blocks is implemented by using Simulink software.

4. FPGA Transmitter and Receiver

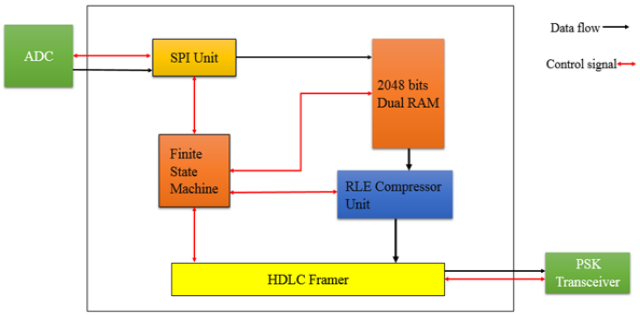

Figure 2. Building blocks of the transmitter FPGA.

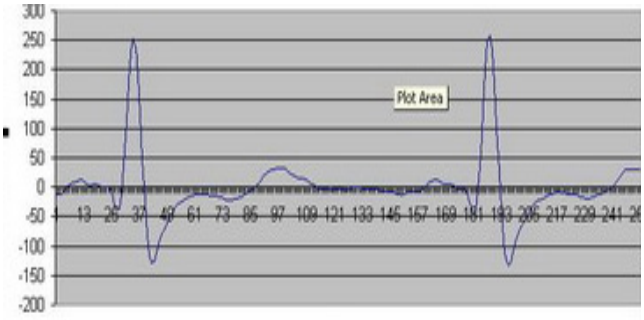

Figure 3. Sample of Electrocardiography (ECG) test.

The block diagram of FPGA transmitter is shown in Figure 2. The FPGA transmitter will process on digital data like interfacing, buffering, compression and framing and then it will pass through the PSK transmitter. All the

units of the FPGA transmitter are coded using Verilog hardware descriptive language which is simulated with Model Sim and implemented using Xilinx ISE 7.1. And the final implementation is done using Spartan-6 device. FPGA transmitter has submodules like- Serial peripheral Interface (SPI)[12], Run Length Encoding (RLE) compressor[13] and High Level Data Link Control (HDLC) protocol[14]. The sample of Electrocardiography (ECG) test is shown in Figure 3. The ADC will be used to convert this analog signal into digital form.

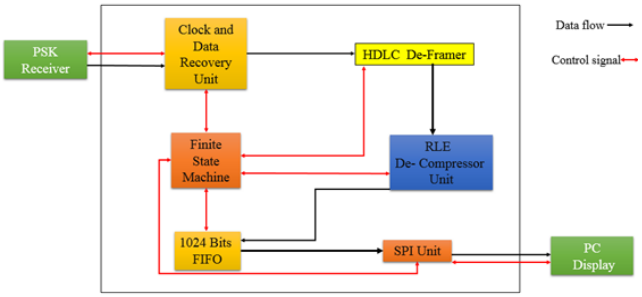

Figure 4. Building block of receiver FPGA.

The Finite State Machine (FSM) controller controlled the operation of system units and the flow of data through the system. At the receiver end, the system units of the FPGA is organised as shown in Figure 4. To extract the clock from the received bit stream, a data recovery unit is included into the receiver side of FPGA. To re-construct the original data byte sent by the transmitter side FPGA, HDLC de-framer and the RLE de-compressor blocks are designed.

4.1 SPI Modelling

Serial to Peripheral Interface (SPI) is defined as a hardware communications protocol which is developed by Motorola, a de facto standard and which is later adopted by other industry. The SPI bus is a synchronous data link type setup which has a master/slave interface and it can support up to the speed of 10 Mbps and it also operates at full duplex mode.

Serial Peripheral Interface (SPI) circuitry is shown in Figure 5. The slave device will respond by sending a data to the master device via the MISO line of master, when a master device transmits data to a slave device via the MOSI line. This results a full duplex transmission, which is controlled by the same clock signal and both the data bit out and data bit in synchronized by the clock. Thus, the byte received will be replaced by the transmitted bit. This reduces the need for a separate transmit-empty and a receiver- full status bits. A single status (SPIF) is enough to signify that the I/O operation has been completed.

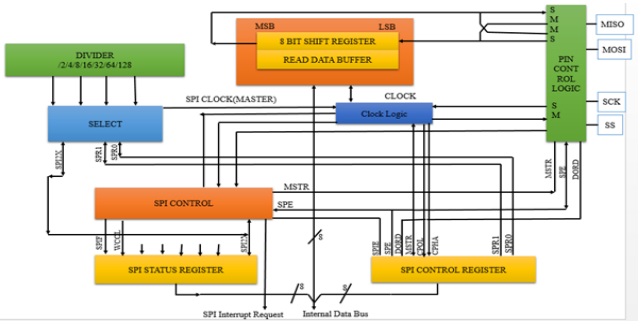

Figure 5. SPI Interface.

The SPI is double buffered on read, but not on write. The write will be unsuccessful, if write is performed during the data transfer but the transfer occurs uninterrupted. This condition will cause the write collision (WCOL) status bit in the SPSR to be set. After a data byte is shifted, the SPIF flag of the SPSR is set.

In the master mode, the SCK pin is an output. It idles high or low, depending on the CPOL bit in the SPCR, until data is written to the shift register, at which point eight clocks are generated to shift the eight bits of data and then SCK goes idle again. The main units of SPI are- clock divider unit, data out clock synchronizer, slave chip select, increment signal, SPI register unit and distributed block RAM. SPI unit is modelled using Verilog code which is synthesizable. Figure 6. shows the simulation output waveform of SPI protocol.

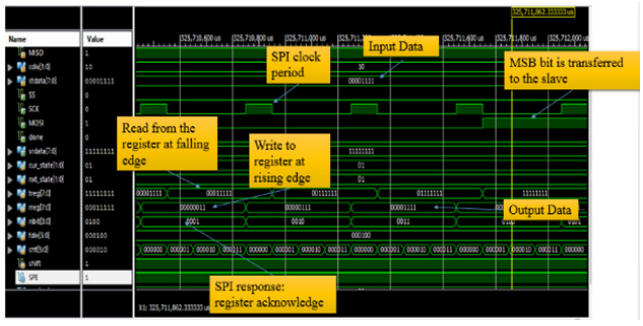

Figure 6. Simulation output waveform of SPI protocol.

4.2 RLE Compressor and De-compressor

Run length encoding is a very simple form of data compression technique in which run of data (sequence of same data value) is stored as a single data value and

count. SPI protocol is used to get the data from analog to digital convertor which contains sequence of ones and zeros. RLE compressor is used to compress the data which repeats.

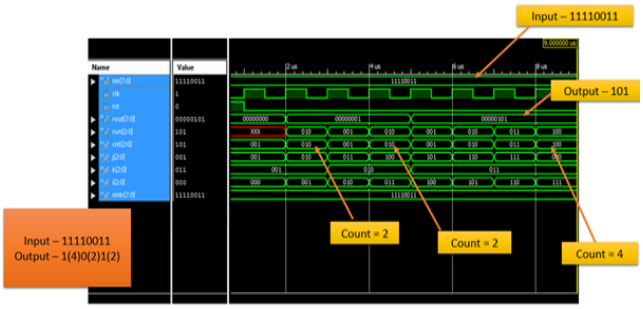

Figure 7. Simulation output waveform of RLE Compressor.

Figure 7 shows the simulation output waveform of run length encoding compressor which compresses the input data 11110011 to 101 with run count of 2, 2 &4. And Figure 8. shows the RLE Decompressor which decompresses the input 101 to 11110011.

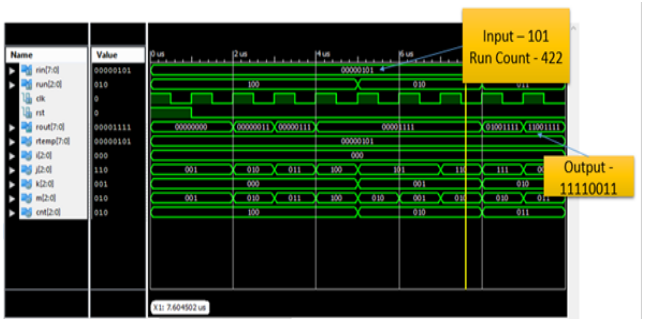

Figure 8. Simulation output waveform of RLE De-compressor.

4.3 HDLC Framer and De-framer

The main core of the FPGA transmitter is HDLC framer. HDLC which falls under the International Organization for Standardization (ISO)- ISO 4335 and ISO 3309 which is a bit oriented Protocol. It specifies a standardpacketization for serial links. It supports both full-duplex and half-duplex communication lines, multi-point network and point to point, non-switched and switched channels. For reliable delivery it supports a simple sliding-window. Most of the applications used the HDLC's unreliable delivery mode which provides retransmission at the higher levels.

HDLC reduces the possibility of errors because the control information bit is always be in the same position of frame and in the frame a specific bit pattern is used to represent the error bit and the data. Link Access Procedure-Balanced (LAP-B) and Synchronous Data Link SDLC;these two subsets are widely in used for the data link transfer.

4.3.1 HDLC Transmitter

HDLC transmitter consists of following main blocks

- Transmitter controller
- Transmit register
- Frame Check Sequence (FCS) generator
- Bit stuffer
- Flag/Abort generator
- Address insertion

The working function of each module is as follows

HDLC transmitter controller has the main responsibility of the generating and controlling all possible and required internal signals which is necessary and use by the all other different modules of the transmitter. Finite State Machine (FSM) approach will be used to implement the transmitter controller and the delay elements are implemented by using the D flip-flop. Transmit register module will capture the data at the rising edge of the each clock pulse.

Bit stuffer is responsible to distinguish between flag pattern and the original data of the same pattern.

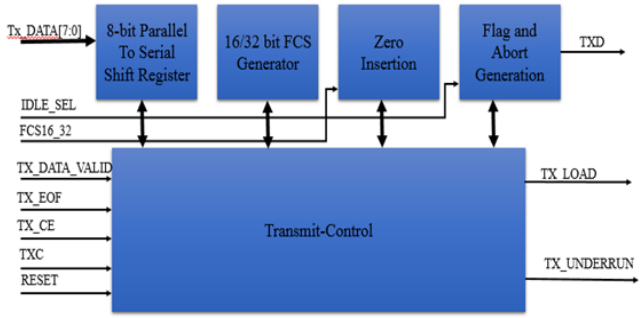

Figure 9. Block Diagram of HDLC Transmitter.

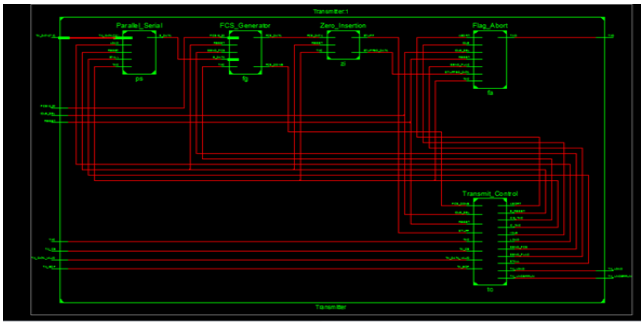

Figure 10. RTL view of HDLC Transmitter.

Flag and abort generator module is used to generate opening flag when the data is available to transmit. Figure 9 shows the block diagram of HDLC Transmitter with the different modules.

Figure 10 shows the RTL view of different units of HDLC transmitter and their connection, the coding is done using Verilog HDL which is synthesizable.

4.3.2 HDLC Receiver

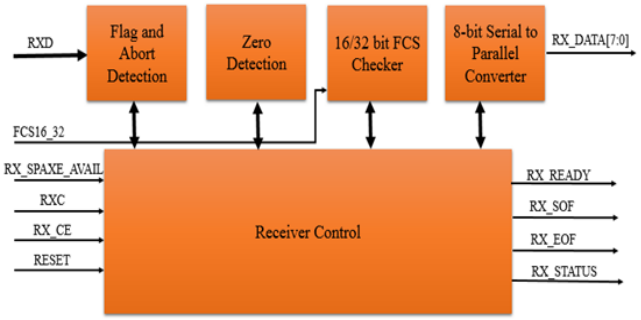

Figure 11. Block diagram of HDLC receiver.

Figure 11 shows the block diagram of HDLC receiver which has modules like- Flag and Abort detection, zero detection, FCS checker, serial to parallel converter and receiver controller.

The working function of each module is as follows

At each and every clock cycle flag and abort detector will compare the input and the register content with the flag and abort pattern. And it will report the detection through the FLAG and ABORT signal to the control unit. When five consecutive ones will be received, then a Zero signal will be asserted to inform the control unit that the incoming bit is an inserted zero. At every clock cycle, the FCS checker circuit will compare the value of scan register with the FCS generator and it will send the result to control unit. At every eight clock cycle the serial to parallel converter will load a byte data to the output and it has its own counter. HDLC receiver controller has the main responsibility of the generating and controlling all the possible and required internal signals which is necessary and use by the all other different modules of the receiver.

Figure12 shows the RTL view of different units of HDLC receiver and their connection, the coding is done using Verilog HDL which is synthesizable.

Figure 13 shows the simulation output waveform of HDLC transmitter and receiver. An input 01001000 is transmitted through the HDLC transmitter as a frame and the HDLC receiver de-framed the data at the receiver side. Targeted speed was 400 MHz.

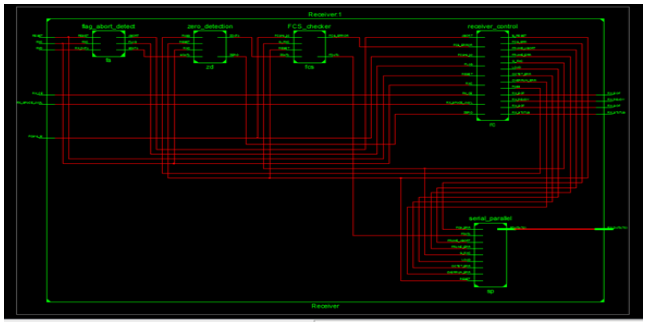

Figure 12. RTL view of HDLC Receiver.

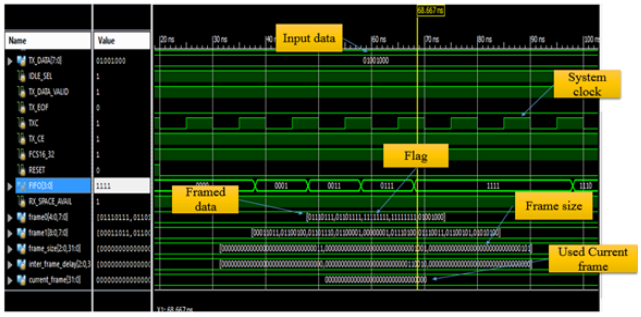

Figure 13. Simulink output waveform of HDLC protocol.

4.4 PSK Transmitter and Receiver Implementation using Simulink

In Phase Shift Keying (PSK) modulation technique[15] phase angle of the carrier wave is varied or modulated according to the message signal. If the message signal or received data is of logic '1' then the modulated signal will have a phase shift of 180 degree and if the message signal or received data is of logic '0' then the modulated signal will have a phase shift of 0 degree which is shown in equation (1) and equation (2) respectively.

In BPSK carrier is used to represent 0 or 1 as:

$s(t)=A\ \cos(2\pi f_c t + \pi)$ For binary '1' (1)

$s(t)=A\ \cos(2\pi f_c t + \pi)$ For binary '0' (2)

In this project PSK transmitter and receiver block diagram is implemented using both Simulink blocks and System Generator blocks which is used to generate the Verilog code.

Sysgenis a tool which is developed from the Xilinx in a Simulink environment of MATLAB; it provides the capability of designing or modelling and implementing a high performance Digital Signal Processing (DSP) system

blocks in a FPGA.It will provide a high speed HDL co-simulation interface mechanism to the ModelSim simulator.

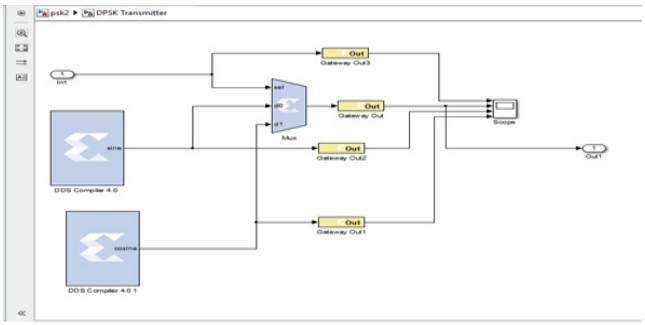

Figure 14. Simulink block diagram of PSK transmitter using system generator.

Figure 14 shows the block diagram of PSK transmitter. If the message signal is of logic '1' then the modulated signal will have a phase shift of 180 degree and if the message signal is of logic '0' then the modulated signal will have a phase shift of 0 degree which can be implemented by using a multiplexer.

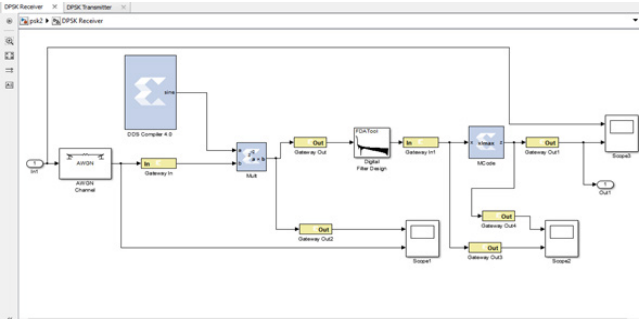

Figure 15. Simulink block diagram of PSK receiver.

Figure 15 shows the block diagram of PSK receiver. The modulated signal is passed through the channel which is having Additive White Gaussian Noise (AWGN). The AWGN is a basic noise model used in the information theory to show the effect of random processes which occurs in nature.

The modulated signal is multiplied with the carrier wave and passed through the low pass filter to get back the desired message signal. The output waveform of PSK transmitter is shown in Figure 16.

Figure 17 shows the output waveform of PSK receiver of each stage and the final waveform of message signal is also shown.

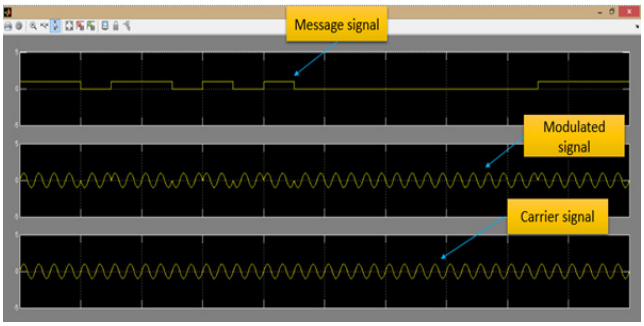

Figure 16. Output waveform of PSK Transmitter.

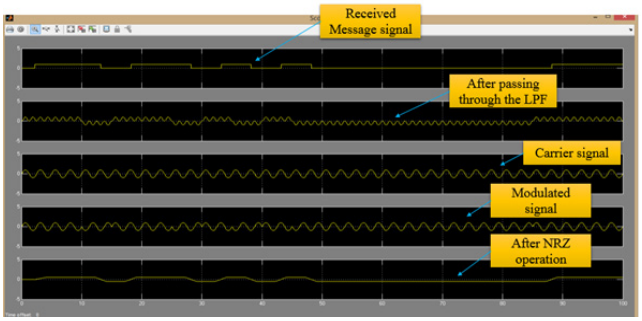

Figure 17. Output waveform of PSK Receiver.

5. Conclusion

A short range health monitoring wireless system is modelled in this paper by using a mixed software and hardware simulation environment. For behavioural modelling Verilog hardware descriptive language is used to provide a high level abstraction and language constructions. And the Simulink software is used to provide a high-level mathematical modelling condition for digital communication system which can be used for the verification and algorithm development.

The important modules implemented for the transmitter and receiver FPGA are bus interfacing, compression and the data framing. SPI protocol is used for the bus interfacing. RLE compression technique is used to compress the data bytes which are stored into the memory with an optimal number of run and states. The HDLC protocol has been used for framing the data and it also provides a very useful technique that is a mechanism to handle the error to the receiver. The FPGA modules have been implemented and verified. And all units were synthesizable. A PSK transmitter and receiver module which can be used for the short range wireless communication system is also implemented.

A realistic design model of health monitoring system is implemented which can be used for future hardware design.

6. Acknowledgement

No study can be done in a single day by a single person but it is a result of long experimentation and observation where the required environment consisting of many people play a vital role in initializing and completing a work.

7. References

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