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Investigation of f_t and f_{max} in Si and $Si_{1-x}Ge_x$ based single and dual material double-gate Tunnel FETs for RF applications

M Pown and B Lakshmi

School of Electronics Engineering, VIT University, Vandalur-Kelambakkam Road, Chennai, Tamil Nadu 600127, India

E-mail: pown.marimuthu@vit.ac.in

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Abstract

This study optimizes $Si_{1-x}Ge_x$ based double gate tunnel field effect transistor (TFET) for their high ON current (I_{on}) and lesser sub-threshold swing and compares Si and $Si_{1-x}Ge_x$ based single material double gate (SMDG) and dual material double gate (DMDG) TFETs. This study also measures the two RF performance metrics, unity gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) by varying the structural parameters, gate length, gate oxide thickness, channel thickness and underlap. Compared to single material gate devices, dual material gate devices give higher I_{on} without compromising the leakage current for both Si and $Si_{1-x}Ge_x$ based TFETs. $Si_{1-x}Ge_x$ based TFETs offers higher f_t and f_{max} compared to that of Si TFETs for all the structural parameter variations considered in this study. DMDG TFETs exhibit higher f_t with respect to SMDG TFETs. SMDG TFETs offers more f_{max} compared to DMDG TFETs due to the smaller values of output conductance.

Keywords: Tunnel FET, BTB tunneling, dual material gate, unity gain cut-off frequency, maximum oscillation frequency
Classification numbers: 2.00, 2.07, 3.02, 4.00, 4.12, 5.01, 6.01

1. Introduction

To meet the scaling demands, many novel devices have been reported with different working principles. Tunnel field effect transistors (TFETs) is one of the promising devices to replace MOSFET because of its sub-threshold swing (SS) limit of 60 mV dec^{-1}, low OFF-state leakage current and low threshold voltage [1–3]. TFET is basically a reverse biased P–I–N junction diode which works on the principle of quantum mechanical band-to-band tunneling (BTBT) mechanism.

Double gate (DG) TFETs shows improved characteristics in terms of higher drive current and less threshold voltage roll-off compared to single gate TFET [4–6]. A dual material double gate (DMDG) TFET was proposed by using two different gate electrode work functions to improve the overall performance of the device [7, 8]. Since silicon (Si) based DG TFETs suffers from lesser ON-state current, this can be further improved by using lower band gap material like silicon–germanium (SiGe) for the entire region [9], or in the source channel region [10], or in the source only [11–13]. By optimizing mole fraction (x) presented in $Si_{1-x}Ge_x$, TFET exhibited higher performance with low SS [14, 15].

In this paper the optimization of $Si_{1-x}Ge_x$ based DG TFET is performed to obtain a higher ON state current with lesser SS. To improve the RF metrics, unity gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}), the structural parameters are varied for Si and $Si_{1-x}Ge_x$ based single material double gate (SMDG) and DMDG TFETs. Section 2 describes the device structures of Si and $Si_{1-x}Ge_x$

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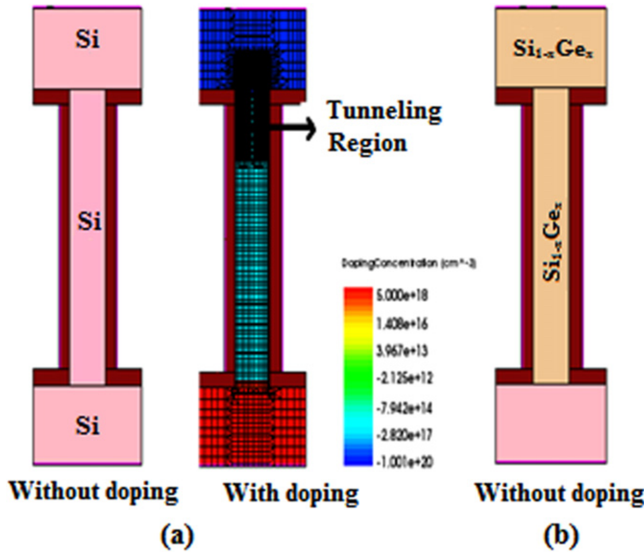

Figure 1. Simulated structure of SMDG TFET: (a) Si based SMDG TFET (with and without doping) and (b) $Si_{1-x}Ge_x$ based SMDG TFET (doping not shown).

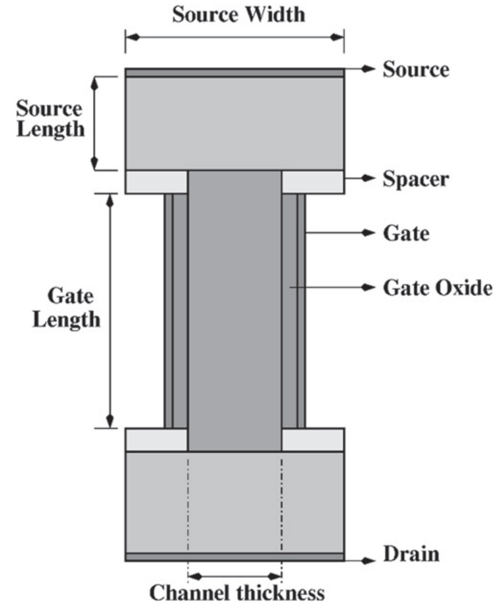

Figure 2. Schematic structure of DG TFET.

DG TFET along with the simulation methodology. The results are discussed in section 3. Finally section 4 provides the conclusion.

2. Device structure and simulation methodology

TCAD simulator from Synopsys is used to perform the simulations [16]. Figure 1 depicts the 2D structure of Si and $Si_{1-x}Ge_x$ based n-type SMDG TFET. The schematic diagram of DG TFET is shown in figure 2 which shows various parameters of the device. The device has the gate length (L_g) of 50 nm, a channel thickness (T_{ch}) of 10 nm, underlap (L_{un}) of 3 nm and gate oxide thickness (T_{ox}) of 3 nm. The source is doped with p^+ type material while the drain is doped with n^+ type material. The drain doping ($N_d = 5 \times 10^{18}\,cm^{-3}$) is lower than source doping ($N_s = 1 \times 10^{20}\,cm^{-3}$) to suppress the ambipolar effect [17]. The channel has an intrinsic concentration of $1 \times 10^{17}\,cm^{-3}$. The gate electrode work function for SMDG TFET is 4.5 eV.

The device simulator includes appropriate models for doping dependence mobility, effects of high and normal electric fields on mobility and velocity saturation. A non-local Hurkx BTBT model is used along with Fermi–Dirac statistics and Shockley–Read–Hall recombination model. Supply voltage used in this study is 1 V and the gate voltage is 1.8 V. To operate the device, the source is grounded and the positive voltage is applied at the drain. The gate voltage (V_g) controls the tunneling by modulating the carrier concentration in the channel region. The SS of the device is defined as the change in gate voltage in order to create one decade increase in the output current. It can be expressed as

$$SS(\mathrm{mV\ dec^{-1}}) = \frac{\mathrm{d}V_g}{\mathrm{d}(\log I_d)}. \qquad (1)$$

The TFET ON currents are based on BTBT mechanism. The BTB tunneling probability can be analytically calculated using Wentzel–Kramers–Brillouin (WKB) approximation method. The result of WKB approximation derived in [18] can be described by [19]

$$I \propto \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(\Delta\Phi + E_g)}\right)\Delta\Phi, \qquad (2)$$

where m^* is the effective carrier mass, E_g is the bandgap, e is the electron charge, $\Delta\Phi$ is the energy range over which the tunneling can take place, $\hbar$ is the Planck's constant and Λ is the spatial extent of the transition at source-channel interface. Λ can be defined by

$$\Lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}, \qquad (3)$$

where t_{ox}, t_{Si}, ε_{ox}, and ε_{Si} are the oxide and silicon-film thicknesses and dielectric constants, respectively. Equation (1) shows that the tunneling current can be increased by increasing electric field along the channel (proportional to $(\Delta\Phi + E_g)/\Lambda$). One of the approaches to improve the performance of the device is to decrease the bandgap of the material. The amount of Ge content (x) for the $Si_{1-x}Ge_x$ based DG TFETs improves the ON state current [14, 20]. Figure 3 represents the I_d–V_g characteristics of $Si_{1-x}Ge_x$ based SMDG TFET with Ge mole fraction (x) which is varied from 0 to 0.4. It is observed that the maximum I_{on} of 23 μA and lesser SS of 32 mV decade^{-1} are obtained for $x = 0.4$. This is because of the lower band gap energy for germanium over silicon. Since

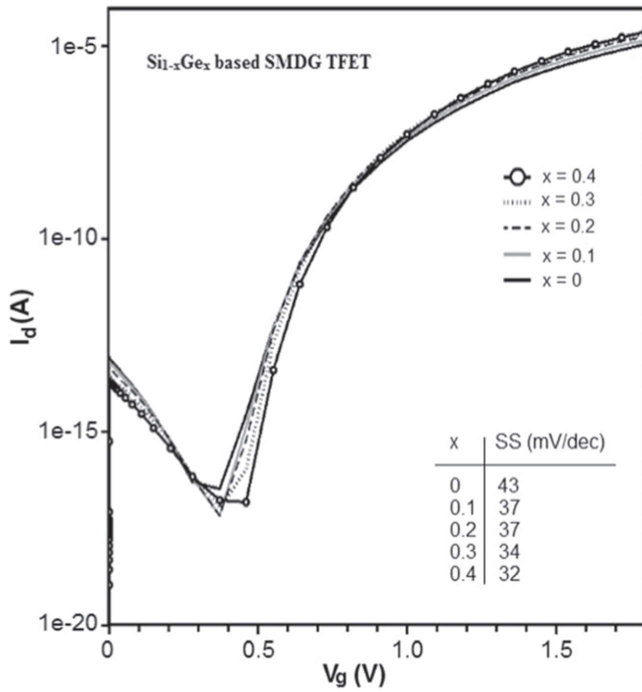

Figure 3. I_d–V_g characteristics of $Si_{1-x}Ge_x$ based SMDG TFET for various mole fractions ranging from $x = 0$ to $x = 0.4$.

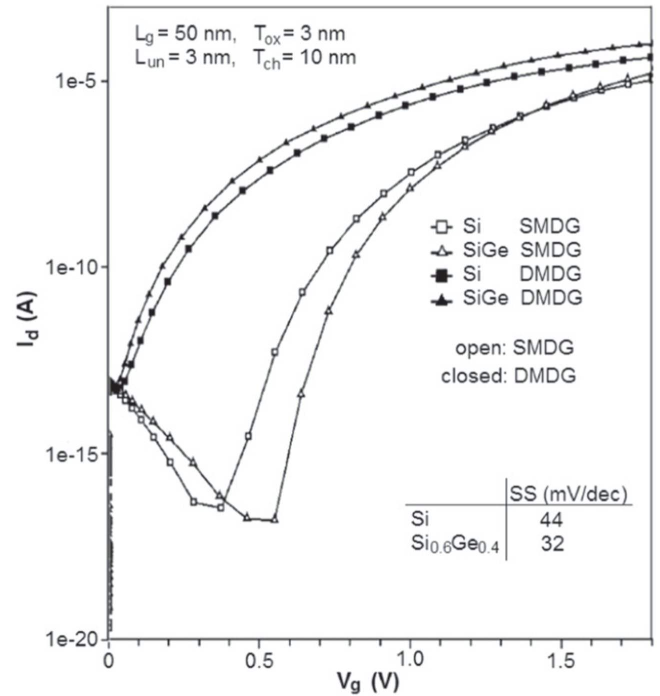

Figure 5. I_d–V_g characteristics of Si and $Si_{0.6}Ge_{0.4}$ based SMDG and DMDG TFETs with $I_{off} = 82.7$ fA.

lesser SS is obtained for a higher I_{on}, mole fraction of $x = 0.4$ is used for SiGe devices.

Figure 4 shows the energy band diagram for Si and $Si_{0.6}Ge_{0.4}$ based DG TFETs. In the OFF-state ($V_g = 0$ V), the tunneling barrier width is extremely large enough to give a very small leakage current. When the gate voltage is increased ($V_g = 1.8$ V), the conduction bands in the intrinsic region are pulled downwards and the tunneling barrier width is reduced allowing electrons move from the source to the channel region [9–11].

The DMDG TFETs have similar dimensions of SMDG TFETs. To get a fair comparison between Si and $Si_{0.6}Ge_{0.4}$ based SMDG and DMDG TFETs, leakage current (I_{off}) of all of these devices are matched to 82.7 fA. I_d–V_g characteristics of SMDG and DMDG of Si and $Si_{0.6}Ge_{0.4}$ based TFETs are extracted and plotted in figure 5. It can be seen from the graph that, compared to SMDG, DMDG offers more I_{on} for both Si and $Si_{0.6}Ge_{0.4}$ based TFETs. This is due to the higher tunneling probability near the source end which enhances I_{on} significantly [21–23]. Because of the property of double material gate and also due to the tunneling phenomenon, DMDG TFET shows the lower threshold voltage than SMDG TFET [20].

Figure 6 shows the plot of electron barrier tunneling with respect to distance along the channel for Si and $Si_{0.6}Ge_{0.4}$ based SMDG and DMDG TFETs. The physical significance

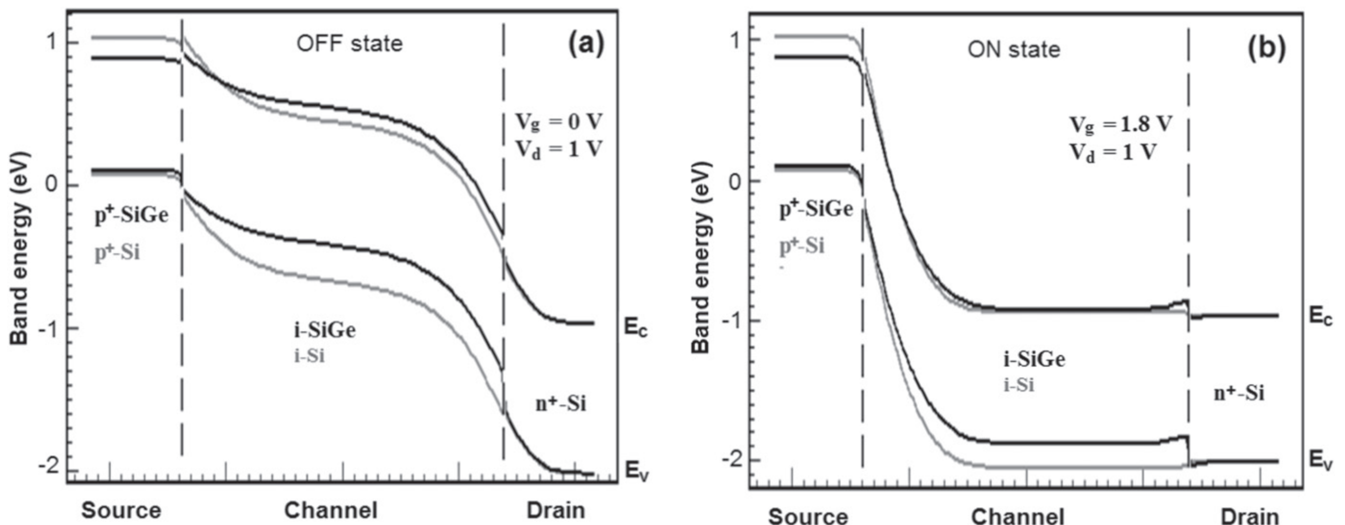

Figure 4. Energy band diagrams for Si and $Si_{0.6}Ge_{0.4}$ based DGTFETs: (a) OFF state and (b) ON state.

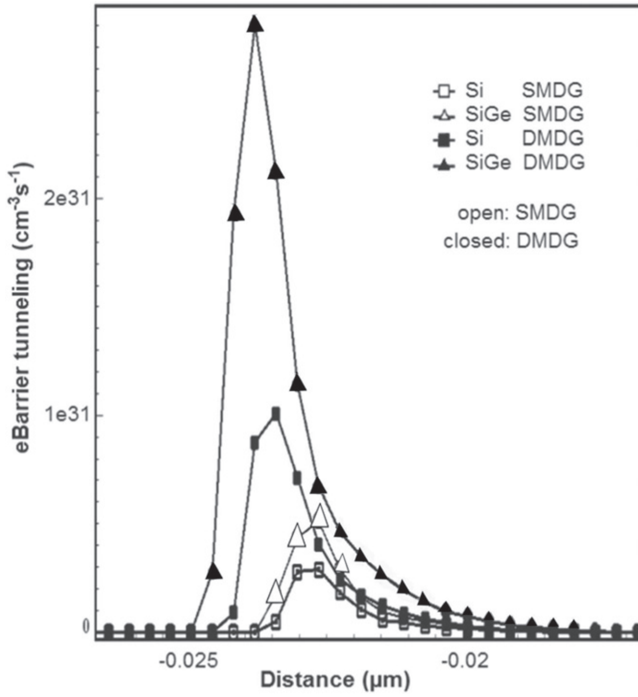

Figure 6. eBarrier tunneling for Si and $Si_{0.6}Ge_{0.4}$ based SMDG and DMDG TFETs.

of this plot represents the rate at which electrons are generated due to tunneling. It can be observed that DMDG TFETs show higher tunneling rate of electrons compared to that of SMDG. Comparatively $Si_{0.6}Ge_{0.4}$ offers more electron tunneling over Si based TFETs.

For the devices mentioned above, the structural parameters considered here are the gate length, gate oxide thickness, channel thickness and underlap. The important RF parameters, f_t and f_{max} are extracted by performing AC simulations. f_t is defined as the frequency where current gain becomes unity and in terms of device parameters it can be expressed as

$$f_t = \frac{g_m}{2\pi C_{gg}}, \quad (4)$$

where g_m is the transconductance and C_{gg} is the combination of gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}). f_{max} is defined as the frequency at which power gain drops to unity and can be expressed as

$$f_{max} = \frac{f_t}{\sqrt{4R_g(g_{ds} + 2\pi f_t C_{gd})}}, \quad (5)$$

where R_g is the gate resistance and g_{ds} is the output conductance.

3. Results and discussion

As mentioned earlier, the gate length, gate oxide thickness, channel thickness and underlap are varied as shown in table 1. The RF parameters, f_t and f_{max} are extracted for all these devices.

Table 1. Range of values for the structural parameters considered.

Parameters	Range of values (nm)
Gate length (L_g)	40–60
Gate oxide thickness (T_{ox})	1–5
Channel thickness (T_{ch})	5–15
Underlap (L_{un})	1–10

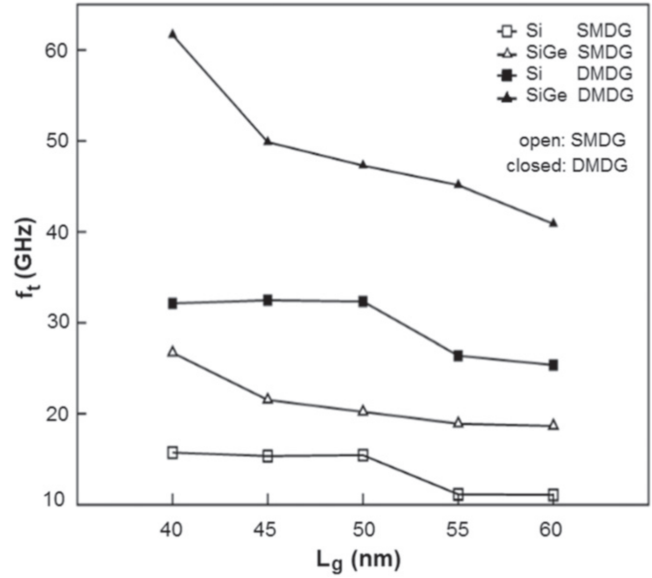

Figure 7. The unity gain cut-off frequency f_t versus gate length L_g.

3.1. Variation in gate length

Figure 7 shows the variations of f_t versus L_g. It can be observed that f_t decreases with increasing gate length. Though f_t is determined by both g_m and C_{gg}, f_t decreases because of g_m degradation for higher gate lengths [24]. Since $Si_{0.6}Ge_{0.4}$ based TFETs offers more g_m comparatively, they exhibits higher cut-off frequencies.

Figure 8 shows the variations of f_{max} versus L_g. Compared to f_t, f_{max} shows higher value because of the inversion layer formed in the drain region and less channel resistance [25]. It can also be observed that f_{max} increases as gate length decreases for both Si and $Si_{0.6}Ge_{0.4}$ TFETs. This can be attributed to the reduced gate resistance. DMDG TFETs shows lesser f_{max} compared to SMDG TFETs due to the larger values of g_{ds} for DMDG TFETs.

3.2. Variation in oxide thickness

Figure 9 shows the variations of f_t versus T_{ox}. It can be observed that f_t increases with decreasing gate oxide thickness for both Si and $Si_{0.6}Ge_{0.4}$ TFETs. This can be attributed by the improvement in the gate electrostatic integrity over the channel due to the screening of the electric field at the source side [26]. $Si_{0.6}Ge_{0.4}$ TFETs exhibits higher f_t compared to Si TFETs since the former has more g_m.

Figure 10 shows the variations of f_{max} versus T_{ox}. It can be inferred from the plot that as T_{ox} decreases, f_{max} increases

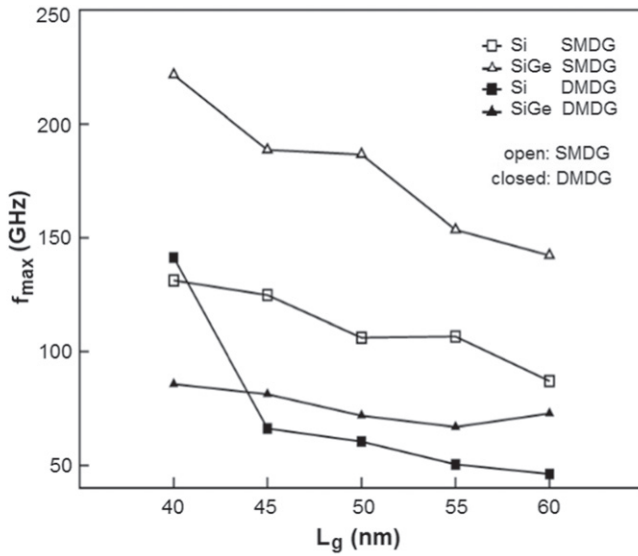

Figure 8. The maximum oscillation frequency f_{max} versus gate length L_g.

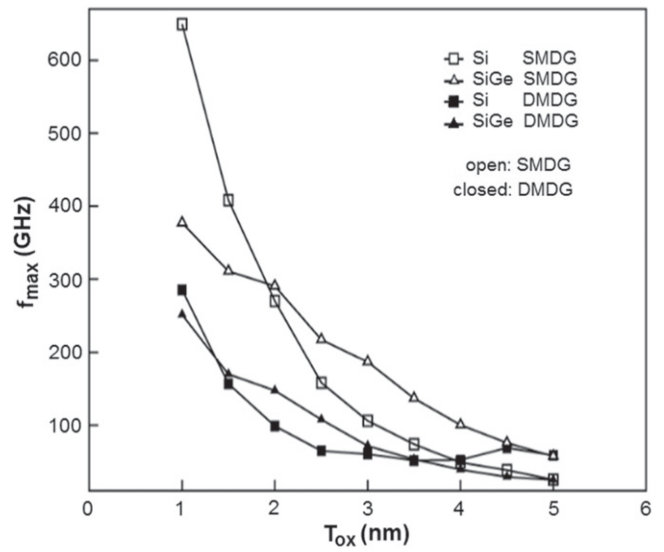

Figure 10. The maximum oscillation frequency f_{max} versus gate oxide thickness T_{ox}.

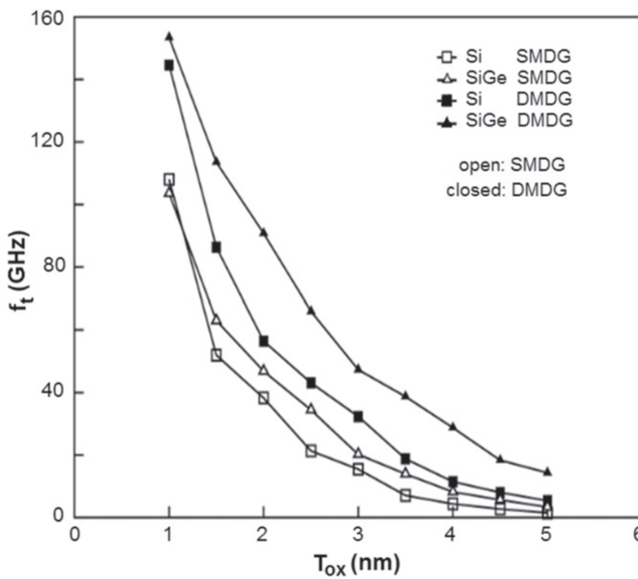

Figure 9. The unity gain cut-off frequency f_t versus gate oxide thickness T_{ox}.

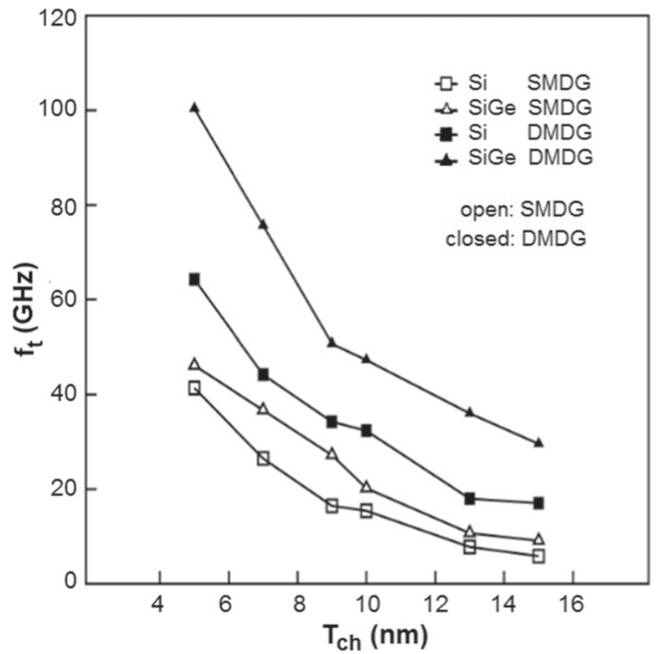

Figure 11. The unity gain cut-off frequency f_t versus channel thickness T_{ch}.

due to the smaller gate resistance near the source side and the charge carriers are confined only near the drain region [26].

3.3. Variation in channel thickness

Figure 11 shows the variations of f_t versus T_{ch}. It can be observed that f_t increases with decreasing channel thickness. With the scaling of the channel thickness, screening of gate fringing fields dominates, and reduces gate capacitance which ultimately improves f_t [26]. As discussed already, $Si_{0.6}Ge_{0.4}$ TFETs exhibits higher f_t compared to Si TFETs.

Figure 12 shows the variations of f_{max} versus T_{ch}. The increase in f_{max} can be reasoned out as the reduction in g_{ds} for lesser values of channel thickness. This holds the same for both Si and $Si_{0.6}Ge_{0.4}$ TFETs.

3.4. Variation in underlap

Figure 13 depicts the plot between f_t and L_{un} for Si and $Si_{0.6}Ge_{0.4}$ SMDG and DMDG TFETs. For all the devices, f_t shows a decreased value for the increase in L_{un}. This may be due to the decreased g_m values for larger values of L_{un} [27, 28].

Figure 14 shows the variations of f_{max} versus L_{un}. The plot depicts the decreased values of f_{max} for higher values of underlap. The effective channel length is wider for the increased underlap and the inversion layer is formed close to the drain region. This increases g_{ds} which ultimately reduces f_{max}. This effect is seen for both Si and $Si_{0.6}Ge_{0.4}$ TFETs.

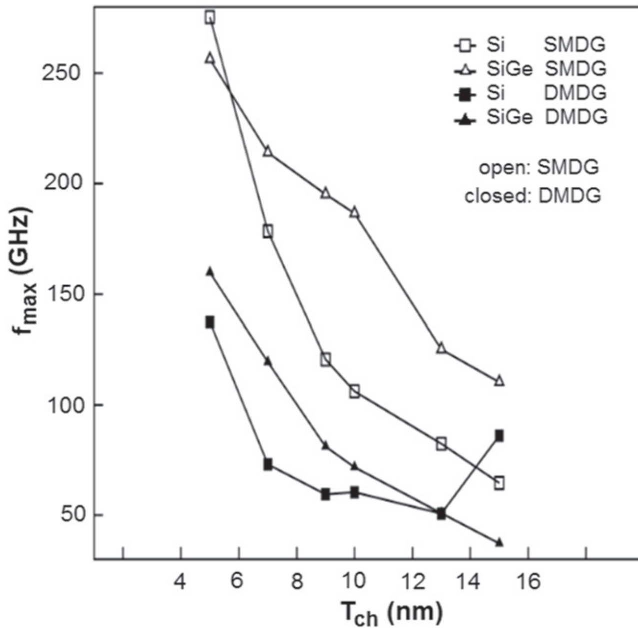

Figure 12. The maximum oscillation frequency f_{max} versus channel thickness T_{ch}.

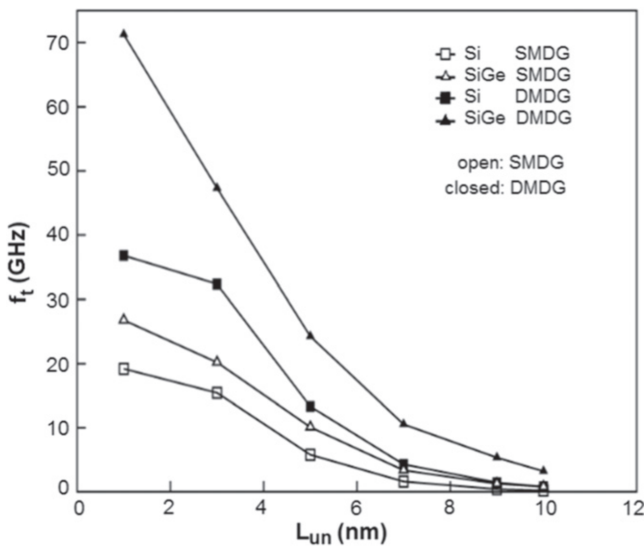

Figure 13. The unity gain cut-off frequency f_t versus underlap L_{un}.

4. Conclusion

To enhance ON current for a reduced SS in TFETs, $Si_{1-x}Ge_x$ is optimized and then compared with Si based SMDG and DMDG devices. Four structural parameters—gate length, gate oxide thickness, channel thickness and underlap are considered to study the impact of f_t and f_{max} in Si and $Si_{0.6}Ge_{0.4}$ SMDG and DMDG TFETs. It can be observed that $Si_{0.6}Ge_{0.4}$ offers more f_t and f_{max} with respect to the variation in the structural parameters. Higher value of f_{max} can be attributed to inversion layer formed closely to the drain more than to the source unlike conventional MOSFETs. Hence SiGe TFETs

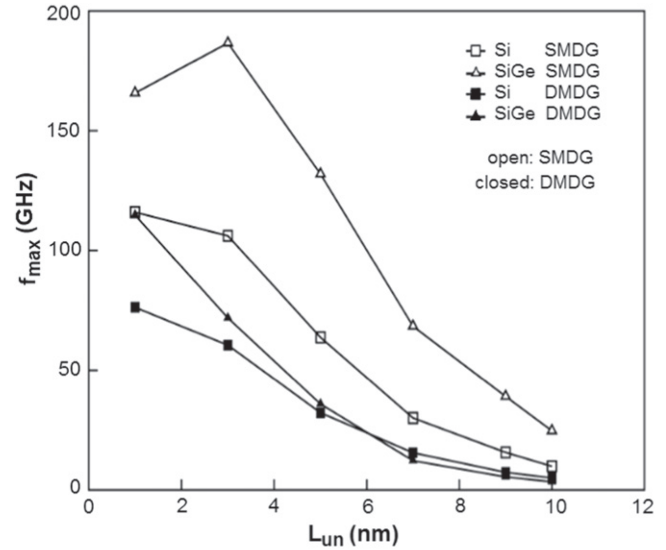

Figure 14. The maximum oscillation frequency f_{max} versus underlap L_{un}.

seems to be promising candidate to replace Si TFETs for the future analog/RF applications.

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