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Low Noise Low Power CMOS Telescopic-OTA for Bio-Medical Applications

Bellamkonda Saidulu *, Arun Manoharan * and Kumaravel Sundaram

School of Electronics Engineering, VIT University, India; kumaravel.s@vit.ac.in
* Correspondence: bellamkonda.saidulu@gmail.com (B.S.); arunm@vit.ac.in (A.M.)

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Abstract: The preamplifier block is crucial in bio-medical signal processing. The power intensive Operational Transconductance Amplifier (OTA) is considered, and the performance of preamplifier is studied. A low noise and low power telescopic OTA is proposed in this work. To reduce the noise contribution in the active load transistors, source degeneration technique is incorporated in the current stealing branch of the OTA. The OTA design optimization is achieved by g_m/I_d methodology, which helps to determine the device geometrical parameters (W/L ratio). The proposed design was implemented in CMOS 90 nm with bias current and supply voltage of 1.6 μA and 1.2 V, respectively. The post layout simulation results of the proposed amplifier gave a gain of 62 dB with phase margin 57°, CMRR 78 dB, input referred noise 3.2 μVrms, Noise Efficiency Factor (NEF) 1.86 and power consumption of 1.92 μW.

Keywords: low noise preamplifier; telescopic OTA; source degeneration; current stealing; CMOS 90 nm; g_m/I_d methodology; subthreshold

1. Introduction

The recent advancement in health monitoring system with NEMS/MEMS technology has opened up the opportunity for integrating a greater number of sensors on a chip (high density) which in its turn allows for better disease diagnosis and treatment of patients. Figure 1 [1] shows the physiological signal's frequency and amplitude distribution in the range of 1 μV–10 mV and 0.5 Hz–10 KHz. This work will focuses on the frequency range of Epilepsy seizure diagnoses using EEG signal which is limited to 100 Hz. Some of the bio-signal recording systems are constructed such that they are implantable, and are placed beneath the skin to record for a fairly long period (7–12 weeks) to diagnose the disorders. These recording systems demand low power consumption, small size [2] and low noise for faithful signal detection.

The preamplifier is shown in Figure 2 [1]. It consists of an MOS Depletion Pseudo Resistor (MDPR), coupling capacitor (C_1), feed back capacitor (C_f) and load capacitor (C_L). MDPR is used for the rejection of DC offset at the electrode-tissue interface, which emulates high resistance values (Tera ohm) with smaller swing. The midband gain of the preamplifier is decided by the ratio of capacitors (C_f/C_1) and the bandwidth approximately to $g_{m,OTA}/A_m * C_L$. To design preamplifier, OTA is the most important circuit for better performance and also for a power-intensive circuit. The challenging issue is to design a preamplifier with low power, low noise and optimized area. The amplifier should be stable and should collect undistorted signal by rejecting large DC offset voltage due to the interface between the electrode and the tissue [3]. Due to bio-compatibility, the existing circuitry still requires improvement in terms of: area, noise level, heat and power dissipation [3]. For instance, the power consuming area of 80 mW/cm^2, produces a heat flux which may cause necrosis in muscle tissue [4].

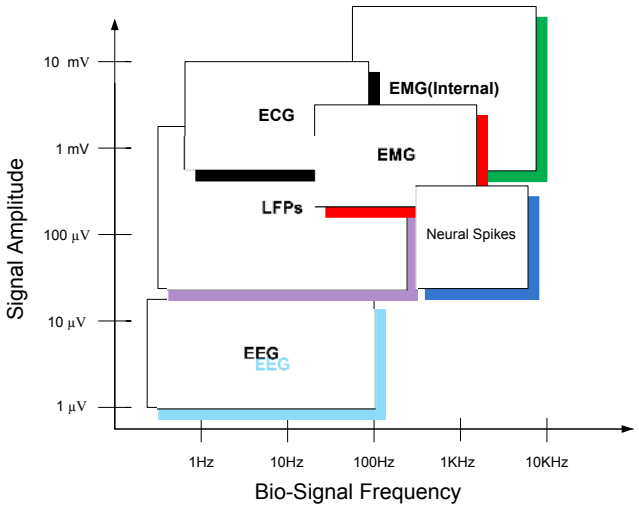

Figure 1. Physiological signal's frequency and amplitude distribution.

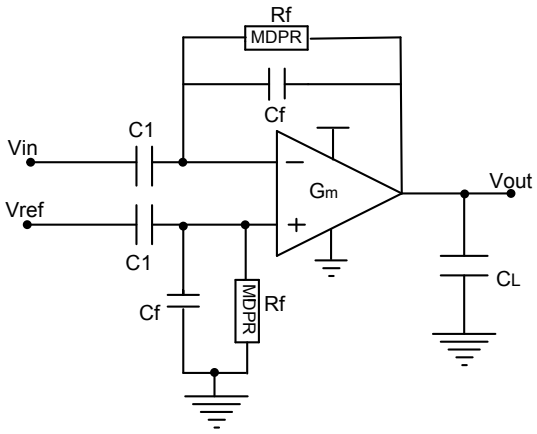

Figure 2. Schematic of the Preamplifier.

Chaturvedi and Amrutur [2] demonstrated the advantages of open loop over closed loop neural amplifier architectures which are based on the requirement of low frequency signal applications. In their work, they had the benefit of area and power consumption. These open loop architectures have drawbacks in terms of inaccuracy in gain and large distortion. Harrison and Charles [1] achieved better noise level with the cost of power consumption and high bias current. Yang and Holleman [5] demonstrated dual stages, single ended input stage and differential second stage, and focused on supply noise cancellation which achieved better NEF. Nemievosky et al. [6] explained the input referred noise and power spectral density model in saturation and subthreshold regions. They proposed an optimization method to reduce the noise by changing the aspect ratio. Study of the related works reveals the importance of low noise and low power preamplifier design with optimized device geometry. The advantages of single stage telescopic OTA [1] are high gain and area efficiency. Therefore, we propose telescopic OTA with source degeneration in the current stealing branch in this work. Optimized device geometry has been selected based on the g_m/I_D method shown in Figure 3. Post-layout simulation of the proposed OTA design is carried out with and without source degeneration in the current stealing branch and the results are compared with conventional OTA. This proposed design achieves better noise level and better power consumption.

This paper is organized as follows. Section 2 demonstrates the g_m/I_D methodology for the proposed OTA. Section 3 reports the proposed OTA with source degeneration in the current stealing branch. Section 4 discuss the obtained post-layout simulation results.

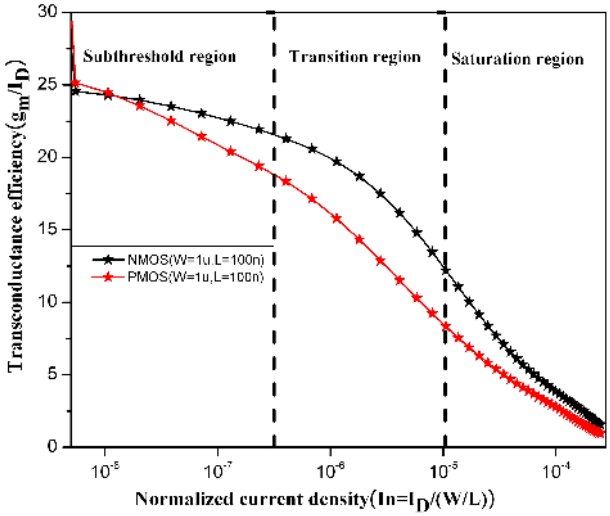

Figure 3. g_m/I_D vs. Normalized current density (In) = (I_D/W/L).

2. g_m/I_D Methodology

The g_m/I_D is a design parameter that reveals the region of operation and aspect ratio of all MOS transistors in a circuit. This g_m/I_D parameter is obtained by characterization of NMOS and PMOS transistors through simulation for a particular technology [7]. Figure 3 shows the simulation of g_m/I_D vs. I_n (normalized current density) plots for both NMOS and PMOS transistors with (W = 10 × L_{min}), (L = L_{min}) in CMOS 90 nm technology.

The design methodology is followed as presented in Figure 4.

1. Akbari et al. demonstrated [8,9] g_m/I_D design flow. Selection of the high g_m/I_D value from the Figure 3 ensures lower V_{gs}, larger W and smaller L without reduction in current. This keeps the input transistors $(M_{1,2})$ operating in weak inversion and leads to minimizing the input-referred noise.
2. The selection of a low g_m/I_D value from Figure 3 for reducing the input referred noise, ensures high V_{gs}, lower W and larger L, without current reduction. This means that the load and stealing transistors $(M_{9,10}, M_{7,8,11,12})$ operate in strong inversion.
3. For cascode transistors $(M_{3,4,5,6})$, a moderate value of g_m/I_D is selected with respect to the curves to ensure operates in moderate inversion. With allowable cost of voltage swing, the cascode transistors are introduced to improve the gain of preamplifier without further noise inclusion by shielding property [10].

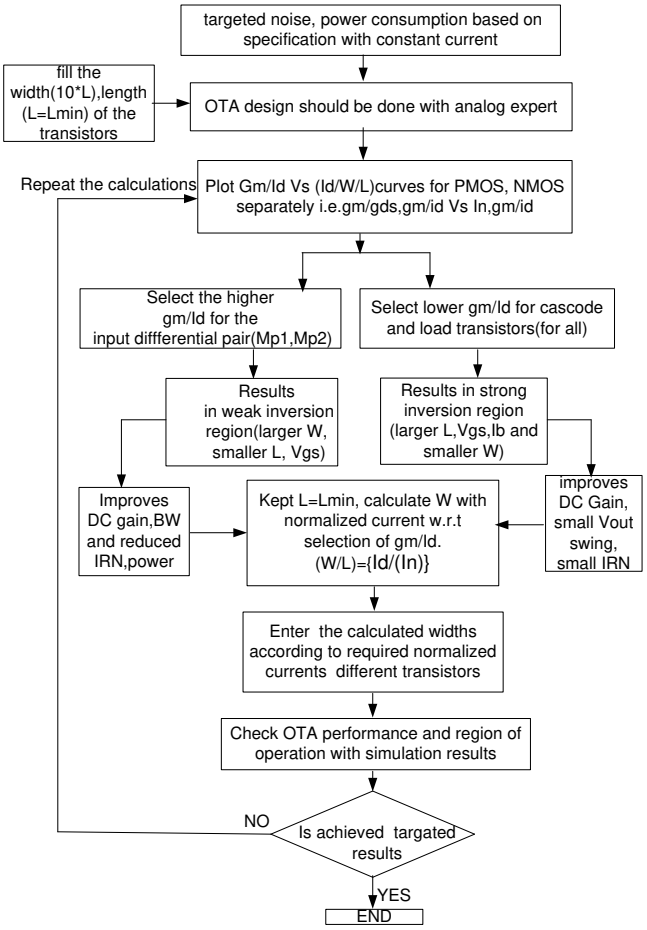

Figure 4. Design flow of g_m/I_D methodology.

3. Design of Telescopic OTA

Figure 5 shows the schematic of proposed telescopic OTA with source degeneration in the current stealing branch. In the proposed OTA, M0 is a bias transistor, and M1 and M2 are input differential transistors. M3, M4, M5 and M6 are cascode transistors. M7 and M8 are load transistors, M9, M10, M11 and M12 are current stealing transistors. R is the source degenerative resistor in each branch and bias current (I_b) is 1.6 μA, I_{steal} is 710 nA, R = 300 kΩ. The local feedback provided by the degeneration resistor circulates part of the noise current in MOS transistor, without passing it to the output [11].

Bio-amplifier overall performance majorly depends on optimized architecture, proper biasing and sizing of OTA. The design parameters of OTA such as gain, phase margin, UGB, power consumption, noise, slew rate and CMRR can be optimized by proper selection of the Vgs, aspect ratio (W/L) and bias current. Factors influencing the overall performance of the preamplifier are: optimized architecture, proper biasing and sizing of OTA. For low noise and low power design, all transistors are operated in different regions i.e., weak inversion, moderate inversion and strong inversion based on their aspect ratio (W/L). The standard biasing circuits [12] are used to bias the OTA.

This paper proposed a noise reduction technique by introducing source degeneration in the current stealing branch [2,11], which has more impact on noise reduction. Current stealing is a gain enhancement technique. OTA's output impedance is inversely proportional to the drain current and transconductance is directly proportional to the square root of I_D. From these relations, gain is inversely proportional to the drain current. The current stealing technique separates the bias currents of input and load transistors to alter the gain and drain currents [13].

Decrement of the current in active load transistors reduces the overall noise and improves the gain. A PMOS input telescopic amplifier with current stealing technique (g_m-g_m structure) is presented in [1]. In this work, the circuit with all PMOS transistors with one side cascode offers less gain.

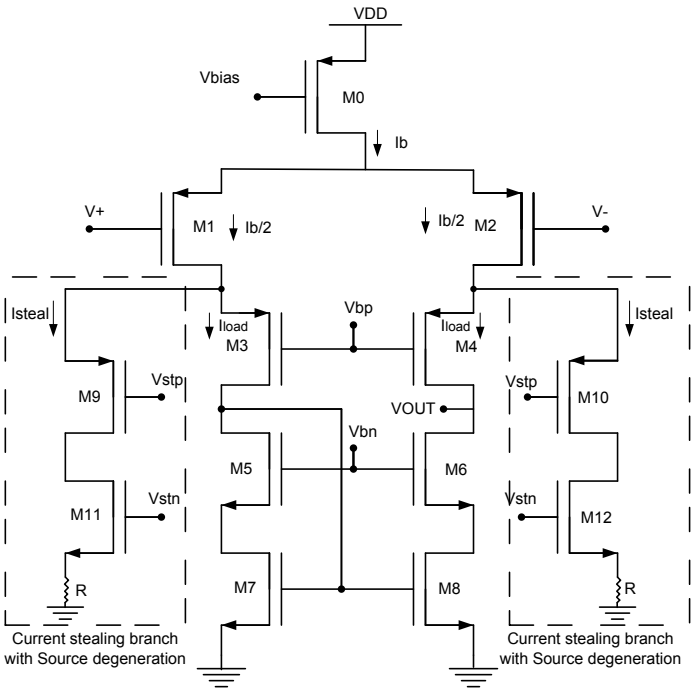

Figure 5. Proposed Telescopic Operational Transconductance Amplifier (OTA).

4. Proposed Low Noise OTA Design

The Inversion Coefficient (IC) can be calculated, based on the ratio of drain current (I_D) to the moderate inversion (IC = 1, both currents are equal) characteristic current (I_S) [3].

$$\text{IC} = \frac{I_D}{I_S} \tag{1}$$

The calculation of the modern inversion characteristic current (I_S) [14] is given by

$$I_S = \frac{2\mu C_{OX} U_T^2}{k} \frac{W}{L} \tag{2}$$

where,
U_T = Thermal voltage (KT/q) = 26 mV,
C_{OX} = Oxide Capacitance per unit area,
μ = Mobility of charge carriers,
k = Subthreshold gate coupling coefficient (Typically, 0.7) and
$\frac{W}{L}$ = Aspect ratio of transistor.

MOS transistors are modeled using any one of the following: BSIM, PSP, EKV or ACM [15]. In this work, EKV semi-empirical model is used. The EKV Model is chosen for low power circuit design and this model is also valid for three regions of operation [16].
MOS transistor Trans conductance (g_m) is

$$g_m = \frac{kI_D}{U_T} \frac{2}{1 + \sqrt{1 + 4IC}} \tag{3}$$

where,
k = Sub threshold slope factor (0.7) is equivalent to $1/n$, n represents reciprocal of surface potential. Table 1 shows the different regions of operation based on their Inversion Coefficient (IC) [17].

Table 1. Relation between g_m, I_D and Region of operation with Inversion Coefficient (IC).

Inversion Coefficient (IC)	Relation between g_m, I_D	Inversion Level	Region of Operation
IC > 10	$g_m \alpha \sqrt{I_D}$	Strong inversion	Saturation region
10 > IC > 0.1	g_m overestimate	Moderate inversion	Middle region
IC < 0.1	$g_m \alpha I_D$	Weak inversion	Subthreshold region

From the Qian [18], the typical "bio-signals" background noise is in the range of 5–10 μVrms. Input referred noise level of OTA should be kept lower than the base level of the "bio-signals" and this noise will effect the OTA performance [19]. Design parameters of the proposed OTA (Figure 5) are given in Table 2. To reduce OTA power consumption, the input referred noise should be varied with reference to background noise. By maximizing the input differential pair transconductance ($g_{m1,2}$), input referred noise voltage is reduced from all noise sources like load transistors and resistors with same power consumption. Input transistors are biased in deep subthreshold region with selection of an Inversion Coefficient (IC) value less than 0.1.

Table 2. Operating Parameters for transistors in OTA with I_{total} = 1.6 μA.

Devices	W/L	$g_m(\mu m)$	$\frac{g_m}{I_D}(V^{-1})$	$I_D(A)$
M0	900 n/130 n	35	22	1.6 μ
M1, M2	80 μ/6 μ	21.28	26	800 n
M3, M4	900 n/2.2 μ	1.97	21	90 n
M5, M6	120 n/100 n	1.90	20	90 n
M7, M8	120 n/100 n	1.933	21	90 n
M9, M10	3 μ/100 n	19.6	17	710 n
M11, M12	820 n/100 n	16	17	710 n

In order to reduce the noise of telescopic OTA, source degeneration resistors are used which provide significant reduction in flicker noise. Noise contribution of different transistors in a circuit is given by the following relative formulae,

$$FlickernoisePSD = i^2_{n,1/f} = \frac{K}{C_{OX}WL} g^2_m \frac{1}{f} (A^2/Hz) \tag{4}$$

$$ThermalnoisePSD = i^2_{n,th} = 4K_B T g_m \gamma (A^2/Hz) \tag{5}$$

Equations (4) are (5) divided by $g^2_{m1,2}$

$$v^2_{n,in,OTA} = v^2_{n,in,th} + v^2_{n,in,1/f} = R + v^2_{n,in,m1} + v^2_{n,in,m7} + v^2_{n,in,m11} (V^2/Hz) \tag{6}$$

$$v^2_{n,in,th} = 4K_B T \gamma \left(\frac{R}{\gamma} + \frac{1}{g_{m,in}} + \frac{g_{m,7}}{g^2_{m,in,eff}} + \frac{g^2_{m,11}}{g^2_{m,in}}\right)(V^2/Hz) \tag{7}$$

$$v^2_{n,in,1/f} = \frac{K}{C_{ox}.f}\left(\frac{1}{W_{in}.L_{in}} + \frac{g^2_{m,7}}{W_7.L_7.g^2_{m,in,eff}} + \frac{g^2_{m,11}}{W_{11}.L_{11}.g^2_{m,in}} (V^2/Hz)\right) \tag{8}$$

$$v_{n,in,OTA}^2 = v_{n,th}^2 + v_{n,1/f}^2 = \frac{4KT\gamma}{\frac{g_m}{I_D} I_D} \left(1 + \frac{f_{co}}{f}\right) \tag{9}$$

$$v_{n,in,amp}^2 = \left(\frac{C_1 + C_f + C_m}{C_1}\right)^2 v_{n,in,OTA}^2 \tag{10}$$

where, C_1, C_f = input and feedback capacitors, C_m is miller capacitance shown in Figure 2. Equations (4) and (5) represent the contribution of noise current density in MOS transistor per unit hertz. In Equation (6) total input-referred noise of OTA is given as ratio of output-referred noise to gain. In Equations (7) and (8), thermal noise and flicker noise of the OTA are shown in terms of noise contributions of input transistors, load transistors and resistor respectively. The area (W $\times$ L)and g_m of $M_{1,2}$ are inversely proportional and transconductance of $M_{7,11}$ is directly proportional to the OTA noise. In Equation (9), overall noise of the OTA is represented in terms of $(\frac{g_m}{I_D})$ and corner frequency (f_{co}). Equation (10) states the impact of OTA noise over preamplifier. By introducing current stealing branch, $g_{m1,2}$ is increased $g_{m7,8}$ which reduces the overall input-referred noise of the OTA. Transistor total gate input referred noise is the combination of flicker noise and thermal noise. At critical frequency (f_{co}), flicker and thermal noises are equal [20].

Flicker noise in the PMOS transistors is less than NMOS due to less trapping of carriers at the gate and mobility [21]. The reason for preferring PMOS as input transistors is that flicker noise is two orders less than NMOS [22]. Larger gate area for an input differential pair reduces the flicker noise and causes instability due to larger gate capacitance (W $\times$ L area).

Low noise amplifier design needs to optimized according to the sizing and biasing of the input and load transistors. Flicker noise can be minimized by increasing the gate area (W $\times$ L) of active transistors as well decreasing the trans conductance (g_m) of load transistors. Gate area can be maximized by increasing the aspect ratio (W/L) for a constant current. Increased gate area in terms of $W_{in} \times L_{in}$ leads to a change in region of operation to the subthreshold. Due to larger g_m and lower currents, low power is attained. Noise contribution from load transistors is reduced by minimizing the transconductance ($g_{m7,8}$) through reduced current in the load transistors. Due to reduction of a large amount of current in the load transistors, output resistance and resulted gain is increased. Cascode transistors provide larger output resistance and zero noise contribution at the output side.

To minimize the noise within limited power budget, trade-off between noise and power should be considered. NEF is calculated theoretically, which is the noise-power trade-off limit. This limit is achieved by operating the transistors in either weak or strong inversion during implementation.

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\Pi U_T 4K_B TBW}} \tag{11}$$

where,
$V_{ni,rms}$ = Input referred noise voltage,
I_{tot} = Total bias current,
U_T = Thermal voltage,
K_B = Boltzman constant,
BW = Bandwidth in Hz.

A single BJT amplifier with zero flicker noise has unity NEF where MOS transistors have accounted for flicker noise. For the proposed OTA, NEF is estimated as 1.86 and compared with the previous works in Table 3.

Table 3. Report of related works done and post layout simulation results of proposed OTA.

Parameter	[8]	[1]	[2]	[5]	This Work
Technology (μm)	0.18	1.5	0.13	0.09	0.09
V_{DD} (V)	$\pm$1.8	$\pm$2.5	1.5	1	1.2
current (μA)	-	0.128	-	2.85	1.6
Gain (dB)	60.8	40	39.4	58.7	62
Power (μW)	720	0.32	1.5	2.85	1.9
Input referred noise (μVrms)	61.5	2.4	5.5	3.04	3.2
CMRR (dB)	-	88	-	-	78
NEF	-	6	-	1.93	1.86
NEF^2.V_{DD}	-	90	-		4.151
Area (μm^2)	-	-	-	-	258.43

5. Simulation and Post Layout Results

Post layout simulation results of proposed telescopic OTA are summarized as follows. All the bio-medical application amplifiers must have input referred noise less than the background noise, i.e., 5–10 μVrms. However, the proposed OTA achieved lesser noise level of 3.2 μVrms with operating frequency of 7 kHz, as shown in Figure 6. For faithful amplification and filtering of signals for bio-medical applications, the amplifier must have a minimum gain of 40 dB and phase margin greater than 45°. Post layout simulation results of the proposed design reveal that gain and phase margin are 62 dB and 57° respectively (as shown in Figure 7). The layout area (as shown Figure 8) of the proposed OTA is optimized to 258.43 μm^2.

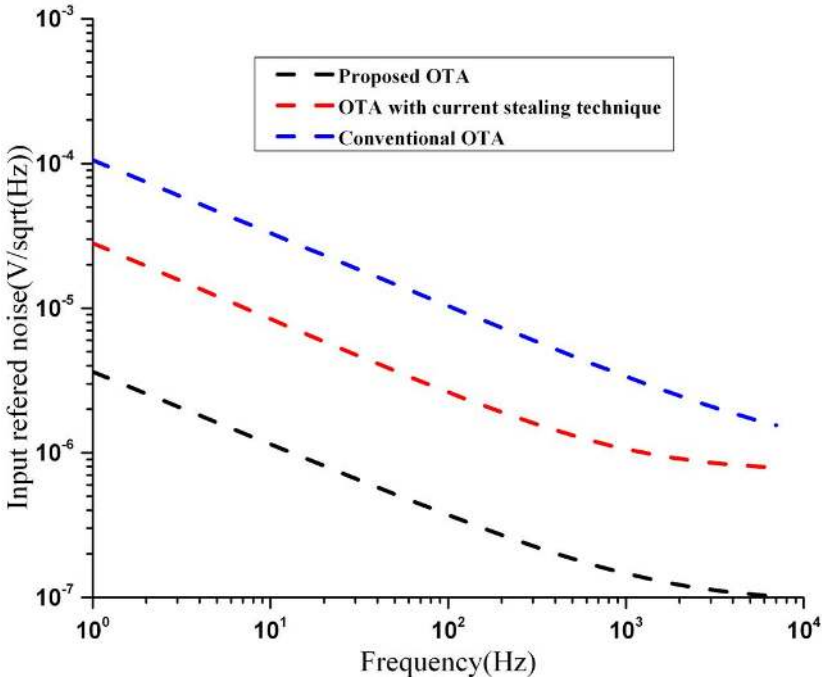

Figure 6. Total Input referred noise voltage density of the OTA.

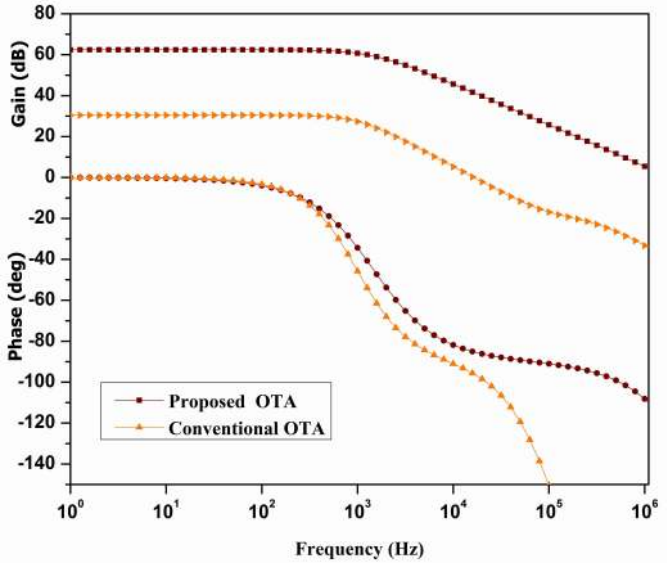

Figure 7. Post layout simulation results of amplifier gain and phase margin.

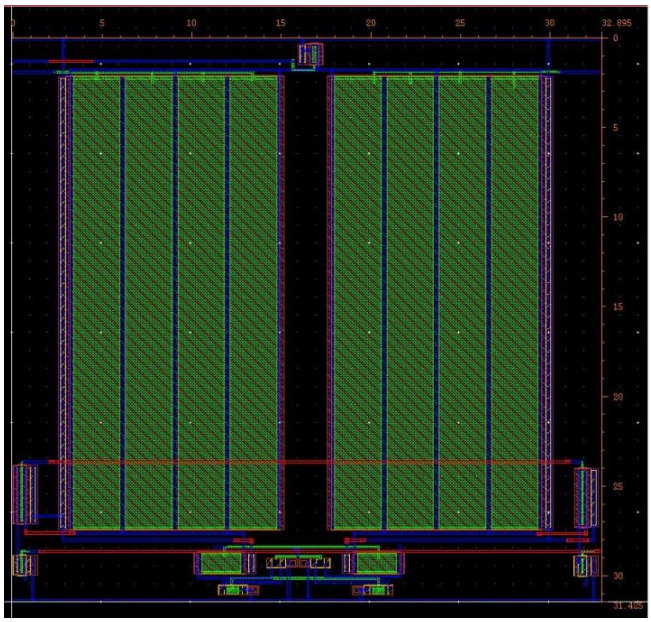

Figure 8. Layout of proposed telescopic OTA.

Table 3 reports the performance of proposed OTA design along with the other existing works. The comparison statistics between proposed and existing work are not presented since the technology node differs. Akbari and Omid [8] presented a folded cascode amplifier using gm/id methodology for flicker noise minimization. This methodology obtained better improvement in the flicker noise reduction as well as DC gain, gain-bandwidth with low power consumption. Harrinson and Charles [1] proposed a neural amplifier with low noise reduction and high power consumption from mHz to kHz. Chaturvedi and Amrutur [2] presented a paper on ultra low power and low noise neural amplifier. In his work, though new concept of current stealing is introduced and a half-side PMOS cascode is used to reduce the noise, gain is reduced. Yang and Holleman [5] presented an ultra low power low noise neural recording amplifier with better achievement in power, noise and gain with low current and supply voltage of 1 V. The proposed design parameters prove that the OTA is suitable for bio-medical applications.

6. Conclusions

The main objective of this work is to propose a telescopic OTA for better gain, low noise and power. Introduction of the current stealing branch with source degeneration will enable this proposed telescopic OTA to yield the expected application parameters. The g_m/I_D methodology is adapted for device geometry and their operating regions. EKV model is recommended for CMOS 90 nm technology. Post layout simulations are carried out with V_{DD} 1.2 V. Proposed OTA achieved 3.2 μVrms low noise level. The input transistors are operated in a subthreshold region where current levels have reduced to 1.6 μA and lead to low power consumption. Simulation results of the present work with reference to gain, power, input referred noise, CMRR and NEF have recommended that the proposed telescopic OTA is more suitable for epileptic seizure detection using EEG signal where noise limitations and gain improvements are required.

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Author Contributions: Bellamkonda Saidulu proposed and carried out the post layout simulation as part of his research. Arun Manoharan and Kumaravel Sundaram supervised the research and participated in the revision processes. All authors have read and approve the final manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

NEMS/MEMS – Nano Electro Mechanical System/Micro Electro Mechanical System
EEG – Electroencephalogram
MOS – Metal Oxide Semiconductor
DC – Direct Current
UGB – Unity Gain Bandwidth
CMRR – Common Mode Rejection Ratio
PSD – Power Spectral density

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