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Low - Power and Area - Efficient Square – Root Carry Select Adders using Modified XOR Gate

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Abstract

Background/Objectives: XOR gate is a primary element in binary adders because which is used to detect sum – output. In this paper a 2-input XOR gate is accomplished by a modified design. **Methods/Statistical Analysis:** Usually a Half Adder (HA) circuit is designed with one XOR and one AND gate but if this modified XOR is used in HA, the design requires only one XOR gate and the AND gate can be acquired from XOR gate itself. **Findings:** This modified XOR gate design gives better result when the adder circuit has more number of XOR gates, so we used this modified XOR gate in conventional sqrt CSLA, Binary to Excess-1 Converter (BEC) based sqrt CSLA and Optimized Logic Based (OLB) sqrt CSLA. The results show that Area – Delay – Product (ADP) has been reduced in proposed circuits, 12.45% in conventional sqrt CSLA, 21.45% in BEC based sqrt CSLA and 17.81% in OLB sqrt CSLA. **Applications/Improvements:** These adders can be used in Arithmetic Logic Unit (ALU) of a micro-processor as a binary adder.

Keywords: Application Specific Integrated Circuits (ASIC), Area Efficient, Low Power, Sqrt CSLA, XOR Gate

1. Introduction

The modern world is becoming a binary world, wherein, most of the applications like DSP, communication, commercial, financial, etc., binary arithmetic circuits are used[1–3]. Binary adder is inevitable in binary arithmetic circuits, Ripple Carry Adder (RCA) was popular in binary adders in early days because of simple design but output delay is more for bigger circuits, so the designers moved to fast adders like CSLA[4] and Carry Look-Ahead Adder (CLA)[5].

The Conventional CSLA is designed with 2 layers of RCA, due to more parallel paths, CSLA is quite faster than RCA, when the size of adder is upstretched, the variable sized CSLA/sqrt CSLA[6] gives result faster than uniform sized CSLA and hence the speed of the CSLA can be further improved by square root technique. The conventional CSLA and the square root (sqrt) CSLA are required more area than RCA.

Anticipated a area efficient CSLA[7] design by one RCA and one add-one circuit, kim - kim designed the add-one circuit with multiplexers, the design require less area but slower than conventional CSLA adder and unfortunately the design[7] could not work correctly due to missing of the multiplexer at the most significant bit of the add-one circuit. A 64-bit square root carry-select adder[8] is presented with only one carry evaluation block and one modified add-one circuit instead of a dual ripple-carry adder structure. Ramkumar and Harish presented a square root CSLA[9] with Binary to Excess-1 Converter (BEC), in that add – one circuit is replaced by BEC. The feature of BEC is not having of full adder and multiplexer, so area of the adder is minimized but the design is slower than conventional square root CSLA because BEC block has to wait for output of RCA in CSLA block.

Basant and Sujit[10] observed that logic optimization depends on redundant operations in the formulation and the delay relies on data dependency, finally they found a new formulation for data dependency and optimized carry generation.

Obviously, in some of the existing techniques (designs), area reduction is achieved with some delay.

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The aim of the proposed design is reducing the area and power without increasing more delay.

First we designed the 4-, 8-, 16-, 32- and 64 bit conventional sqrt CSLA, BEC based sqrt CSLA and OLB sqrt CSLA using conventional XOR gate then these circuits were designed by modified XOR gate. The results show that the design with modified XOR is better than the design with conventional XOR gate.

2. Sqrt CSLA

The conventional sqrt CSLA consists different sizes of CSLA group and each CSLA group consist two layers of RCA, first RCA layer is for Cin = 0 and second RCA layer is for Cin = 1. Each RCA has half adder and full adders besides each half adder and full adder is made up of XOR gates and these XOR gates are constructed by AND, OR and NOT gates. Block diagram of a 16 bit conventional sqrt CSLA is shown in Figure 1.

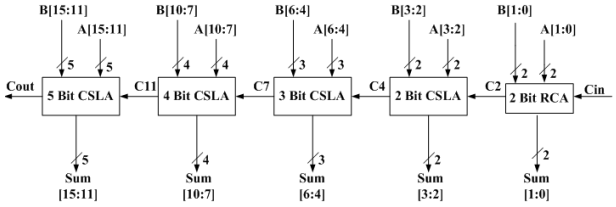

Figure 1. Block diagram of a 16 bit conventional CSLA adder.

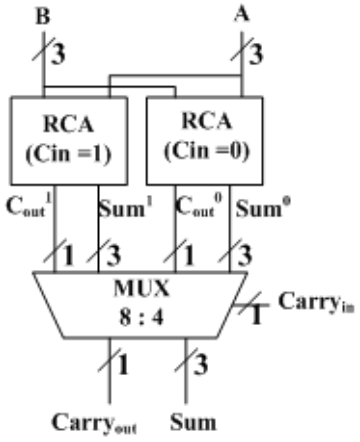

Figure 2. Block diagram of a 3 bit CSLA group.

A 16 bit sqrt CSLA needs a 2 bit RCA, 2-, 3-, 4- and 5-bit CSLA groups. Each CSLA group in 16 bit CSLA adder runs concurrently will produce 2 set of $Carry_{out}$ with Sum outputs, it needs $Carry_{in}$ for finding actual Carryout and Sum output, The $Carry_{in}$ is nothing but the $Carry_{out}$ of previous block, for instance, the $Carry_{in}$ of the 3 bit CSLA group is C4, which is $Carry_{out}$ of 2 bit CSLA group. The block diagram of a 3bit CSLA group is shown in Figure 2 and the gate level circuit of RCAs in 3 bit CSLA group is shown in Figures 3 and 4 respectively.

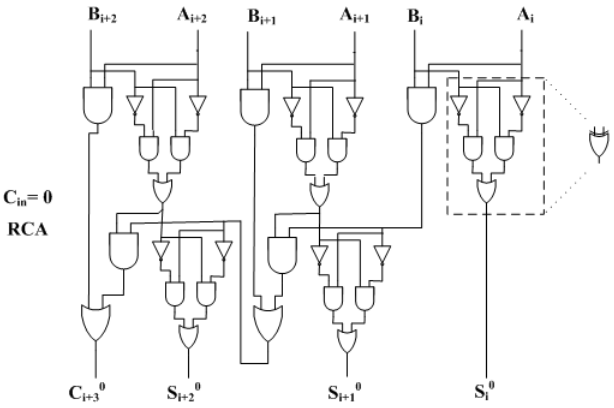

Figure 3. RCA with Cin = 0 in 3 bit CSLA group.

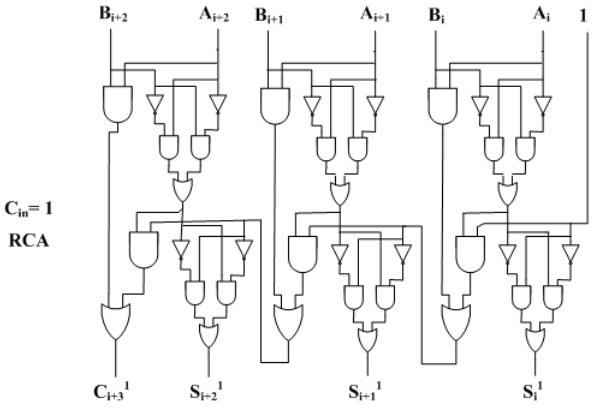

Figure 4. RCA with Cin = 1 in 3 bit CSLA group.

Here the conventional XOR gate is designed with AOI i.e. AND, OR and Inverter. The same way the remaining CSLA groups are also designed and we didn't deal with MUX because which has no XOR gate.

Table 1. The size of RCA and CSLA groups are used in 4-, 8-, 16-, 32- and 64 bit conventional sqrt CSLA adder

Size of the CSLA Adder	RCA group	CSLA group
4 bit	2 bit	2 bit
8bit	2 bit	2- and 4 bit
16bit	2 bit	2-, 3-, 4- and 5 bit
32 bit	2 bit	2-, 3-, 4-, 6-, 7- and 8 bit
64 bit	2 bit	2-, 3-, 4-, 5-, 6-, 7-, 8-, 8-, 9- and 10 bit

We designed 4-, 8-, 16-, 32- and 64 bit conventional sqrt CSLA, the groups are required for CSLA adders are given in Table 1, these adders were synthesized and shown in Table 2.

Table 2. Gates are needed for RCA, CSLA, BEC and OLB groups using modified XOR gate

	No. of Gates are needed		
Size of the Group	Conventional CSLA group	BEC based CSLA group	OLB CSLA group
2 bit (RCA)	18	18	18
2 bit	43	34	25
3 bit	65	51	39
4 bit	87	68	53
5 bit	109	85	67
6 bit	131	102	81
7 bit	153	119	95
8 bit	175	136	109
9 bit	197	153	123
10 bit	219	170	137

3. BEC based sqrt CSLA

A conventional sqrt CSLA needs more area and power because of two RCA layers, this is overwhelmed by BEC based sqrt CSLA and it has one RCA and one BEC circuit. The Block diagram of a 16 bit BEC based sqrt CSLA is shown in Figure 5.

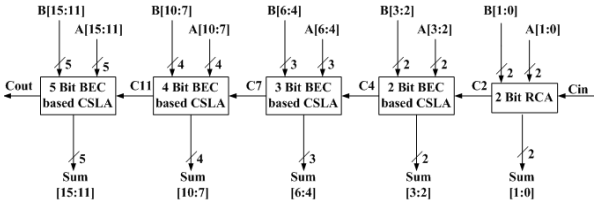

Figure 5. Block diagram of a 16 bit BEC based sqrt CSLA adder.

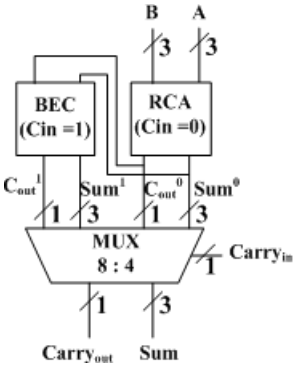

Figure 6. Block diagram of a 3 bit BEC based CSLA.

Each n bit BEC based CSLA group has one n bit RCA and one n+1 BEC block, the output of the n bit RCA is given to n+1 BEC block. The block diagram of a 3bit BEC based CSLA group is shown in Figure 6.

The gate-level circuit of a 3 bit BEC based CSLA group except MUX part is shown in Figure 7. The same logic is used for remaining BEC based CSLA groups, further we designed the 4-, 8-, 16-, 32- and 64 bit BEC based CSLA adder and synthesized results are shown in Table 3.

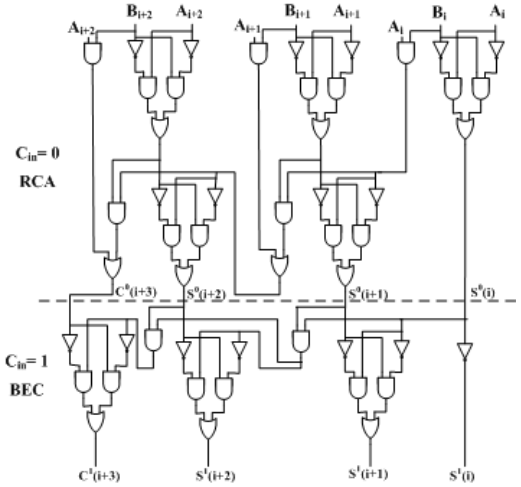

Figure 7. 3 bit RCA and 4 bit BEC gate-level circuits of a 3 bit BEC based CSLA group.

4. OLB sqrt CSLA

The OLB sqrt CSLA is unlike BEC based CSLA, here the design is optimized with the help of data redundancy, the OLB sqrt CSLA adder has different size of OLB based CSLA groups and the design has five sub-blocks namely 1) Half Sum Generation (HSG) and Half Carry Generation (HCG), 2) Carry Generation (CG_0) block for Cin = 0, 3) Carry Generation (CG_0) block for Cin = 1, 4) Final Carry Generation (FCG) and 5) Final Sum Generation (FSG). The block diagram of a 16 bit OLB sqrt CSLA adder and the block diagram of a 3 bit OLB sqrt CSLA group are shown in Figures 8 and 9 respectively.

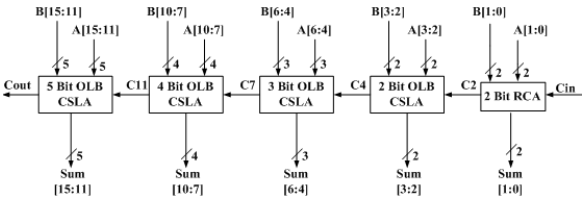

Figure 8. Block diagram of a 16 bit OLB CSLA adder.

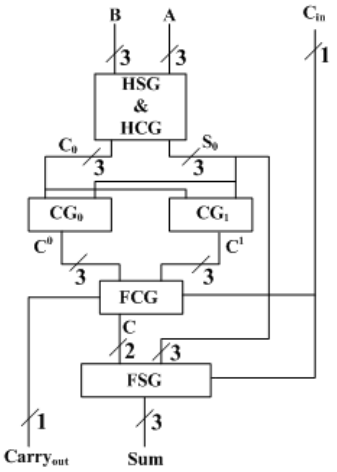

Figure 9. Block diagram of a 3 bit OLB CSLA group.

We designed the 4-, 8-, 16-, 32- and 64 bit BEC based CSLA adder and synthesized results are shown in Table 3.

The HSG and HCG, CG_0, CG_1, FCG and FSG blocks of a 3 bit OLB CSLA group are shown from Figures 10 to 14.

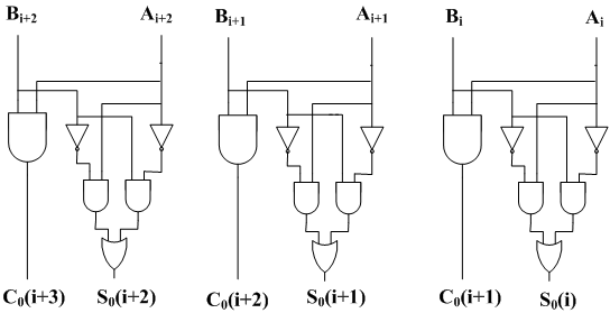

Figure 10. HSG and HCG of a 3 bit OLB CSLA group.

Table 3. ADP of 4-, 8-, 16-, 32- and 64 bit conventional CSLA, BEC based CSLA and OLB CSLA using conventional XOR and modified XOR gate

Adder	Size (Bit)	Time required (ns)	Area required (μM2)	Power consumption (μW)	Energy P x T (10-15 J)	ADP A x T (10-15)
Conventional sqrt CSLA	4	0.603	128	52.616	31.727	77.184
	8	0.844	359	154.026	129.998	302.996
	16	1.311	762	300.055	393.372	998.982
	32	1.852	1588	540.968	1001.872	2940.976
	64	2.927	3221	822.732	2408.137	9427.867
Conventional sqrt CSLA using Modified XOR gates (Proposed circuit 1)	4	0.606	123	64.305	38.969	74.538
	8	0.885	291	133.690	118.316	257.535
	16	1.608	614	223.519	359.419	987.312
	32	1.887	1273	440.054	830.382	2402.151
	64	3.193	2585	648.001	2069.067	8253.905
BEC based sqrt CSLA [7]	4	0.659	151	75.635	49.843	99.509
	8	1.009	311	122.937	124.043	313.799
	16	1.362	731	291.451	396.956	995.622
	32	1.904	1524	527.668	1004.680	2901.696
	64	2.978	3107	816.834	2432.530	9252.646
BEC based sqrt CSLA using Modified XOR gates (Proposed circuit 2)	4	0.679	119	59.898	46.671	80.801
	8	0.964	272	128.776	124.140	262.208
	16	1.382	579	231.781	320.321	800.178
	32	1.924	1196	414.877	798.233	2301.104
	64	2.998	2424	644.781	1933.053	7267.152
OLB sqrt CSLA [8]	4	0.711	131	60.123	42.747	93.141
	8	0.780	283	126.252	98.477	220.740
	16	1.197	587	229.852	275.133	702.639
	32	1.555	1212	419.966	653.047	1884.660
	64	2.288	2452	675.652	1545.892	5610.176
OLB sqrt CSLA using modified XOR gates (Proposed circuit 3)	4	0.732	104	50.236	36.773	76.128
	8	0.814	235	108.245	88.111	191.29
	16	1.138	496	206.271	234.737	564.448
	32	1.509	1033	378.289	570.838	1558.797
	64	2.202	2094	617.638	1360.039	4610.988

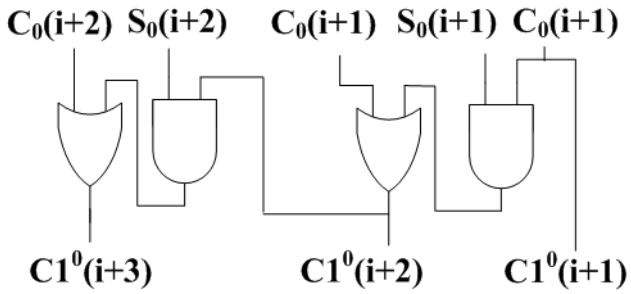

Figure 11. CG0 of a 3 bit OLB CSLA group.

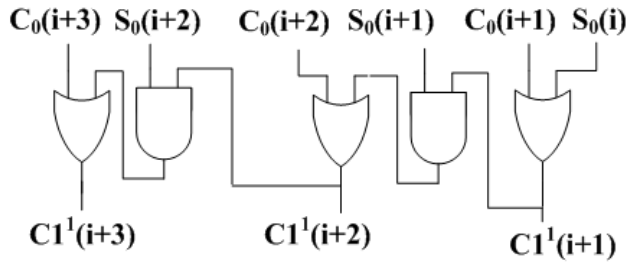

Figure 12. CG1 of a 3 bit OLB CSLA group.

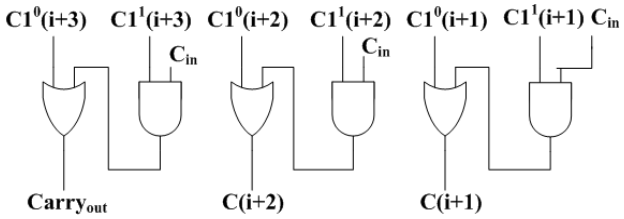

Figure 13. FCG of a 3 bit OLB CSLA group.

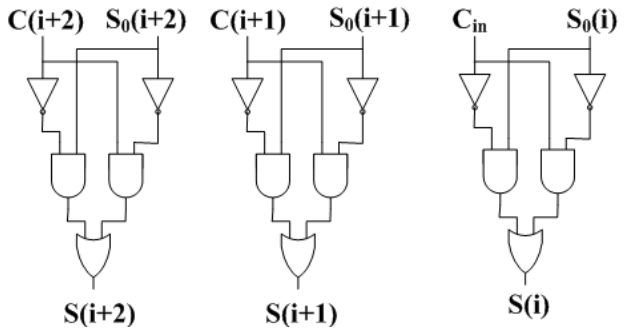

Figure 14. FSG of a 3 bit OLB CSLA group.

5. Sqrt CSLA using Proposed XOR Gate

Though the Half and Full adder are basic and primary blocks of adder circuits, inside of them XOR gates are used. Hence XOR gate is modified then there is a chance of area and power reduction, so in the proposed design, XOR gate is modified and this modified XOR gates are used in the adder design.

The modified XOR gate is shown in Figure 15. AND and OR gates are used in the first level of modified XOR gate instead NOT gates in conventional XOR gate and 4 gates are required to design a modified XOR gate but in conventional XOR, 5 gates are used.

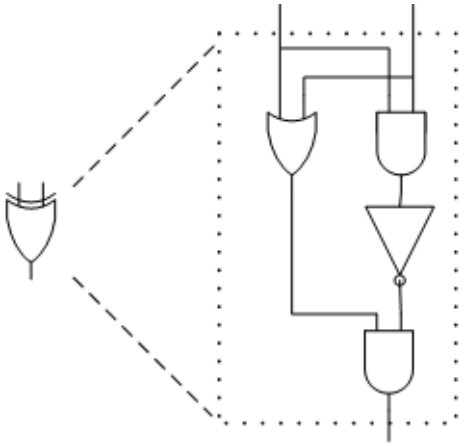

Figure 15. The modified/proposed XOR gate.

Logical expression for the modified XOR is given below:

$$output = (A+B)\bullet\overline{(A\bullet B)}$$
$$= (A+B)\bullet(\overline{A}+\overline{B})$$
$$Output = (A \oplus B)$$

Where + is OR gate, • is AND gate and ⊕ is XOR/EX-OR gate.

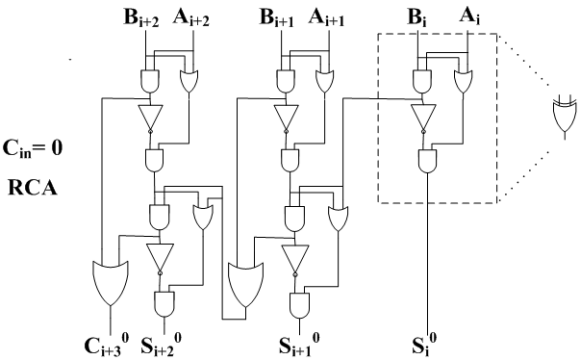

Figure 16. RCA (using modified XOR gate) with Cin = 0 in a 3 bit CSLA.

This modified XOR gate is used inside RCA and CSLA circuits to reduce required gates as well as area of the circuit. Furthermore, the design is quite easy because

conventional XOR gate is replaced by modified XOR gate are shown from Figures 16 to 20 respectively.

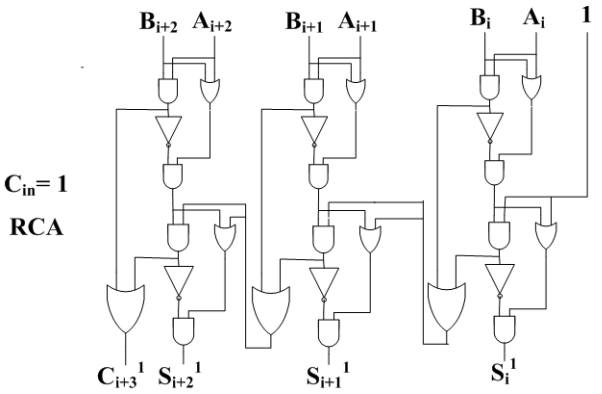

Figure 17. RCA and BEC circuits (using modified XOR gate) of a 3 bit BEC based CSLA.

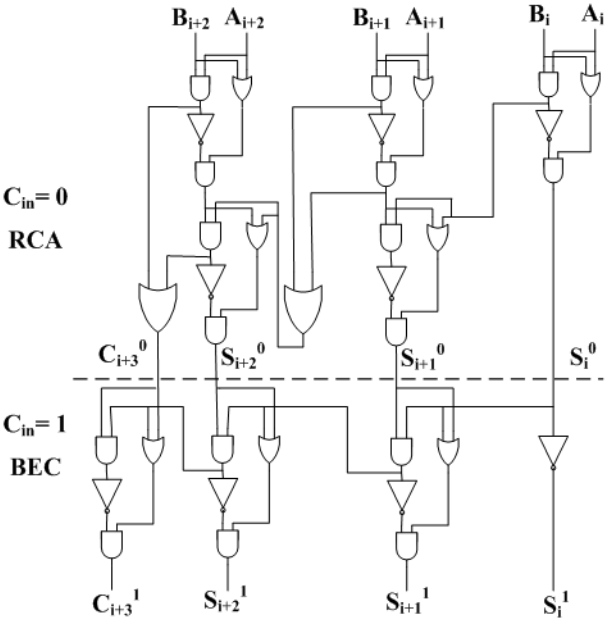

Figure 18. RCA and BEC circuits (using modified XOR gate) of a 3 bit BEC based CSLA.

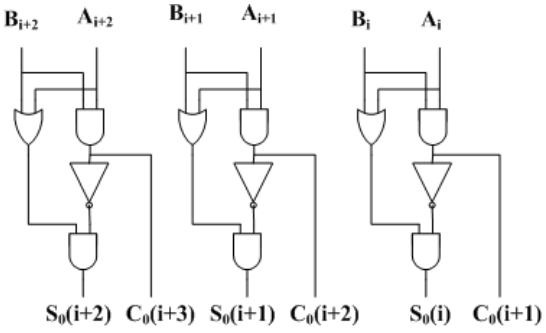

Figure 19. HSG and HCG (using modified XOR gate) of a 3 bit OLB CSLA,

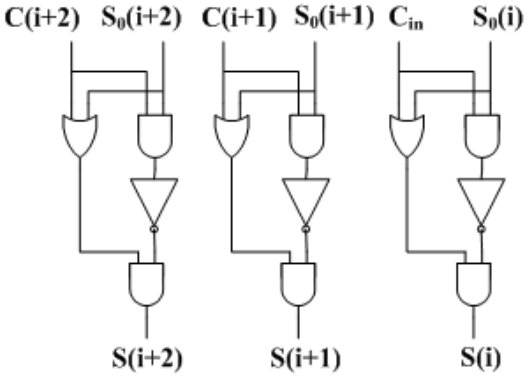

Figure 20. FSG (using modified XOR gate) of a 3 bit OLB CSLA.

We calculated the required gates for 4-, 8-, 16-, 32- and 64 bit adders besides groups in the adders are shown in Figure 21 and Table 2 respectively.

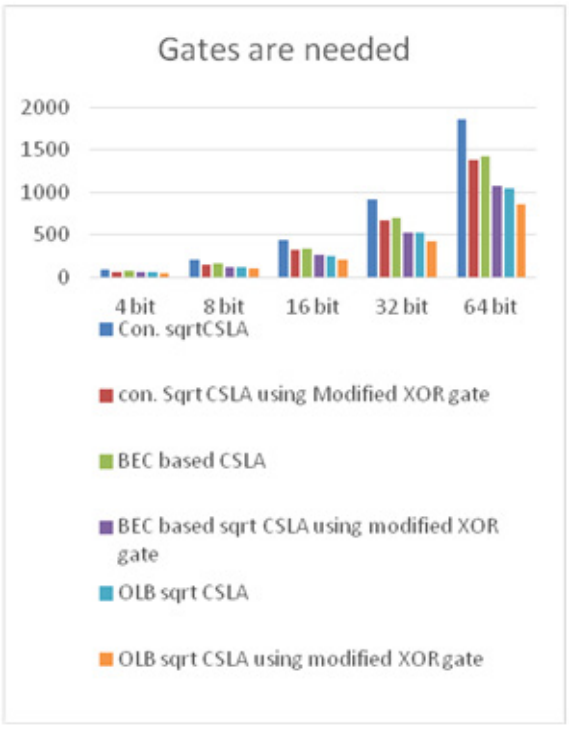

Figure 21. Gates are needed for 4-, 8-, 16-, 32- and 64 bit conventional CSLA, BEC based CSLA and OLB CSLA using con. XOR and modified XOR gate.

6. ASIC Implementation

First, we wrote the Verilog HDL code in gate level for adder circuits then they were synthesized by RC tool in cadence and we used gpdk45nm technology. The synthesized results are shown in Table 3.

ADP, Area and Power comparison charts of 4-, 8-, 16-, 32- and 64 bit Conventional CSLA, BEC based CSLA and OLB CSLA using conventional XOR and modified XOR gate are shown from Figures 22 to 24 respectively.

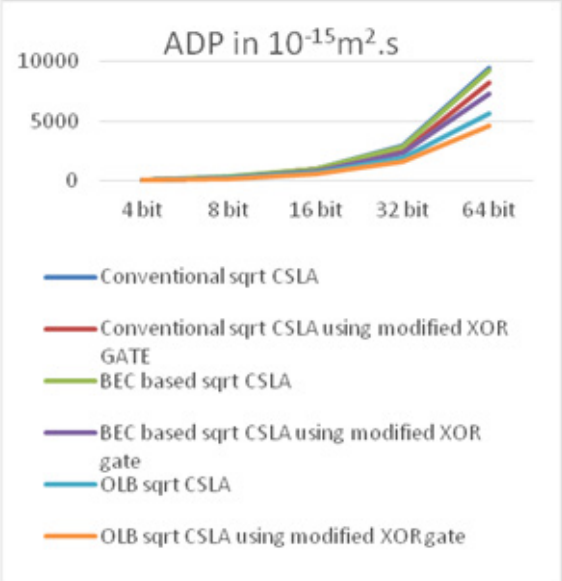

Figure 22. ADP of 4-, 8-, 16-, 32- and 64 bit Conventional CSLA, BEC based CSLA and OLB CSLA using conventional XOR and modified XOR gate.

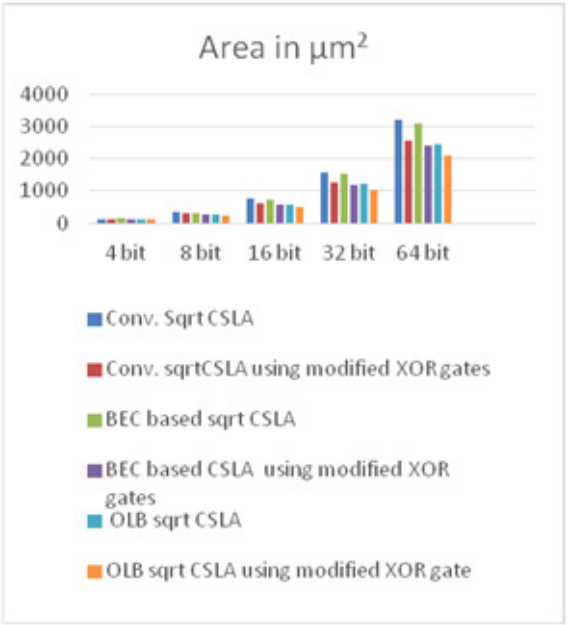

Figure 23. Required area for 4-, 8-, 16-, 32- and 64 bit Conventional CSLA, BEC based CSLA and OLB CSLA using conventional XOR and modified XOR gate.

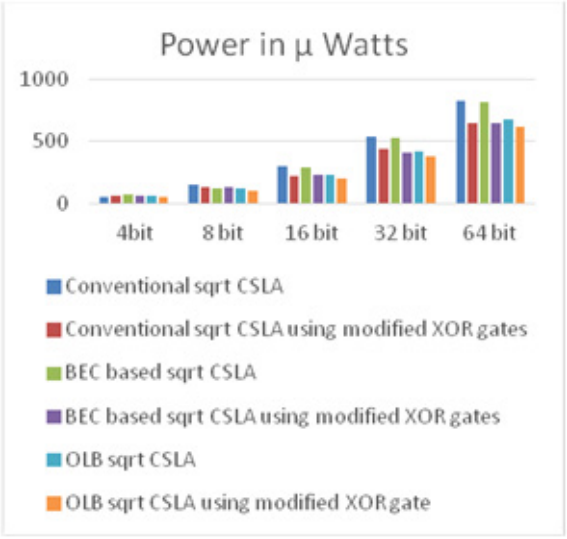

Figure 24. Power consumption of 4-, 8-, 16-, 32- and 64 bit conventional CSLA, BEC based CSLA and OLB CSLA using conventional XOR and modified XOR gate.

7. Conclusion

We designed a modified XOR gate, which was used in conventional sqrt CSLA, BEC based sqrt CSLA and OLB sqrt CSLA and the circuits were synthesized, the results shows that ADP has been reduced in proposed circuits, 12.45% in conventional sqrt CSLA, 21.45% in BEC based sqrt CSLA and 17.81% in OLB sqrt CSLA.

8. References

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