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Modified recycling folded cascode OTA with enhancement in transconductance and output impedance

Sudheer Raja VENISHETTY[1,2,*], **Kumaravel SUNDARAM**[1]

[1]Department of Micro and Nano Electronics, School of Electronics Engineering, Vellore Institute of Technology, Vellore, India

[2]Department of Electronics and Communication Engineering, Vaagdevi College of Engineering, Warangal, India

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Abstract: A modified recycling folded cascode (MRFC) operational transconductance amplifier (OTA) for achieving high DC gain, slew rate, and unity gain bandwidth (UGB) is proposed in this paper. Positive feedback is adopted to enhance DC gain and unity gain bandwidth. The proposed MRFC OTA is compared with conventional folded cascode (FC), recycling folded cascode (RFC), and other OTAs existing in the literature. Three OTAs, FC, RFC, and MRFC, are realized and implemented using the UMC 180 nm CMOS process for the same bias current of 300 μA. The designs are simulated in the Cadence Spectre Environment. From the simulation results, it may be noted that the proposed amplifier achieves a gain of 76.24 dB and unity gain bandwidth of 74.7 MHz with an input referred noise and slew rate of 139.2 μV_{rms} and 64.05 V/μs respectively. The proposed amplifier occupies an area of 2760 μm^2.

Key words: Amplifiers, CMOS, input referred noise, recycling folded cascode, slew rate, unity gain bandwidth, transconductance

1. Introduction

Operational transconductance amplifiers (OTAs) are the basic building blocks used for realizing analog systems like analog-to-digital converters or filters. To realize these systems, OTAs are required to have high DC gain, high slew rate, and high unity gain bandwidth. As technology scales down, the intrinsic gain $(g_m.r_o)$, which becomes the bottleneck to design high-performance OTAs, has been reduced. To overcome this limitation, in deep submicron technologies, folded cascode OTA is the preferred topology due to its high gain and large swings. In the existing literature, FC OTAs are extensively analyzed for achieving high gain, high slew rate, and high unity gain bandwidth. In [1, 2], the FC OTA uses current recycling to enhance transconductance, gain, bandwidth, and slew rate. In [3, 4], an improved recycling structure of a folded cascode amplifier (IRFC) enhanced the transconductance and unity gain bandwidth by separating AC and DC currents. An RFC OTA with increase in transconductance and output impedance by using positive feedback was presented in [5], while the works in [6, 7] employed phase network and additional current sources to improve the performance of RFC. In [8], an RFC OTA with current steering positive feedback was presented for enhancing the DC gain. In [9], an adaptive improved recycling folded cascode amplifier with improved gain, high slew rate, high phase margin, and reduced power consumption was discussed. In [10], a self bias cascode current mirror with frequency compensation is utilized for enhancing the phase margin of the RFC OTA. In [11], the FC OTA was

*Correspondence: kumaravel.s@vit.ac.in

implemented for achieving higher DC gain and unity gain bandwidth with low power consumption using the enhanced recycling technique by operating all the transistors in the subthreshold region.

The existing architectures of FC and RFC OTAs are discussed in Section 2 of the paper. Section 3 describes the architecture and analysis of the proposed MRFC OTA. Simulation results and the conclusion are presented in Sections 4 and 5, respectively.

2. Conventional FC and RFC OTAs

The operation of FC and RFC OTAs existing in the literature is reproduced here for the sake of clarity. Figure 1 and Figure 2 show the conventional FC and RFC amplifiers, respectively. In the conventional FC OTA, transistors M3 and M4 conduct high current and exhibit high transconductance. Since their role is limited to providing a folded node, they do not contribute to the overall transconductance of the OTA. To utilize transistors M3 and M4 in a contribution for transconductance of the OTA, a modified FC OTA is proposed and referred to as a recycling folded cascode OTA [2]. In the RFC OTA, input transistors M1 and M2 are split into four transistors, M1a, M1b, M2a, and M2b, which carry equal currents. Additionally, current mirrors M3a, M3b and M4a, M4b are formed by modifying the M3 and M4 transistors separately with a current-carrying ratio of k:1. The crossover connections shown in Figure 2 ensure the in-phase addition of small signal currents at the sources of M5 and M6, respectively. Moreover, transistors M11 and M12 are added to the current mirrors to ensure equal drain potentials of M3a and M3b and of M4a and M4b, respectively.

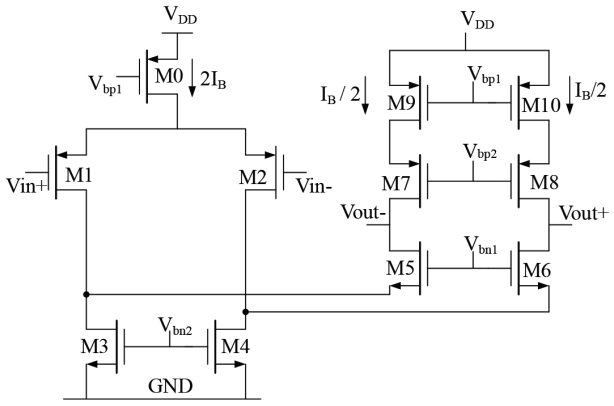


Figure 1. Folded cascode amplifier (FC).

From [2], it is observed that the effective transconductance (G_m) of the FC and RFC is given by:

$$G_{mFC} = g_{m1}, \tag{1}$$

$$G_{mRFC} = g_{m1a}.(1+k). \tag{2}$$

Eq. (2) suggests that the increase in gain bandwidth product is because of enhancement in overall transconductance. However, the phase margin is degraded by the large value of k. For k=3, the transconductance of the RFC is double that of the FC and hence the gain and gain bandwidth (GBW) of the RFC are also doubled.

3. Architecture of the proposed amplifier

In [2], the RFC is implemented to improve the DC gain and UGB (unity gain bandwidth) with low power compared to the FC OTA. Furthermore, to increase the gain and to provide separate paths for AC and DC

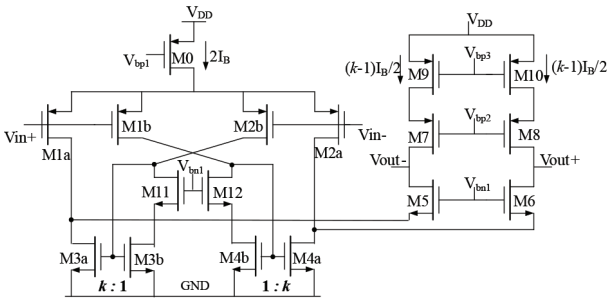


Figure 2. Recycling folded cascode amplifier (RFC).

currents, two new transistors, M3c and M4c, are introduced to the RFC structure and this is called IRFC OTA [3]. In IRFC, the enhancement of transconductance (G_m) can be achieved by driving transistors M9 and M10 shown in Figure 3 with an incremental signal from the drain of M2b and M1b, respectively. Tail current $2I_B$ from M0 is distributed among each transistor with ratios chosen as follows: M1a : M1b = M2a : M2b = $x : (1-x)$, where $0 < x \leq 1$; M3a : M3b : M3c = M4a : M4b : M4c = $(1+x) : y : z$, where $y + z = (1-x)$, M3a : M3b and M4a : M4b ratio is $(1+x) : y$, M11a : M11b = M12a : M12b = $y : z$. The architecture is referred to as MRFC, as shown in Figure 3.

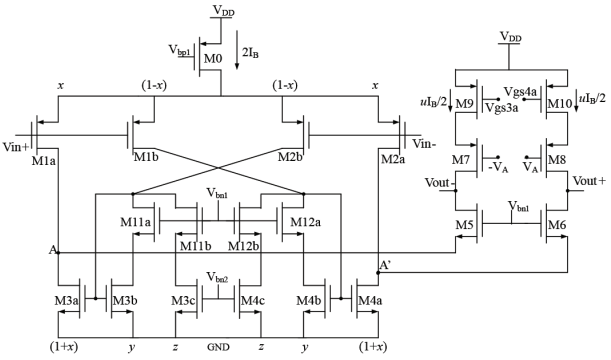


Figure 3. Modified recycling folded cascode amplifier (MRFC).

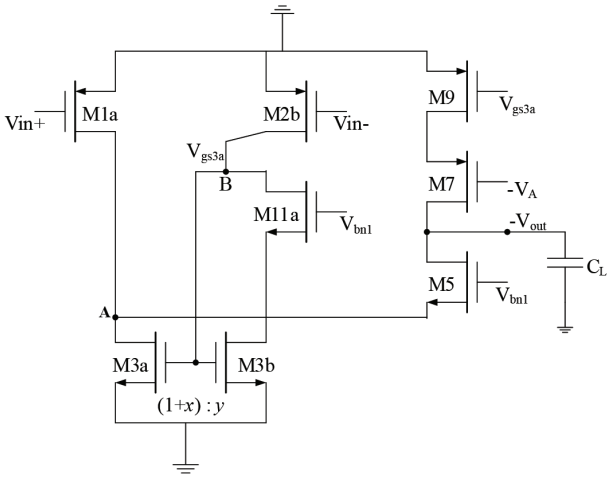


Figure 4. Half circuit transistor model of proposed MRFC amplifier.

3.1. DC Gain

The low-frequency gain of an OTA is expressed as:

$$A_V = G_m R_{OUT}. \tag{3}$$

The DC gain can be increased either by increasing effective transconductance or by output impedance or both in an OTA.

3.1.1. Transconductance (G_m) enhancement

The effective transconductance (G_{mMRFC}) of the MRFC OTA shown in Figure 3 is obtained from a half circuit transistor model and small signal equivalent model of the MRFC as depicted in Figure 4 and Figure 5,

respectively. The small signal analysis is done from loop 1 and loop 2 with different node voltages V_A, V_{gs3a}, and V_{out} at nodes A and B and output, respectively, as shown in Figure 5. Effective transconductance is found by shorting V_{out} to the ground and assuming I_S current into the output node.

The equivalent transconductance can be expressed as the ratio of short circuit current (I_S) to the input voltage (V_{in}).

As shown in Figure 5, from loop 1,

$$V_{gs3a} = g_{m2b}.V_{in}.(r_{02b} \| \frac{1}{g_{m3b}}) \cong \frac{g_{m2b}}{g_{m3b}}.V_{in}, \tag{4}$$

and from loop 2,

$$I_S \cong g_{m3a}.V_{gs3a} + g_{m1a}.V_{in} + g_{m9}.V_{gs3a}. \tag{5}$$

Substituting Eq. (4) in (5) results in:

$$I_S \cong V_{in}.[g_{m1a} + \frac{g_{m3a}.g_{m2b}}{g_{m3b}} + \frac{g_{m9}.g_{m2b}}{g_{m3b}}]. \tag{6}$$

Since the currents flowing through M1a and M2b are in the ratio $x : (1-x)$, their transconductances are in the same ratio. The current flowing through M3b is mirrored by a factor of $(1+x) : y$ into M3a and hence the ratio of their transconductance is $(1+x) : y$. The transconductance ratio of M9 and M3b is $u : y$. By substituting all the current ratios in Eq. (6), the effective transconductance of the proposed amplifier is expressed as:

$$G_{mMRFC} = g_{m1a}.[1 + \frac{(1-x^2)}{x.y} + \frac{u.(1-x)}{x.y}], \tag{7}$$

where g_{m1a} is the transconductance of input transistor M1a. Eq. (7) depicts the increase in transconductance of the proposed amplifier when compared to the FC and RFC amplifiers.

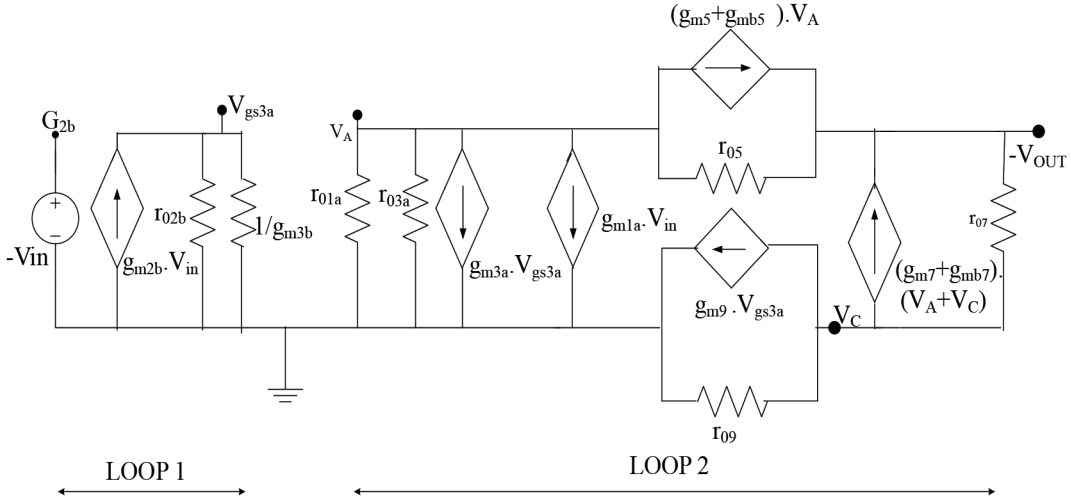


Figure 5. Half circuit small signal equivalent of MRFC.

3.1.2. Output impedance

In [5], to enhance the output impedance of the RFC OTA [2], positive feedback is implemented in the amplifier architecture by driving the gate terminal of the M7 and M8 output transistors from the folded node. The same methodology is adopted for the IRFC OTA [3] in this paper. The half circuit analysis for deriving the expression for the output impedance of the MRFC OTA is shown in Figure 6. The output impedance is expressed as a parallel combination of R_N and R_P, where R_N and R_P are the equivalent impedances looking into drains of M5 and M7, respectively.

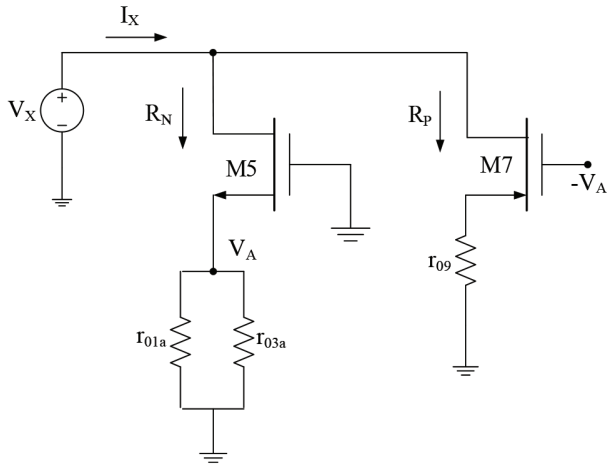


Figure 6. Small signal equivalent of positive feedback part for output impedance calculation.

Using basic Kirchhoff current laws and a small signal equivalent model, impedances R_N and R_P can be expressed as:

$$R_N \cong (r_{01a} \| r_{03a}).r_{05}.(g_{m5} + g_{mb5}), \tag{8}$$

$$R_P \cong (r_{01a} \| r_{03a} + r_{09}).r_{07}.(g_{m7} + g_{mb7}). \tag{9}$$

Therefore, the low-frequency output impedance of the proposed amplifier using Eqs. (8) and (9) can be expressed as:

$$R_{out,MRFC} = R_N \| R_P \cong r_{07}.(g_{m7} + g_{mb7}).[r_{03a} \| (r_{03a} + r_{09})]. \tag{10}$$

Similarly, the output impedance of the FC and RFC OTAs can be expressed as:

$$R_{out,FC} \cong g_{m5}.r_{05}.(r_{01} \| r_{03}) \| g_{m7}.r_{07}.r_{09}, \tag{11}$$

$$R_{out,RFC} \cong g_{m5}.r_{05}.(r_{01a} \| r_{03a}) \| g_{m7}.r_{07}.r_{09}, \tag{12}$$

where r_{0i} is drain-to-source resistance of transistor i and g_{mi} is the transconductance of corresponding transistor i.

From Eq. (10) it is found that the output impedance of MRFC is very high compared to the FC and RFC OTAs. With these modifications, an enhancement of 10–20 dB gain is expected compared to the FC and RFC configurations.

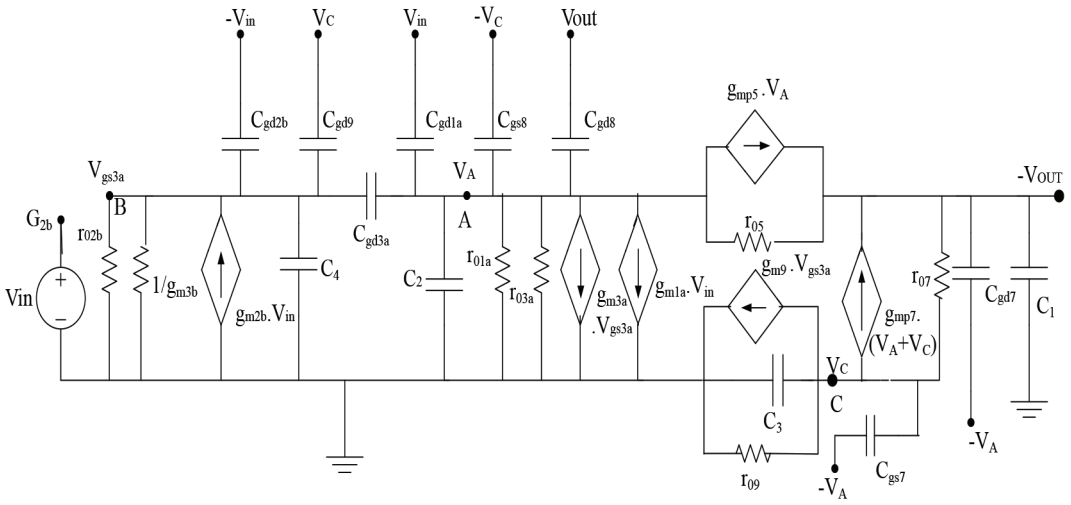


Figure 7. High frequency half circuit equivalent of MRFC.

3.2. Frequency response

The frequency response of the MRFC OTA is derived from its high-frequency half circuit equivalent shown in Figure 7. The circuit consists of 4 nodes named A, B, C, and D at the drains of M1a, M2b, M9, and M5, respectively. The voltages associated with each node are labeled as V_A, V_{gs3a}, V_C, and V_{out-}. It is observed from Figure 6 that the amplifier is exhibiting 3 zeros and 4 poles. Two poles and one zero are considered for studying the frequency response, while the other poles and zeros have been neglected, assuming that they exist at a very high frequency when compared to dominant poles.

3.2.1. Dominant pole

The pole that is closer to the origin is considered to be the dominant pole. Since output node D is connected with high output impedance $R_{out,MRFC}$ and large load capacitance C_L, it contributes to a dominant pole. The pole frequency is expressed as:

$$\omega_{p1} = \frac{1}{R_{out,MRFC}.C_1}, \tag{13}$$

where $R_{out,MRFC} = R_N \| R_P \cong r_{07}.(g_{m7} + g_{mb7}).[r_{03a} \| (r_{03a} + r_{09})]$ and $C_1 \cong C_L + C_{gd5} + C_{db7} + C_{db5}$.

3.2.2. Nondominant pole:

The nondominant pole occurs in cascode node A, i.e. the drain of M1a is at a very high frequency in contrast to the dominant pole. This nondominant pole frequency can be expressed as:

$$\omega_{p2} = \frac{1}{R_2.C_2}, \tag{14}$$

where $R_2 \cong r_{o1a} \parallel r_{o3a} \parallel r_{o5} \parallel \frac{1}{g_{m5}}$ and $C_2 \cong C_{db1a} + C_{db3a} + C_{gb8} + C_{sb5} + C_{gs5}$.

3.2.3. Zero

The existence of the feedforward path for the input signal through C_{gd1a} introduces a zero in the transfer function. The frequency of this zero is given as:

$$\omega_{z1} \cong \frac{g_{m1a}}{C_{gd1}}. \tag{15}$$

3.2.4. Unity gain bandwidth:

The unity gain bandwidth (UGB) of an OTA is expressed as:

$$UGB = A_o.f_{-3dB}. \tag{16}$$

From Eqs. (7), (10), and (13),

$$UGB = \frac{g_{m1a}.[1 + \frac{(1-x^2)}{x.y} + \frac{u.(1-x)}{x.y}]}{C_1}. \tag{17}$$

With Eq. (17) it is inferred that the proper selection of x, y, u will lead to enhanced UGB of the proposed amplifier compared to FC and RFC configurations.

3.3. Noise

Noise has become the limiting factor in analog systems, especially when implemented for biomedical applications. In this section noise expressions for FC, RFC, and MRFC OTAs are derived. The extreme noise current measured at the output of a single MOSFET is expressed as:

$$\bar{i}_0^2 = [4K_BT\gamma g_m + \frac{k_f.I_D}{C_{ox}.L^2.f}].\Delta f = [4K_BT\gamma g_m + \frac{k_f.{g_m}^2}{C_{ox}.W.L.f}].\Delta f. \tag{18}$$

The first term in Eq. (18) corresponds to thermal equivalent noise, while the latter represents the flicker noise component. To simplify the analysis, the thermal and flicker noise components are separately found and examined. The transistors that contribute more noise in the circuit include M1a, M2a, M1b, M2b, M3a, M3b, M9, and M10. The other transistors contribute comparatively less noise current.

The input referred thermal noise component of the FC, RFC, and MRFC OTA is expressed as:

$$\bar{V}_{iT,FC}^2 = \frac{8K_BT\gamma}{g_{m1}}[1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}].\Delta f, \tag{19}$$

$$\bar{V}_{iT,RFC}^2 = \frac{8K_BT\gamma}{(k+1)g_{m1a}}[\frac{1+k^2}{1+k} + \frac{g_{m3a}}{g_{m1a}} + \frac{g_{m9}}{(k+1)g_{m1a}}].\Delta f, \tag{20}$$

$$\bar{V}_{iT,MRFC}^2 = \frac{8K_BT\gamma}{g_{m1a}.(\psi)^2}.[\varphi + \frac{g_{m3a}}{g_{m1a}}.[1 + \frac{(u+x+1)^2}{(1+x).y}] + \frac{g_{m9}}{g_{m1a}}].\Delta f. \tag{21}$$

The input referred flicker noise component of three amplifiers can be expressed as:

$$\bar{V}_{if,FC}^2 = \frac{K_p}{\mu_p C_{ox}^2 f(WL)_1}[1 + 2\frac{K_n}{K_p}(\frac{L_1}{L_3})^2 + (\frac{L_1}{L_9})^2].\Delta f, \tag{22}$$

$$\bar{V}_{if,RFC}^2 = \frac{K_p}{\mu_p(1+k)C_{ox}^2 f(WL)_{1a}}[\frac{1+k^2}{1+k} + \frac{K_n}{K_p}k(\frac{L_{1a}}{L_{3a}})^2 + \frac{k-1}{k+1}(\frac{L_{1a}}{L_9})^2].\Delta f, \tag{23}$$

$$\bar{V}_{if,MRFC}^2 = \frac{K_p}{\mu_p C_{ox}^2 f(WL)_{1a}(\psi)^2}[\varphi + \frac{K_n}{K_p}[\frac{1+x}{x} + \frac{(u+x+1)^2}{xy}](\frac{L_{1a}}{L_{3a}}^2) + \frac{u}{x}(\frac{L_{1a}}{L_9})^2].\Delta f, \tag{24}$$

where $\psi = 1 + \frac{(1-x).(u+x+1)}{x.y}$, $\varphi = 1 + \frac{(1-x).(u+x+1)^2}{x.y^2}$.

Comparing Eqs. (19), (20), and (21), it is found that the thermal noise component of the MRFC OTA is lower than that of the FC and RFC OTAs. Similarly, from Eqs. (22), (23), and (24), it is found that the flicker noise of MRFC is smaller than that of its counterparts FC and RFC. This reduction is observed due to an increase in the overall transconductance of MRFC.

3.4. Slew rate

Slew rate is the design parameter that affects the settling time of OTAs. Slew rate is derived by assuming capacitive load C_L and applying a large signal at the inputs of the amplifier. When Vin+ in Figure 3 goes high, M1a and M1b are turned off. This increases the drain voltage of M4a, which leads M6 to be turned off while M2a is driven into the deep triode region. Consequently, tail current $2I_B$ flows through M2b and part of the same flows through the DC path M3c, M11b in a ratio of $(1-x) : z$, and the remaining goes through M3b and is mirrored into M3a by a factor of $(1+x) : y$ and by a factor of $z : y$ into C_L, respectively. As a result, the current through load capacitor C_L is increased. Hence, the slew rate of MRFC is increased. The slew rate expressions for the FC, RFC, and MRFC OTAs are:

$$SR_{FC} = \frac{2I_B}{C_L}, \tag{25}$$

$$SR_{RFC} = \frac{2kI_B}{C_L}, \tag{26}$$

$$SR_{MRFC} = \frac{(2-z)(u+x+1)I_B}{y.C_L}. \tag{27}$$

Eq. (27) ensures that the proper selection of x, y, z, and u leads to an enhanced slew rate for the proposed OTA compared to FC and RFC configurations.

3.5. Input offset voltage

Amplifiers exhibit a finite output voltage even for zero input conditions, leading to either systematic or random deformities termed as "offset". Systematic offset results because of the improper selection of amplifier design or inappropriate quiescent operating points of active devices. The random offset is due to process variations or mismatched devices. The offset voltage is the minimum amount of input voltage required to make the output zero. Using Pelgrom's mismatch model as in [12, 13], the input offset voltage of a device can be expressed as:

$$\sigma^2(V_{GS}) = \sigma^2(V_T) = \frac{A_{V_T}^2}{W.L}, \tag{28}$$

where A_{V_T} is the area proportionality constant for threshold voltage V_T and is provided by the process technology.

Using Eq. (28), the input offset voltages of all the three configurations of FC, RFC, and the proposed amplifier shown in Figure 1, Figure 2, and Figure 3, respectively, are expressed as follows:

$$\sigma^2(V_{i,OS,FC}) = 2.\frac{A^2_{V_{T_P}}}{W_1.L_1}[1 + 2\frac{\mu_n}{\mu_p}(\frac{A_{V_{T_N}}}{A_{V_{T_P}}})^2(\frac{L_1}{L_3})^2 + (\frac{L_1}{L_9})^2], \tag{29}$$

$$\sigma^2(V_{i,OS,RFC}) = 2.\frac{A^2_{V_{T_P}}}{W_{1a}.L_{1a}}[\frac{1+k^2}{(1+k)^2} + \frac{\mu_N}{\mu_P}\frac{k}{1+k}(\frac{A_{V_{T_N}}}{A_{V_{T_P}}})^2(\frac{L_{1a}}{L_{3a}})^2 + \frac{k-1}{(k+1)^2}(\frac{L_{1a}}{L_9})^2], \tag{30}$$

$$\sigma^2(V_{i,OS,MRFC}) = 2.\frac{A^2_{V_{T_P}}}{W_{1a}.L_{1a}.\psi^2}[1 + (\frac{1+x}{y})^2 + \alpha.\frac{\mu_N}{\mu_P}(\frac{A_{V_{T_N}}}{A_{V_{T_P}}})^2(\frac{L_{1a}}{L_{3a}})^2 + u.\frac{L_{1a}}{L_9})^2], \tag{31}$$

where $\psi = 1 + \frac{(1-x).(u+x+1)}{x.y}$ and $\alpha = \frac{(x+y+1).(1-x)}{y^2}$.

4. Simulation results

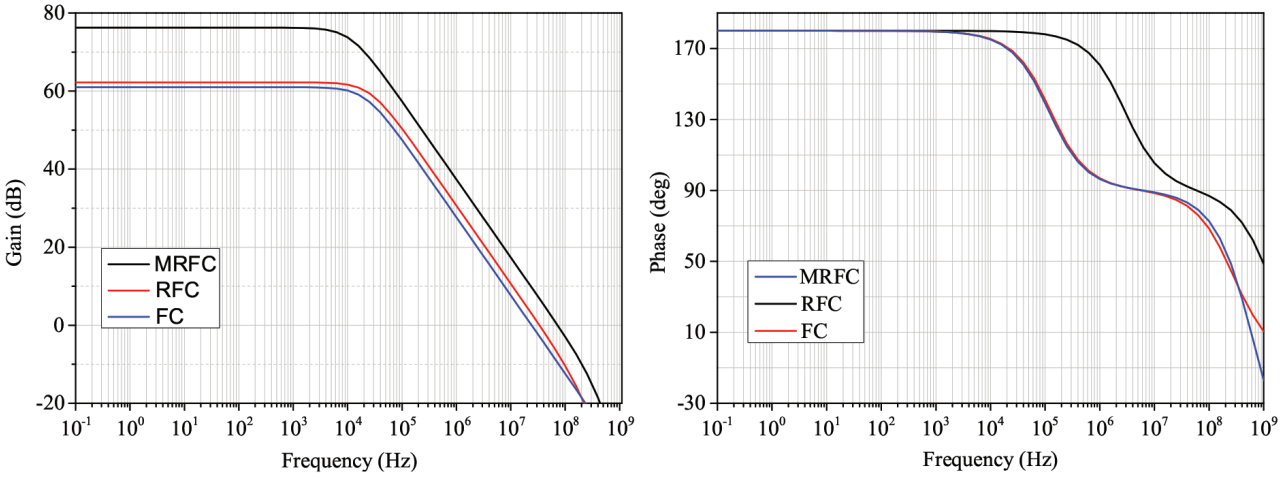
4.1. Performance comparison of FC, RFC, and MRFC OTAs

Three OTA configurations of FC, RFC, and MRFC are implemented using the UMC 180 nm CMOS process for a bias current of 300 μA with a supply voltage of 1.8 V. The bias currents of FC, RFC, and MRFC are split in the ratios of 1:1, $k:1$, and $(1+x):y:z$, respectively. For achieving stability conditions, the values of k, x, y, z, and u for RFC and MRFC amplifiers are considered to be 3, 0.5, 0.25, 0.25, and 2, respectively. Table 1 illustrates the device sizes used for implementing the FC, RFC, and MRFC amplifier configurations. For ease of implementation, the length of all the transistors is fixed at 500 nm [14–16]. The load capacitance C_L for all the OTAs is considered to be 5 pF. The open loop AC responses of all three configurations are shown in Figure 8. The simulated unity gain bandwidth of FC, RFC, and MRFC is found to be 24.6 MHz, 34.4 MHz, and 74.71 MHz, respectively. Compared with the FC, the UGB of the MRFC is improved by 3 times, while the enhancement is around 2.2 times when compared with the RFC. The phase margin of the FC, RFC, and MRFC is 88.418^o, 79.78^o, and 74.40^o, respectively.

For the slew rate, a large step of $1.8V_{PP}$ at 1 MHz is applied to the amplifiers and responses are illustrated in Figure 9. The slew rates of the three configurations are 13.85 V/μs, 40.6 V/μs, and 64.05 V/μs, respectively. It shows that the slew rate of the MRFC OTA is improved by 5 times compared to FC and 1.6 times compared to RFC.

The noise performance of FC, RFC, and MRFC are characterized by simulation. The spectral density of input referred noise of all three configurations are illustrated in Figure 10. The integrated input referred noise for a frequency range of 1 Hz to 100 MHz for FC, RFC, and the proposed amplifier are 220.4 μV_{rms}, 201.3 μV_{rms}, and 139.2 μV_{rms}, respectively.

For the offset calculation, the circuit has been connected in voltage follower mode and the difference between two input nodes is measured. The offset standard deviation of the MRFC OTA is found to be in line with the FC and RFC OTAs. The layout of the proposed amplifier is developed and it is found that the area occupied by the MRFC OTA is 2760 μm^2, which is smaller than the other two configurations. The layout of the MRFC is illustrated in Figure 11.



(a) Magnitude Response (b) Phase Response

Figure 8. AC frequency response of FC, RFC, and MRFC amplifiers.

Table 1. Obtained transistor width (μm) for L = 500 nm.

Device	FC	RFC	MRFC
M0	164.14	161.6	158.2
M1/M2	43.86	-	-
M1a/M1b/M2a/M2b	-	11.2	12.08
M3/M4	29.89	-	-
M3a/M4a	-	120	8.28
M3b/M4b	-	40	1.54
M3c/M4c	-	-	4.02
M5/M6	60.11	7.06	16.02
M7/M8	104.12	110	92.2
M9/M10	78.25	80	3.9
M11/M12	-	40	-
M11a/M12a	-	-	1.54
M11b/M12b	-		4.02

Furthermore, to study the robustness of the proposed amplifier against mismatch and process spreads, Monte Carlo simulations of all three configurations are carried out for 1000 runs to find the offset, as illustrated in Figure 12. Figure 13 shows the effects of various process corners (TT, SS, and FF) on the frequency response of the proposed OTA.

4.2. Performance comparison of IRFC and MRFC amplifiers

In order to validate the proposed enhancements in MRFC, the IRFC architecture discussed in [8] is simulated using UMC 180 nm CMOS for a bias current of 300 μA with a supply voltage of 1.8 V. Simulations are conducted on the assumption that x, y, and z of the MRFC are equivalent to p, $\alpha(1-p)$, and $\beta(1-p)$ of IRFC reported in [3], while u is equivalent to $K-1$ of IRFC in [8]. For simulation purposes, MRFC's x, y,

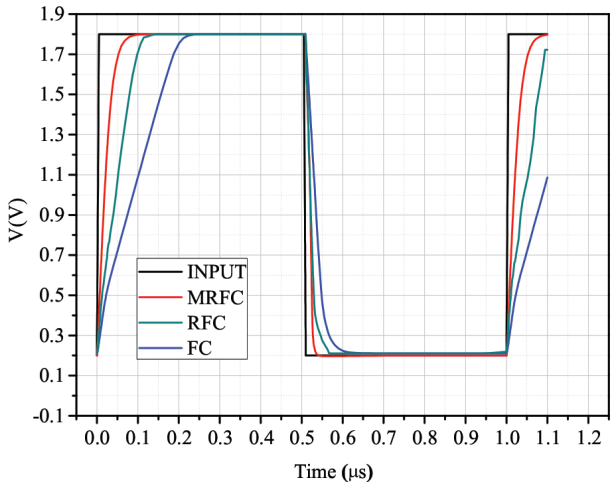


Figure 9. Step response of FC, RFC, and MRFC amplifiers.

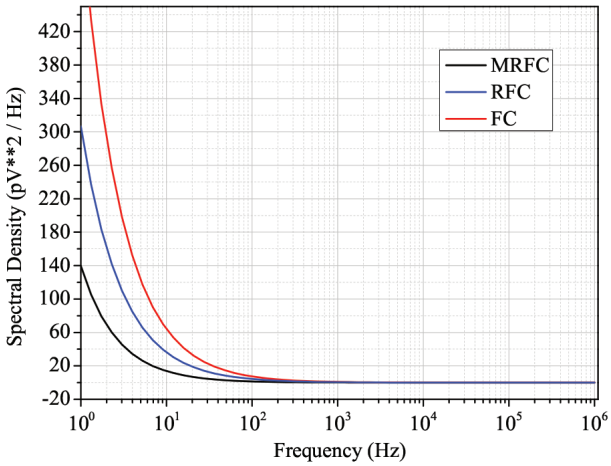


Figure 10. Spectral density of input referred noise for FC, RFC, and MRFC amplifiers.

Table 2. Operating points of different transistors of FC, RFC, IRFC, and MRFC OTAs.

Architecture	FC			RFC			IRFC			MRFC		
Transistor	g_m (μS)	g_{mb} (μS)	r_0 $(K\Omega)$	g_m (μS)	g_{mb} (μS)	r_0 $(K\Omega)$	g_m (μS)	g_{mb} (μS)	r_0 $(K\Omega)$	g_m (μS)	g_{mb} (μS)	r_0 $(K\Omega)$
M1/M2	817.6	227	199	-	-	-	-	-	-	-	-	-
M1a/M1b/ M2a/M2b	-	-	-	297.2	85.25	448.1	297.2	85.25	448.1	307.3	87.76	438.7
M3 / M4	1934	373.6	26.9	-	-	-	-	-	-	-	-	-
M3a / M4a	-	-	-	2296	452.9	26.58	2296	452.9	26.58	908.7	172	41.17
M3b / M4b	-	-	-	768.4	151.4	81.28	768.4	151.4	81.28	157.5	29.86	184.2
M3c /M4c	-	-	-	-	-	-	247.4	47.7	209.4	247.4	47.7	209.4
M5 / M6	1465	211.1	37.08	697.4	99.73	59.34	998	142.7	41.18	1003	143	46.02
M7 / M8	1098	278.5	114.7	1125	299.5	129.5	1128	300.3	140.8	1043	253.5	86.43
M9 / M10	1011	300.9	105.2	1008	300.1	72.5	1008	300	72.64	187.6	61.87	52.18

z, and u are considered to be respectively 0.5, 0.25, 0.25, and 2 while IRFC's K and a are assumed to be 3 and 0.25. Table 2 shows the operating points of transistors used in the architectures of FC, RFC, IRFC, and MRFC. The comparison between IRFC and MRFC in terms of effective transconductance, output impedance, and DC gain is reported in Table 3. The results of the simulation show that the effective transconductance and output impedance of the proposed MRFC architecture is increased by approximately 746 μS and 712 KΩ, respectively. This improvement in effective transconductance and output impedance resulted in an increase of 6 dB in DC gain.

The performance summary of simulated results including commonly used figures of merit FoM_1 and FoM_2 are given in Table 4. The expressions for FoM_1 and FoM_2 are:

$$FOM_1 = \frac{GBW.C_L}{I_D}, \tag{32}$$

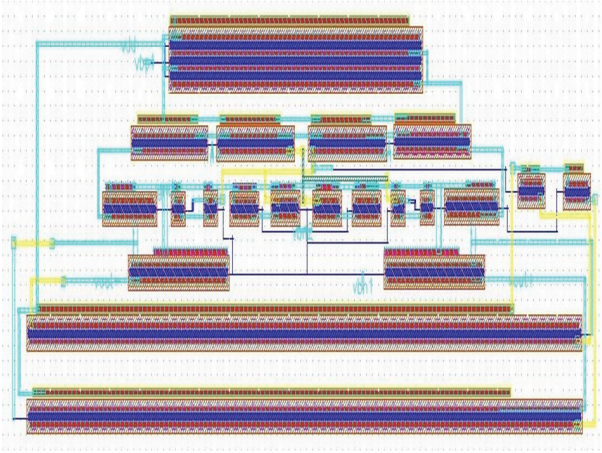


Figure 11. Layout of proposed MRFC OTA.

Table 3. Comparison of various parameters of IRFC and MRFC.

Parameter	IRFC		MRFC	
	Formula	Calculated value	Formula	Calculated value
Effective transconductance (μS)	$G_{mIRFC} = g_{m1a}.(1+\frac{K}{a})$	3863.6	$G_{mMRFC} = g_{m1a}.X^*$	4609.5
Output impedance ($K\Omega$)	$R_{out,IRFC} \cong g_{m5}.r_{05}.(r_{01a}\|\|r_{03a})\|\|g_{m7}.r_{07}.r_{09}$	946.4	$R_{out,MRFC} = R_N\|\|R_P \cong r_{07}.(g_{m7}+g_{mb7}).[r_{03a}\|\|(r_{03a}+r_{09})]$	1658
DC gain	$A_o = G_{mIRFC}.R_{out,IRFC}$	71.26 dB	$A_o = G_{mMRFC}.R_{out,MRFC}$	77.66 dB

Where $X^* = [1+\frac{(1-x^2)}{x.y}+\frac{u.(1-x)}{x.y}]$.

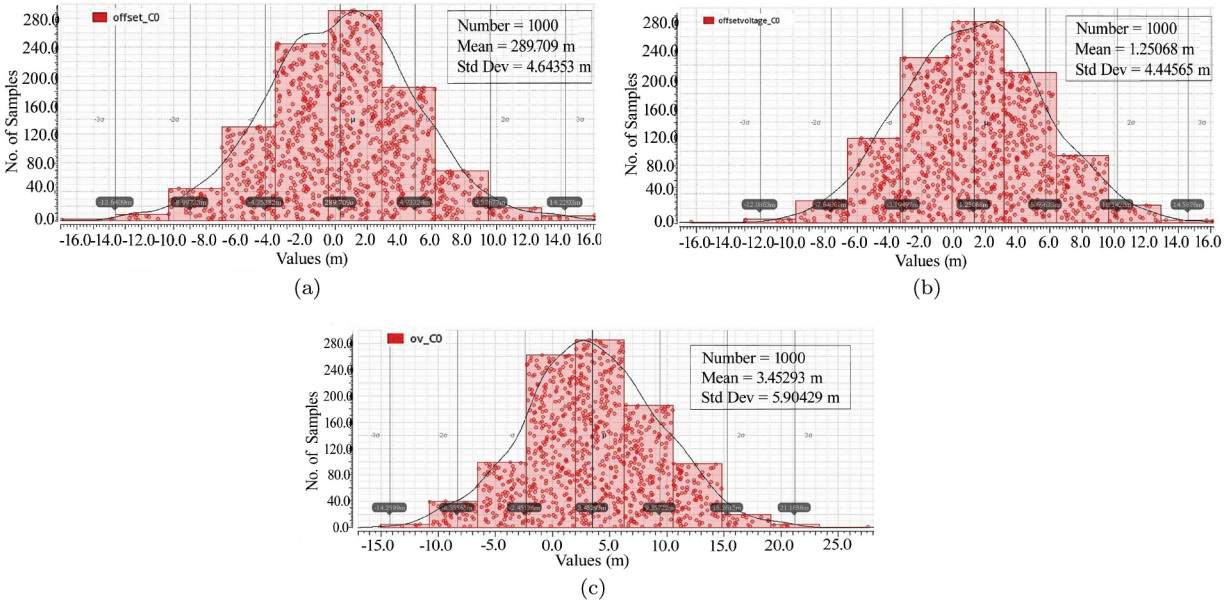
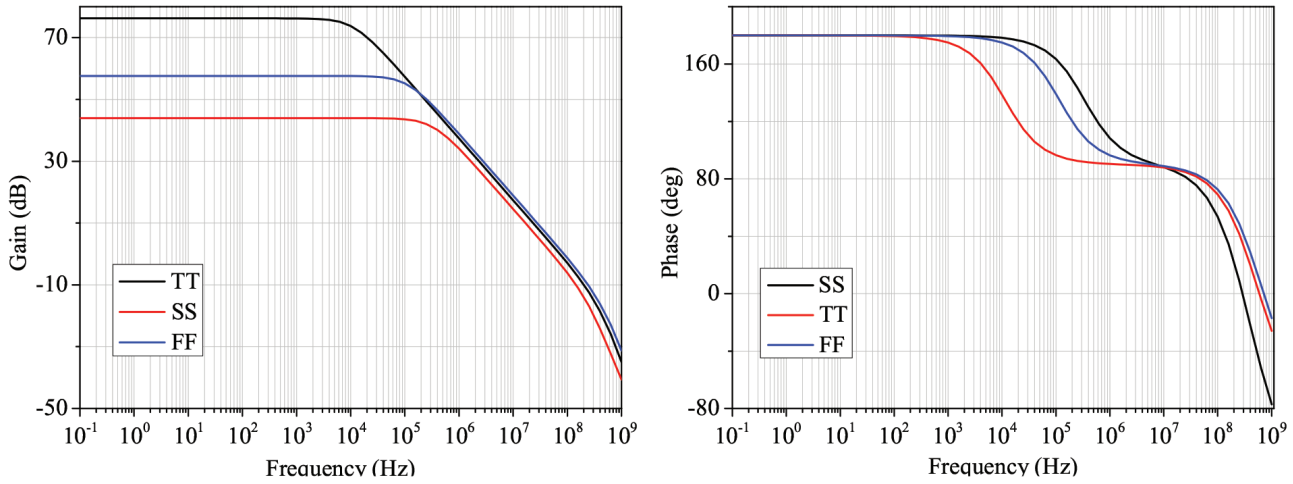


Figure 12. Monte Carlo simulations for input offset voltage of (a) FC, (b) RFC, and (c) MRFC OTA.

$$FOM_2 = \frac{SR.C_L}{I_D}. \tag{33}$$



(a) Magnitude Response (b) Phase Response

Figure 13. Frequency response of proposed OTA at various process corners (TT, SS, and FF).

From Table 4, it is observed that the proposed MRFC OTA has high FoMs compared to FC, RFC, and other OTAs considered from the literature survey.

Table 4. Performance comparison of proposed MRFC OTA with FC and RFC OTAs.

Parameter	FC	RFC	[3]	[4]	[8]	[10]	MRFC
Supply voltage (V)	1.8	1.8	1.2	1.2	1.2	1.8	1.8
Technology (nm)	180	180	130	130	90	180	180
Bias current (μA)	300	300	300	260	560	416	300
Power consumption (μW)	540	540	360	312	672	750	540
Capacitive load (pF)	5	5	5.5	7	5.6	2.5	5
Area [μm^2]	3748	4052	1139	1072	-	5000	2760
DC gain (dB)	60.9	62.8	64.9	70.2	62	59	76.24
Phase margin (^{o})	88.418	79.78	72.7	70	50	86	74.406
Unity gain bandwidth (MHz)	24.6	34.95	67	-	164	86.1	74.7
Slew rate (V/μs)	13.85	40.6	20.7	29.8	39.3	-	64.05
Input referred noise @ (1 Hz–100 MHz) (μV_{rms})	220.48	201.3	98.5	-	-	-	139.2
Input offset voltage (3σ) [mV]	4.64	4.45	-	-	-	-	5.9
FOM_1 (MHz.pF/mA)	410	573.5	1228.3	2235	-	-	1245
FOM_2 (V/μs.pF/mA)	230.8	676.6	379.5	-	393	-	1067.5

5. Conclusion

A modified version of an improved recycling folded cascode OTA is presented in this paper. Compared to FC, RFC, and IRFC OTAs, the designed circuit exhibits better performance in terms of transconductance, DC gain, slew rate, noise, and UGB, thus resulting in better FoMs with the same power consumption. The enhancement in DC gain is achieved by employing positive feedback at the cascode node. Since the proposed amplifier exhibits

reduced input referred noise compared to FC and RFC OTAs, this can be used as a preamplifier in biomedical applications. The input offset of the MRFC is also aligned with FC and RFC. The responses of the proposed amplifier at various corners are found to be well matched.

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