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Non-isolated DC–DC converter with cubic voltage gain and ripple-free input current

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Abstract: In this study, a non-isolated high gain DC–DC converter is presented. The proposed converter yields a voltage conversion ratio value which is a cubic function of the voltage gain obtained from a boost converter. The proposed converter is synthesised by judiciously interfacing a two-phase interleaved boost converter with voltage-lift capacitor and a quadratic boost converter. Resultantly, the proposed converter yields a practical voltage gain of 21.11. Further, due to the use of interleaving technique, the input current is completely free from ripples. The proposed concept is validated by conducting experiments on 18/380 V, 160 W prototype converter. The experimental results clearly demonstrate that the proposed converter operates at a full-load efficiency of 95.6%. Further, by practically implementing a simple closed-loop control, the output voltage of the converter is quickly regulated against variations in input voltage and load current so as to provide the desired 380 V across the load terminals.

1 Introduction

Tangible contributions are being made by renewable energy sources to meet the ever-increasing per capita electrical energy consumption. The output voltage from a photovoltaic (PV) panel is generally low and needs a high gain DC–DC power electronic converter interface between the source and load [1–3].

Voltage gain extension mechanisms like voltage multiplier cells [4], diode capacitor multiplier [5] and switched inductors [6, 7] are employed to enhance the voltage gain obtainable from a classical boost converter (CBC). The number of gain extension stages employed impacts the voltage gain capability and overall efficiency of the converter [4, 6]. The converter described in [7] yields a maximum voltage gain of 10.

Some of the well-known converters like single-ended primary-inductor converter and Cuk are judiciously modified to obtain higher voltage gain values [8–10]. In [11], a high gain DC–DC converter which yields a voltage gain of 12.9 is obtained by employing three switches and operating them at two different duty ratio values.

Replacing the conventional energy storage inductor with a coupled inductor (CI) in a CBC structure offers an excellent option to achieve higher voltage gain values [12]. Generally, the turns-ratio of the CI is adjusted to obtain the required voltage at the output. In [13], two CIs and four switches are employed to enable converter operation in buck and boost modes.

CIs are also employed in conjunction with gain extension modules to obtain high-voltage conversion ratios as outlined in [14–20]. CI-based converters are adopted in interleaved structures also ([15, 16, 18, 19]) to reap the dual benefits of reduced input current ripple and high-voltage gain. In [20], a three winding CI is employed and its turns ratio is adjusted to obtain a high-voltage gain of about 16.5.

The voltage gain of a CBC is significantly enhanced by cascading another similar CBC structure. The resultant converter is termed as quadratic boost converter (QBC) which yields a voltage gain that is square of the CBC's voltage conversion ratio [21]. To further enhance the voltage gain capability of the QBC, simple inductors are replaced by CIs and gain extension cells are also introduced in [22–26].

In [27], the voltage stress on the buffer capacitor is reduced, however, with a penalty of the reduced voltage gain of 4. Some QBC variants are also obtained by employing inductor–capacitor and diode combinations [28]. Since the switch is situated closer to the output, it is subjected to high-voltage stress.

The converter presented in [23] uses the basic QBC structure with CIs and snubber circuit to reduce the voltage stress on the main switch. The converter presented in [24] offers an excellent voltage gain of about 16 and operates at 1 kW power level. However, the input current is pulsed. The QBC presented in [25] employs CI and voltage doubler network to achieve a voltage gain of 12.7 with the pulsed input current.

The current ripple at the input side is reduced by employing a reasonably large energy storage inductor [17], interleaving mechanism ([16, 26]) and carefully selecting the operating duty ratio of the switches [29]. In [30], the input current ripple is reduced by adjusting the value of the magnetic element and the operating frequency. An interesting way of reducing the current ripple is described in [31, 32]; an additional winding is employed in series with a capacitor and connected at the input side.

In this paper, a high gain DC–DC converter which is constructed from an interleaved structure to reduce the current ripple at the input port is proposed. This paper is organised as follows: Section 1 presents an overview of the recent state of the art converters and a prelude to the proposed work. Section 2 provides the power circuit description of the proposed converter while its operating principle and design details are presented in Sections 3 and 4, respectively. Discussion on the experimental results is elaborated in Section 5 and the key comparative features are detailed in Section 6. In Section 7, concluding remarks are presented.

2 Description of power circuit

Fig. 1 presents the circuit configuration of the proposed high gain cubic boost converter (C^3BC). The proposed C^3BC consists of two stages. A two-phase interleaved boost converter (IBC) with voltage-lift capacitor forms stage 1 of the proposed converter while stage 2 comprises of a classical QBC structure. In stage 1, voltage lift capacitor C_{Lift} is utilised to increment the voltage gain obtained from IBC. Diode D_2 is the intermediate diode which cascades both the stages and prevents the discharge of C_1. The capacitor C_1 acts as a source for the QBC in stage 2. Diode D_0 and capacitor C_0 are the conventional output rectifier diode and output filter capacitor,

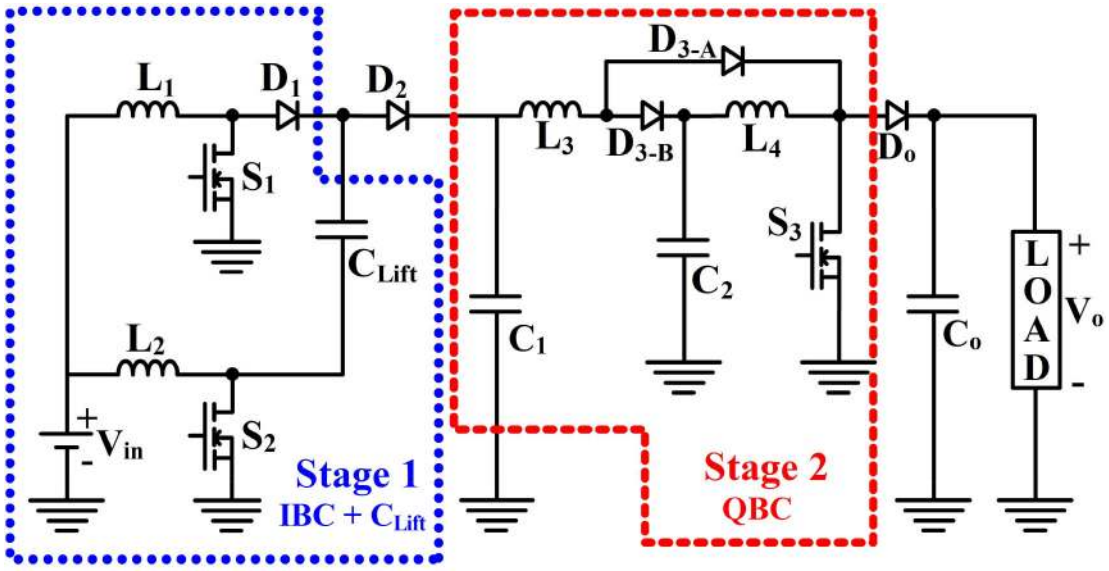


Fig. 1 *Power circuit of the proposed C³BC*

respectively. In the next section, the principle of operation is elaborated.

3 Operating principle of the proposed C³BC

The proposed C³BC consists of three switches. The switches S_1 and S_2 are located in the interleaved phases of stage 1. Hence, to cancel the input current ripple, the switches S_1 and S_2 are operated at a duty ratio of $\delta_1 = \delta_2 = \delta_0 = 0.5$ and with 180° phase-shift. The switching frequencies of S_1 and S_2 are the same and equal to $f_1 = f_2 = f_0 = 50$ kHz. Switch S_3 which is located in stage 2 of the proposed C³BC is operated at a duty ratio of $\delta_3 = 0.57$ and switching frequency of $f_3 = 100$ kHz. Stage 2 is operated at a higher frequency to reduce the inductor size. Since the two stages of the proposed converter are operated with two different switching frequencies four modes are required to elaborate its operating principle. The following effective assumptions are made to easily understand the operating principle:

(i) The power circuit comprises of ideal elements.
(ii) The converter draws continuous current from the input port; the converter operates in continuous conduction mode.
(iii) All the inductors are initially charged before the switching cycle commences.

Mode 1 (t_0–t_1): Mode 1 commences at t_0 when switches S_1 and S_3 are turned ON and switch S_2 is turned OFF. In stage 1, as S_1 is ON, the energy stored in L_1 increases. Since S_2 is OFF, the energy stored in L_2 and C_{Lift} forward biases D_2 and charges the capacitor C_1 which acts as the source to stage 2. In stage 2, as S_3 is ON, the currents flowing through L_3 and L_4 rise linearly and their stored energy increases. The diode $D_{3\text{-A}}$ is forward biased while $D_{3\text{-B}}$ and D_0 are reverse biased due to the conducting state of S_3. The capacitor C_2 transfers its stored energy to L_4 through S_3. The output capacitor C_0 supplies the load. Mode 1 ends at time $t = t_1$ when the current through the inductors L_3 and L_4 reach their respective maximum values. The equations governing mode 1 are

$$i_{L_1}(t) = I_{L_{1,\min}} + \frac{v_{L_1}}{L_1}t \tag{1}$$

$$i_{L_2}(t) = I_{L_{2,\max}} - \frac{v_{L_2}}{L_2}t = I_{L_{2,\max}} - \frac{(V_{\text{in}} + v_{C_{\text{Lift}}} - v_{C_1})}{L_2}t \tag{2}$$

$$i_{L_3}(t) = I_{L_{3,\min}} + \frac{v_{L_3}}{L_3}t = I_{L_{3,\min}} + \frac{v_{C_1}}{L_3}t \tag{3}$$

$$i_{L_4}(t) = I_{L_{4,\min}} + \frac{v_{L_4}}{L_4}t = I_{L_{4,\min}} + \frac{v_{C_2}}{L_4}t \tag{4}$$

Mode 2 (t_1–t_2): Transition from mode 1 to mode 2 occurs at time $t = t_1$ when S_3 is turned OFF. As the state of switches S_1 and S_2 remains unchanged, the operation of stage 1 is the same as in mode 1. In stage 2, as S_3 is OFF, the energy stored in L_3 and L_4 is transferred to C_2 and C_0, respectively, besides meeting the load requirement. The electrical inertia of L_3 and L_4 forward biases the $D_{3\text{-B}}$ and D_0, respectively. Since D_0 conducts, the cathode terminal of $D_{3\text{-A}}$ is held at output potential while its anode is clamped at the voltage developed across C_2. Therefore, $D_{3\text{-A}}$ is reverse biased. Mode 2 comes to an end when the inductor currents I_{L_3} and I_{L_4} reach their respective minimum values at time $t = t_2$. The following equations characterise mode 2

$$i_{L_3}(t) = I_{L_{3,\max}} - \frac{v_{L_3}}{L_3}t = I_{L_{3,\max}} - \frac{(v_{C_1} - v_{C_2})}{L_3}t \tag{5}$$

$$i_{L_4}(t) = I_{L_{4,\max}} - \frac{v_{L_4}}{L_4}t = I_{L_{4,\max}} - \frac{(v_{C_2} - v_{C_0})}{L_4}t \tag{6}$$

$$v_{C_x}(t) = V_{C_x} + \frac{i_{c_x}(t)}{C_x}t \quad \text{where } x = \text{Lift}, 1, 2, 0 \tag{7}$$

Mode 3 (t_2–t_3): Mode 3 begins at time $t = t_2$ when switch S_1 is turned OFF and the switches S_2 and S_3 are turned ON. In stage 1, as S_1 is OFF, L_1 transfers its stored energy to C_{Lift} through D_1 and S_2. Since S_2 is ON, the energy stored in L_2 increases. In stage 2, C_1 acts as a power source for the QBC structure. As S_3 is ON, all the elements used in QBC structure operate exactly similar to mode 1. The output demand is met by the capacitor C_0. When the inductor currents I_{L_3} and I_{L_4} reach their respective maximum values at time $t = t_3$, S_3 is turned OFF to mark the end of mode 3. The equations that govern the behaviour of inductors L_3 and L_4 are the same as in mode 1 (since S_3 is ON). The other governing equations are

$$i_{L_1}(t) = I_{L_{1,\max}} - \frac{v_{L_1}}{L_1}t = I_{L_{1,\max}} - \frac{(V_{in} - v_{C_{\text{Lift}}})}{L_1}t \tag{8}$$

$$i_{L_2}(t) = I_{L_{2,\min}} + \frac{v_{L_2}}{L_2} t \tag{9}$$

Mode 4 (t_3–t_4): Mode 4 commences at time $t = t_3$, when S_3 is turned OFF. Since the state of S_1 and S_2 remains unchanged from mode 3, the status of elements located in stage 1 is also similar to mode 3. The operation of elements in stage 2 is easily comprehended by observing mode 2. Since S_3 is OFF, the elements in stage 2 behave similarly as in mode 2. The equations governing mode 4 are given by (5)–(9). Figs. 2*a–d* depict the equivalent circuit during each mode.

As S_3 is operated at twice the frequency of S_1 and S_2, one switching cycle is completed at the end of mode 4. Obviously, in one switching cycle, S_1 and S_2 are turned ON and OFF once while S_3 is switched twice. Fig. 3 depicts the characteristic waveforms of the proposed C^{3}BC.

4 Voltage gain and design details

In this section, the voltage gain of the proposed C^{3}BC and its design details are presented.

4.1 Voltage conversion ratio

As there are two stages in the proposed C^{3}BC, for easier understanding, the stage-wise voltage gain is derived by employing volt-second balance concept. The voltage gain of a CBC is well known and expressed as

$$M_{\text{CBC}} = \frac{1}{(1-\delta)} \tag{10}$$

where δ is the duty ratio of the switch.

In the proposed converter, stage 1 comprises of two-phase IBC with voltage lift technique. The voltage obtained from stage 1 charges C_1 which acts as a source for stage 2. Hence, the voltage conversion ratio of stage 1 is

$$M_{\text{Stage 1}} = \frac{V_{C_1}}{V_{\text{in}}} = \frac{2}{(1-\delta_0)} \tag{11}$$

where δ_0 is the duty ratio of the switches S_1 and S_2.

Since stage 2 is a classical QBC, its voltage gain is given by

$$M_{\text{Stage 2}} = \frac{V_0}{V_{C_1}} = \frac{1}{(1-\delta_3)^2} \tag{12}$$

where δ_3 is the duty ratio of the switch S_3.

Using (11) and (12), the overall voltage gain is obtained as

$$M = \frac{V_0}{V_{\text{in}}} = M_{\text{Stage 1}} \times M_{\text{Stage 2}} = \frac{2}{(1-\delta_0)(1-\delta_3)^2} \tag{13}$$

from (13), when all the three switches are operated at the same duty ratio, the overall voltage gain is expected to be the cube of the voltage gain obtainable from a CBC as expressed in (14); voltage lift technique further doubles the voltage gain

$$M = \frac{V_0}{V_{\text{in}}} = M_{\text{Stage 1}} \times M_{\text{Stage 2}} = \frac{2}{(1-\delta)^3} \tag{14}$$

another interesting observation is inferred from (13) regarding the two degrees of freedom available to vary the voltage gain. Fig. 4 clearly demonstrates the flexibility in obtaining the desired voltage gain easily. In fact, multiple duty ratio values are possible to obtain the required voltage gain. In the proposed C^{3}BC, δ_0 is deliberately fixed at 0.5 to nullify the current ripples at the input while δ_3 is slightly varied to meet the required voltage gain.

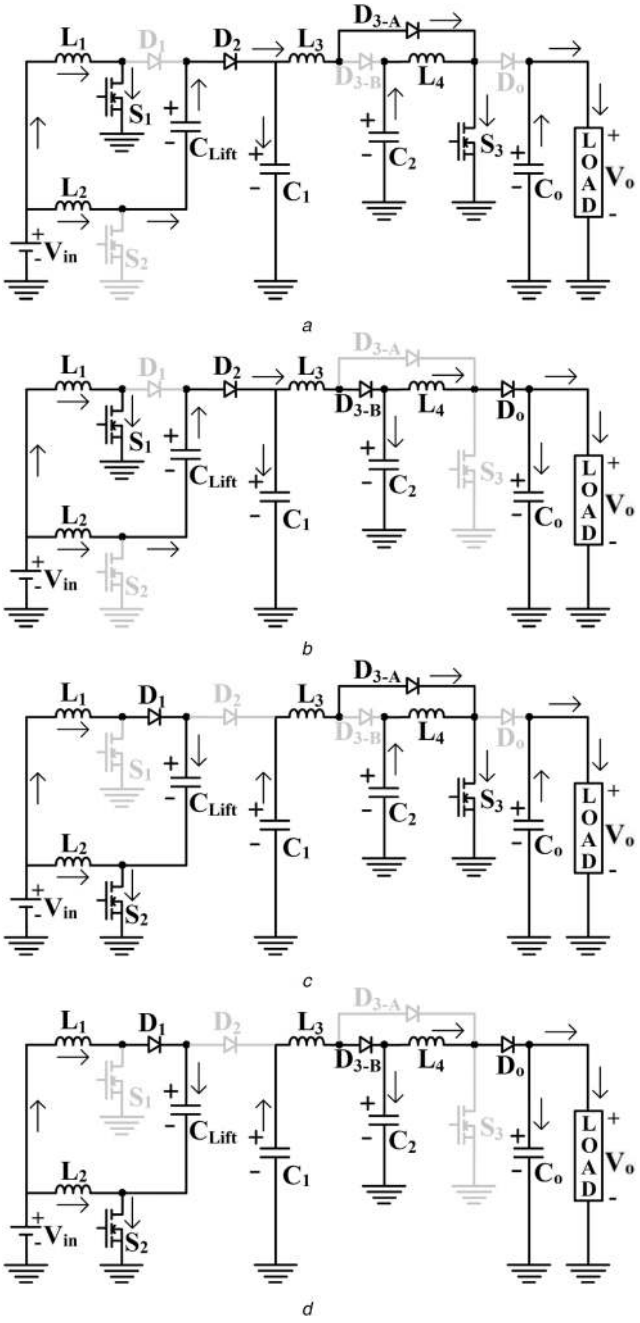


Fig. 2 *Equivalent circuit of the C^{3}BC during* ***(a)*** Mode 1, ***(b)*** Mode 2, ***(c)*** Mode 3, ***(d)*** Mode 4

4.2 Ratings of the switches

The switches in the proposed converter are subjected to different voltage stress levels as they are located in different stages of the circuit. The voltage stress on S_1 and S_2 is similar to that of in a CBC as they are employed in stage 1. Hence, their voltage stress magnitudes are given by

$$V_{S_1} = V_{S_2} = \frac{1}{(1-\delta_0)} V_{\text{in}} \tag{15}$$

In terms of output voltage, the switch stresses of S_1 and S_2 are expressed as

$$V_{S_1} = V_{S_2} = \frac{(1-\delta_3)^2}{2} V_0 \tag{16}$$

As the switch S_3 is located near the output port, its voltage stress is the same as that of the output voltage and is deduced as

$$V_{S_3} = \frac{2}{(1-\delta_0)(1-\delta_3)^2} V_{in} = V_0 \quad (17)$$

When S_1 is ON the inductor L_1 charges through S_1. Since S_1 is located in stage 1 (IBC structure), the current stress on the switch S_1 is given by

$$I_{S_1} = I_{L_1} = \frac{I_{in}}{2} \quad (18)$$

When S_2 is conducting, inductor L_2 charges through S_2 while inductor L_1 also transfers its stored energy to C_{Lift} through S_2. Hence, the current stress on the switch S_2 is the sum of the currents flowing through L_1 and L_2 as given by

$$I_{S_2} = I_{L_1} + I_{L_2} = I_{in} \quad (19)$$

4.3 Ratings of diodes

Generally, the voltage stress on diodes is determined when they are in reverse biased condition. The voltage stress magnitude is equal to voltage impressed across the anode and cathode terminals of a particular diode. In stage 1, D_1 and D_2 operate in a complementary manner. D_1 is reverse biased during modes 1 and 2; the anode of D_1 is grounded and its cathode is connected to C_1 through D_2. The voltage stress on D_1 is equal to the voltage developed across the capacitor C_1 and is given by

$$V_{D_1} = \frac{2}{(1-\delta_0)} V_{in} \quad (20)$$

during modes 3 and 4, D_2 is reverse biased; the reverse voltage applied on D_2 is equal to the difference between the voltage across capacitors C_1 and C_{Lift}. Hence, the voltage stress on D_2 is derived as

$$V_{D_2} = V_{C_1} - V_{C_{Lift}} = \frac{1}{(1-\delta_0)} V_{in} \quad (21)$$

In stage 2, diodes D_{3-A} and D_{3-B} complement each other while operating. During modes 2 and 4, D_{3-A} is reverse biased as its cathode is clamped to C_0 through D_0, while its anode is connected to C_2 through D_{3-B}. Hence, the voltage stress on D_{3-A} is determined to be

$$V_{D_{3-A}} = V_{C_0} - V_{C_2} = \frac{2\delta_3}{(1-\delta_0)(1-\delta_3)^2} V_{in} \quad (22)$$

D_{3-B} is reverse biased during modes 1 and 3; the anode of D_{3-B} is grounded through D_{3-A} while its cathode is connected to C_2. Therefore, the voltage stress on D_{3-B} is given by

$$V_{D_{3-B}} = V_{C_2} = \frac{2}{(1-\delta_0)(1-\delta_3)} V_{in} \quad (23)$$

The voltage rating of output diode D_0 is equal to the output voltage of the converter and is expressed as

$$V_{D_0} = V_0 = \frac{2}{(1-\delta_0)(1-\delta_3)^2} V_{in} \quad (24)$$

The current stress on diodes D_1 and D_2 is the same as the inductor currents I_{L_1} and I_{L_2}, respectively, and given by

$$I_{D_x} = \frac{I_{in}}{2}, \quad x = 1, 2 \quad (25)$$

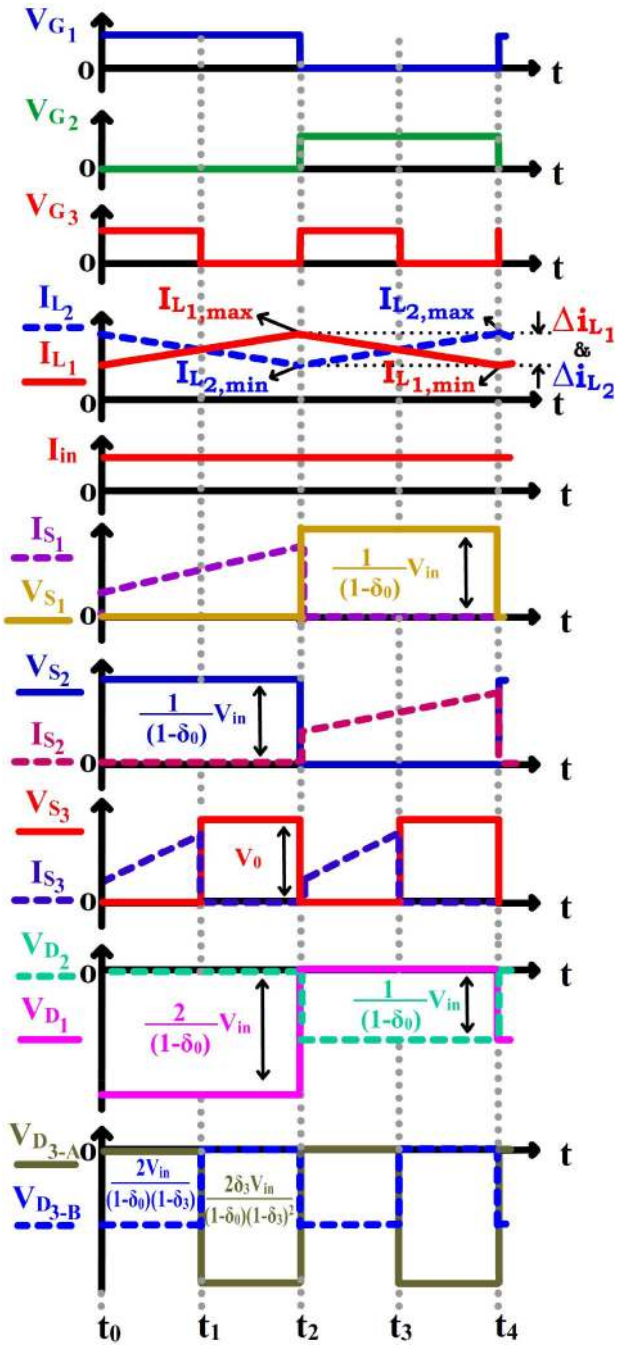


Fig. 3 *Characteristic waveforms of the proposed C^3BC*

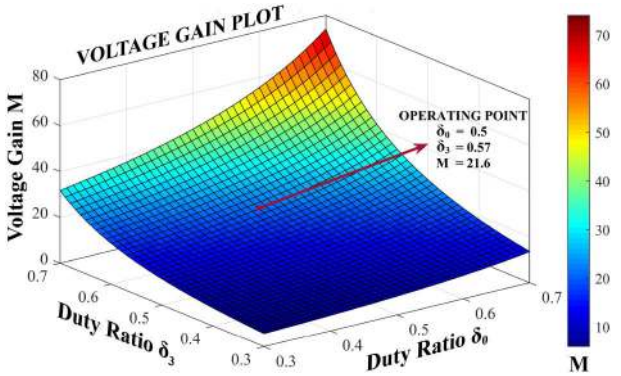


Fig. 4 *3D plot showing the voltage gain variation when duty ratios vary along with the practical operating point*

diodes $D_{3\text{-A}}$ and $D_{3\text{-B}}$ must be rated to carry currents whose magnitudes are equal to the inductor current I_{L_3}. Hence, the current stress on $D_{3\text{-A}}$ and $D_{3\text{-B}}$ is expressed as

$$I_{D_{3-A}} = I_{D_{3-B}} = I_{in}\frac{(1-\delta_0)}{2} \tag{26}$$

Due to the proximity between D_0 and load terminals, D_0 must be rated to carry I_0. Hence, its current stress is

$$I_{D_0} = I_o \tag{27}$$

4.4 Design of energy storage elements

In the proposed C^{3}BC, inductors L_1 and L_2 are the main energy storage inductors in stage 1. Since L_1 and L_2 are employed in two interleaved phases, their values are estimated based on their individual current ripple magnitudes. The inductance values are designed using

$$L_1 = L_2 = \frac{V_{\text{in}}\delta_0}{f_0\Delta i_{L_1}} \tag{28}$$

$$L_3 = \frac{V_{C_1}\delta_3}{f_3\Delta i_{L_3}} \text{ and } L_4 = \frac{V_{C_2}\delta_3}{f_3\Delta i_{L_4}} \tag{29}$$

where Δi is the current ripple in individual inductors.

In the proposed C^{3}BC, the values of δ_0 and δ_3 are fixed to achieve the required voltage gain of 21.11. As observed in (28) and (29), the inductance value is directly proportional to its input voltage and inversely proportional to frequency and current ripple. The excitation voltage to the energy storage inductors L_3 and L_4 located in the QBC structure is significantly higher; the voltage magnitude is 4 and 9.3 times the input voltage for L_3 and L_4, respectively. Obviously, operating stage 2 also at 50 kHz would yield a large inductance value even at reduced current ripple magnitude. Hence, by deliberately doubling the operating frequency of the QBC stage to 100 kHz the inductance value is only half of the inductance at 50 kHz.

Generally, the capacitances are determined from (i) the voltage ripple experienced by the capacitors, (ii) frequency, (iii) charging current and (iv) duty ratio. Therefore, the value of capacitors C_{Lift}, C_1, C_2 and C_0 is obtained as

$$C_{\text{Lift}} = \frac{I_{C_{\text{Lift}}}\delta_0}{f_0\Delta v_{C_{\text{Lift}}}},\ C_1 = \frac{I_{C_1}\delta_0}{f_0\Delta v_{C_1}} \text{ and } C_y = \frac{I_{C_y}\delta_3}{f_3\Delta v_{C_y}} \tag{30}$$

where $y = 0$ and 2.

Table 1 Proposed converter specifications

Parameter	Value
input voltage (V_{in})	18 V
output voltage (V_0)	380 V
output power (P_0)	160 W
switching frequencies	f_0 = 50 kHz, f_3 = 100 kHz
inductance of L_1, L_2	100 µH
inductance of L_3	390 µH
inductance of L_4	2 mH
duty ratio (δ)	δ_0 = 0.5, δ_3 = 0.57

Table 2 Components used in the proposed C^{3}BC

Circuit element	Device type	Part number (ratings)
switches (S_1, S_2)	MOSFET	IPP037N08N3GXKSA1 (80 V, 100 A, 3.1 mΩ)
switch (S_3)	MOSFET	IPA60R060P7XKSA1 (600 V, 48 A, 49 mΩ)
diodes (D_1, D_2)	fast recovery diode	DSS16-01A (100 V, 16 A, 0.64 V)
diodes ($D_{3\text{-A}}$, $D_{3\text{-B}}$)	fast recovery diode	DURF1030CTR (300 V, 10A, 1.3 V, dual common anode)
diode (D_0)	fast recovery diode	MUR460 (600 V, 4 A, 1.05 V)
capacitor (C_{Lift})	polypropylene capacitor	B32774D4106K000 (10 µF, 450 V)
capacitor (C_1)	electrolytic capacitor	UBW2A101MHD1TO (100 µF, 100 V)
capacitor (C_2)	electrolytic capacitor	ECO-S2DA101BA (100 µF, 200 V)
capacitor (C_0)	electrolytic capacitor	LGN2H101MELA30 (100 µF, 450 V)

5 Discussion on experimental results

A prototype version of the proposed C^{3}BC is fabricated and tested to validate the proposed concept. Table 1 provides the converter specifications while the details of the components are presented in Table 2. STM32F411RE microcontroller is employed to generate the required gating pulses of the MOSFETs. Two IR25600 dual low-side MOSFET drivers interface the microcontroller and the power switches. Four-channel digital storage oscilloscope (DSO) from Tektronix and standard accessories such as high voltage and current probes are used to obtain the required oscillograms.

The voltage gain capability of the proposed converter is validated through the experimental waveforms portrayed in Figs. 5*a*–*c*. When 18 V DC is supplied at the input port, an output of 380 V DC is obtained at the output port as depicted in Figs. 5*a* and *b*. Thus, a practical voltage gain of 21.11 is achieved using the proposed C^{3}BC. The phase-shifted operation of S_1 and S_2 owing to the interleaved structure is verified from Fig. 5*c*. The switches S_1 and S_2 are operated at a safe duty ratio of $\delta_0 = 0.5$ at 50 kHz, while S_3 is operated at $\delta_3 = 0.57$ at 100 kHz. The gating instant of S_3 is synchronised with the switches S_1 and S_2 as validated through Fig. 5*c*.

The voltage gain obtained at each stage of the proposed converter is validated through Figs. 6*a* and *b*. The voltage between the top plate of C_{Lift} and ground swings periodically depends on the states of S_1 and S_2. During modes 1 and 2, the top plate of C_{Lift} is clamped at a potential determined from (11) with respect to ground. Likewise, during modes 3 and 4, the bottom plate of C_{Lift} is grounded. Therefore, the voltage between the top and bottom plates of C_{Lift} is same as the output of a CBC. The voltage magnitude swings between 72 and 36 V as validated through the waveform presented in CH2 of Fig. 6*a*.

The voltage obtained across C_1 is equal to the output of a conventional two-phase IBC whose voltage gain is enhanced using voltage lift technique. Thus, the voltage obtained across C_1 during experimentation matches pretty closely with the analytical value computed using (11). The capacitor C_1 serves as a voltage source for stage 2 while C_2 serves as the intermediate capacitor in the QBC structure. Therefore, the voltage across C_2 is the same as that of a CBC, with C_1 considered as its input source. The practical value is in accordance with the analytical value derived using (13). Thus, the proper operation of various stages in the proposed C^{3}BC is validated and further reassured by the required voltage gain value of 21.11 at the output terminals.

Fig. 7 shows the voltage stress on the switches in comparison with the output voltage. As S_1 and S_2 are located in stage 1, they are subjected to minimal voltage stress of about 9.47% of V_0. The practical value matches correctly with the theoretical value predicted using (15). Due to interleaving, they operate with 180° phase shift which is depicted in the waveform (CH1 and CH2).

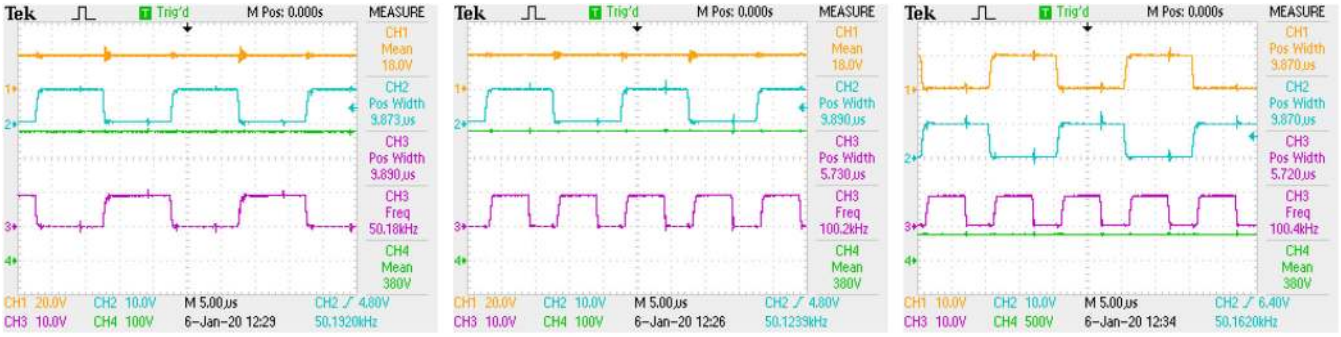


Fig. 5 *Experimental results to demonstrate the voltage gain capability of the proposed C^3BC*
(a) CH1: input voltage, CH2 and CH3: gate pulses applied to S_1 and S_2, respectively, and CH4: output voltage, ***(b)*** CH1: input voltage, CH2 and CH3: gate pulses applied to S_1 and S_3, respectively, and CH4: output voltage, ***(c)*** CH1, CH2, CH3: gate pulses applied to S_1, S_2 and S_3, respectively, and CH4: output voltage

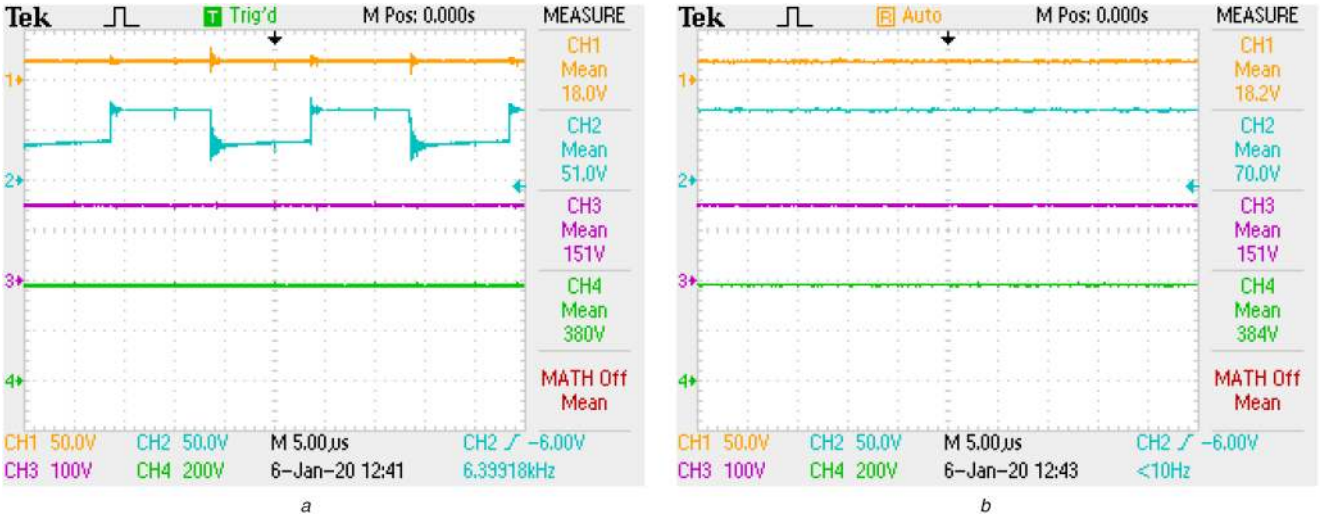


Fig. 6 *Experimental waveforms obtained from the prototype converter to validate the voltage gain at various locations*
(a) CH1: voltage at the input, CH2: voltage across top plate of C_{Lift} and ground, CH3 and CH4: voltage across C_2 and C_0, ***(b)*** CH1: input voltage, CH2, CH3 and CH4: voltage across the capacitors C_1, C_2 and C_0, respectively

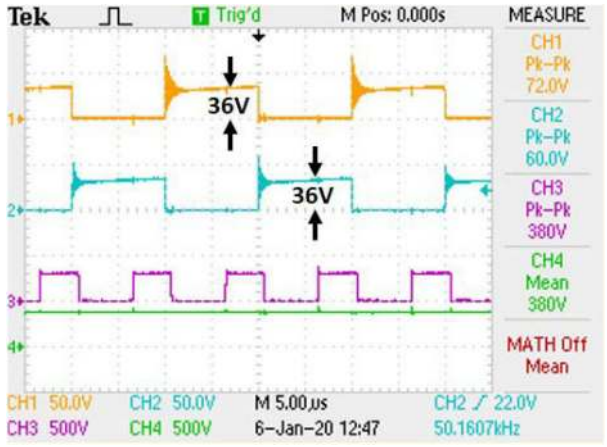


Fig. 7 *Voltage stress on switches compared with V_0 CH1, CH2, CH3: voltage stresses on S_1, S_2 and S_3, respectively, and CH4: output voltage*

Although S_3 operates at a higher frequency (100 kHz) compared to S_1 and S_2 (50 kHz), the operation of S_3 is synchronised with the other two switches.

As S_3 is located closer to the load terminals, its voltage stress is equal to the output voltage as verified from the oscillogram also. As switches with a very low drain to source resistance ($R_{\text{DS-ON}}$) are employed to obtain better-operating efficiency, slight ringing is observed in the waveforms. However, the magnitude of the ringing voltage is not alarming.

The operation of diodes D_1 and D_2 which are employed in stage 1 is verified through the waveforms presented in CH1 and CH2 of Fig. 8*a*. The complementary operation of D_1 and D_2 is clearly observed from the experimental waveforms. The practical value of voltage stress on D_1 and D_2 is 18.95 and 9.47% of V_0, respectively. The practical stress values match perfectly with the theoretical values obtained using (20) and (21). In stage 1, switch S_1 and D_1 operate in a complementary manner (similar to the switch and diode in a CBC) while S_2 compliments the operation of D_2. Fig. 8*b* confirms the complementary operation under practical conditions.

The proper operation of diodes $D_{3\text{-A}}$, $D_{3\text{-B}}$ and D_0 which are located in stage 2 is validated through Fig. 9*a*. Since $D_{3\text{-A}}$ and $D_{3\text{-B}}$ are located in the QBC structure, their complementary behaviour is evident. As discussed during the operating modes, due to the QBC structure, the conducting state of diodes $D_{3\text{-B}}$ and D_0 are similar. Based on the location and operating principle, the voltage stress experienced by the diodes during experimental conditions are in perfect accordance with the analytical values which are computed using (22)–(24). The coordinated operation of the S_3, $D_{3\text{-A}}$ and $D_{3\text{-B}}$ in the QBC structure is further validated by observing the oscillogram presented in Fig. 9*b*.

The current through the inductors L_1, L_2 and the input port is depicted in Fig. 10*a*. As interleaving mechanism is employed, (i) the net input current is equally shared by the inductors and (ii) the input current ripple is completely nullified; the minimal ripple (3.43% of I_{in}) is due to the switching action. In fact, in the proposed C^3BC, to cancel the current ripple, the switches in stage 1 are fixed to operate at a duty ratio of $\delta_0 = 0.5$ always. The required

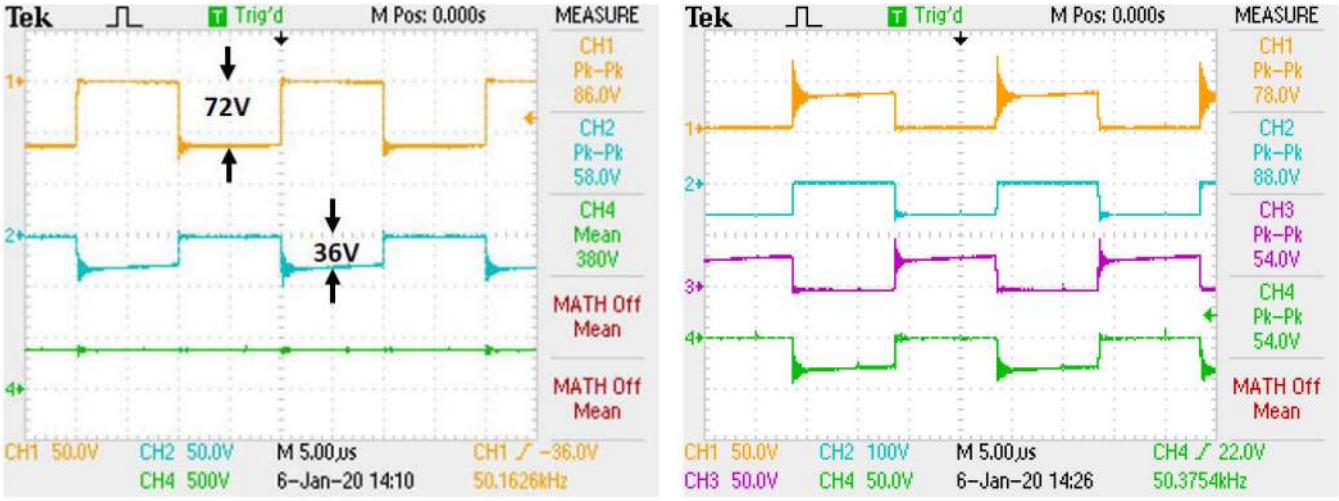


Fig. 8 *Voltage stress on D_1, D_2 compared with output voltage and correlated operation of D_1, D_2 with S_1, S_2, respectively*

(a) CH1, CH2: voltage stress on D_1 and D_2, respectively, and CH4: output voltage, ***(b)*** CH1, CH2, CH3 and CH4: voltage across S_1, D_1, S_2 and D_2, respectively

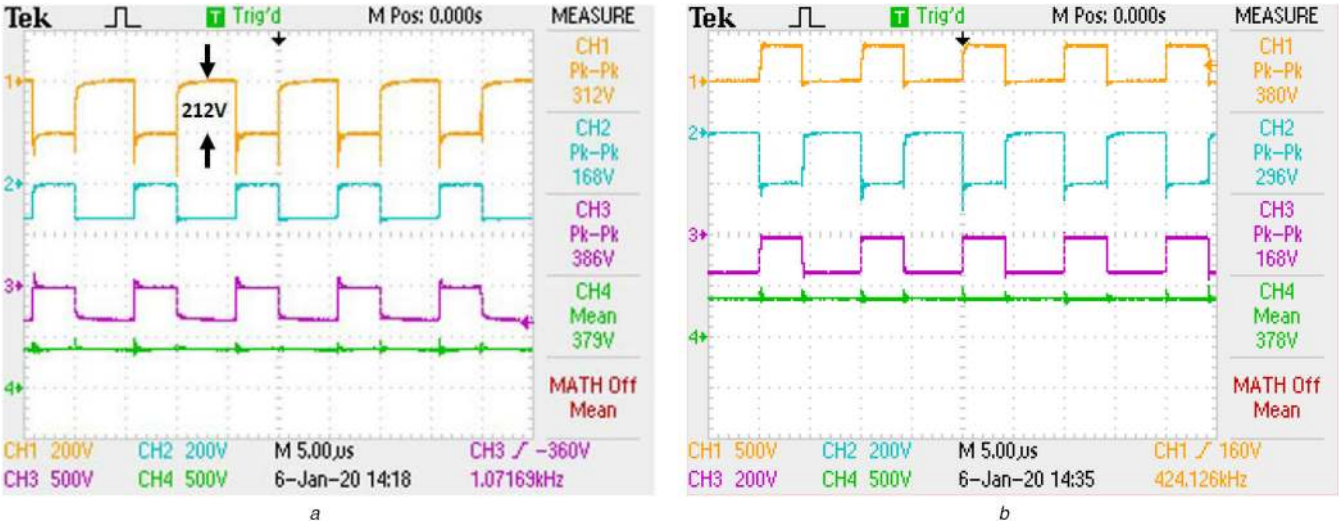


Fig. 9 *Voltage stress on diodes D_{3-A}, D_{3-B} and D_0 compared with V_0 and their operation correlated with S_3*

(a) CH1, CH2, CH3: voltage across D_{3-A}, D_{3-B} and D_0, respectively, and CH4: output voltage, ***(b)*** CH1, CH2, CH3: voltage stress on S_3, D_{3-A}, and D_{3-B}, respectively, and CH4: voltage at the output port

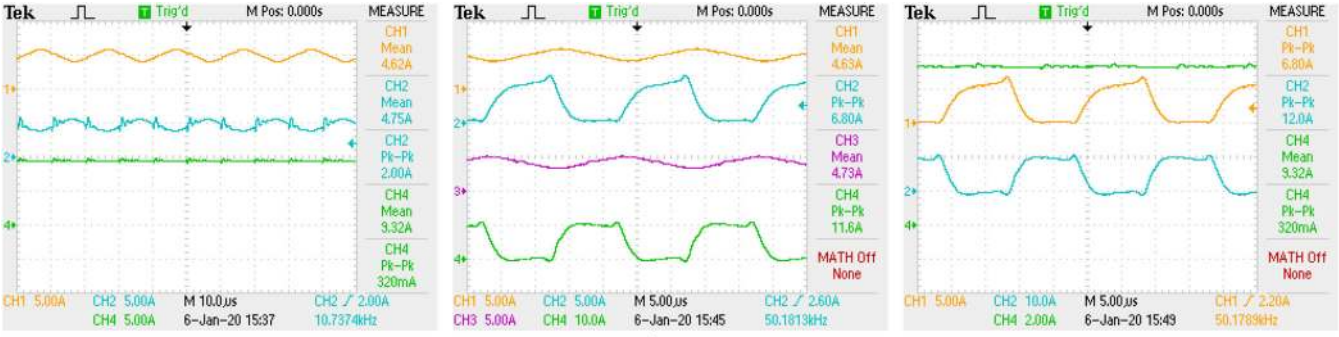
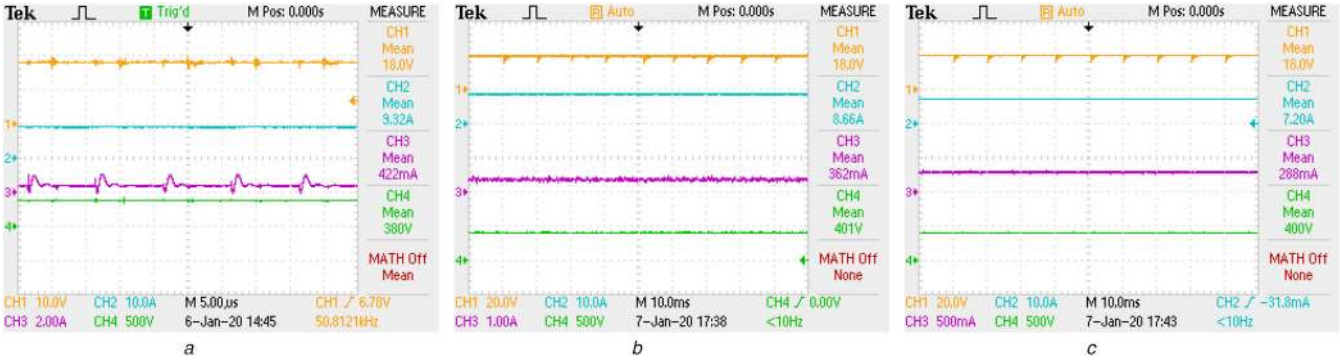


Fig. 10 *Oscillograms depicting the current through the inductors and switches*

(a) CH1 and CH2: current through L_1 and L_2, respectively, and CH4: input current, ***(b)*** CH1, CH2, CH3 and CH4: current through L_1, S_1, L_2 and S_2, respectively, ***(c)*** CH1, CH2: current through S_1 and S_2 and CH4: current drawn from the input supply

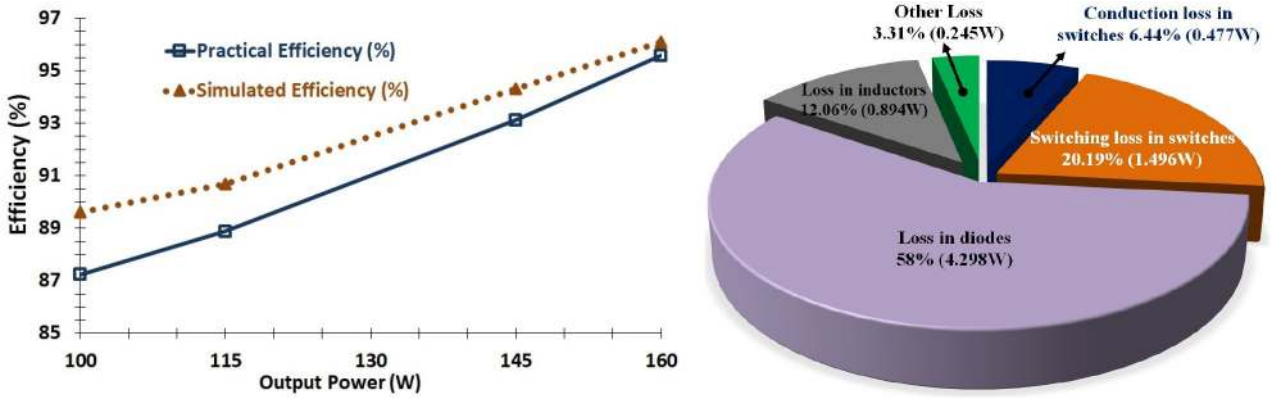
change in voltage gain is obtained by controlling δ_3. Resultantly, even during dynamic operating conditions, a ripple-free input current is easily realised.

The linear rise and fall of I_{L_1} and I_{L_2} is correlated with the operation of S_1 and S_2, respectively, and validated through Fig. 10*b*. While S_2 is ON (and S_1 is OFF), both the inductors L_1 and L_2 are functional through S_2. In other words, inductor L_1 transfers its stored energy to C_{Lift} and L_2 charges through S_2. Hence, S_2 is subjected to double the current stress magnitude as that of S_1 and clearly observed in Fig. 10*c*. Further, the practical current stress magnitudes are in accordance with their theoretically predicted counterparts. As observed in Fig. 10*c*, since interleaving



a *b* *c*

Fig. 11 *Experimental waveforms obtained from the prototype C³BC to determine the efficiency at*
(a) Full load condition (160 W) – input voltage and current (CH1 and CH2, respectively), load current (CH3) and output voltage (CH4), ***(b)*** Reduced load condition (145 W) – voltage and current at the input (CH1, CH2, respectively), load current (CH3) and load voltage (CH4), ***(c)*** Light load condition (115 W) – parameters captured in CH1–CH4 are same as in *(b)*



a *b*

Fig. 12 *Efficiency curves at the full-load condition and loss distribution profile*
(a) Full-load efficiency values during simulation and experimentation, ***(b)*** Power loss occurring in various components of the proposed C³BC

Table 3 Key parameters and their values which are used to compute various losses occurring in the proposed C³BC

Switch	$R_{sw,ON}$, mΩ	$I_{sw,RMS}$, A
S_1	3.1	3.267
S_2	3.1	6.597
S_3	49	2.514

Diode	I_{diode}, A
D_1, D_2	2.31
$D_{3\text{-}A}$, $D_{3\text{-}B}$	0.86
D_0	0.21

Inductor	$I_{inductor}$, A	$R_{inductor}$, mΩ	P_{iron}, W
L_1	4.63	8	0.09
L_2	4.73	8	0.09
L_3	2.11	9.1	0.06
L_4	1.06	12	0.25

mechanism is employed, current stress on S_1 is reduced. However, due to C_{Lift}, the total input current flows through S_2.

The oscillograms presented in Figs. 11*a–c* are used to determine the practical efficiency of the proposed C³BC at full-load (Fig. 11*a)* and slightly reduced loaded conditions (Figs. 11*b* and *c*). The proposed converter delivers the required and rated power of 160 W to the load at 95.58%. Since MOSFETs with low $R_{DS\text{-}ON}$ and diodes with low ON-state voltage drops are employed, the converter operates at good efficiency at rated condition. When the load on the C³BC is reduced to 145 W (Fig. 11*b*) and later to 115 W (Fig. 11*c*) the output voltage increases to about 400 V under open-loop. Expectedly, as in CBC and all boost-derived converters, since C_0 supplies a reduced load, it charges to a potential which is higher than the nominal voltage. In the proposed converter, considering the operation under light load, the voltage rating of C_0 is deliberately chosen to be higher than the nominal V_0. The efficiency of the proposed C³BC at 145 W power level is determined to be 93.12% while at 115 W and the converter operates at an efficiency of 88.88%. Fig. 12*a* presents the efficiency curve of the proposed C³BC.

The power loss dissipated across various components of the C³BC is computed as

$$P_{sw,loss} = I^2_{sw,RMS} \times R_{sw,ON} + P_{sw,ON} + P_{sw,OFF} \quad (31)$$

$$P_{diode\_loss} = V_{diode\_ON} \times I_{diode} \quad (32)$$

$$P_{inductor\_loss} = I^2_{inductor} \times R_{inductor} + P_{iron} \quad (33)$$

By referring to the manufacturers' datasheets, parameters like $R_{sw,ON}$ and V_{diode_ON} are obtained. The value of key parameters that are required to compute the loss occurring in various components is provided in Table 3. Substituting these values in (31)–(33), the loss distribution profile of the C³BC is obtained and portrayed in Fig. 12*b*. The total loss (P_{total_loss}) is computed by summing up the individual power losses and the theoretical efficiency value which is computed using (34) works out to 95.6%

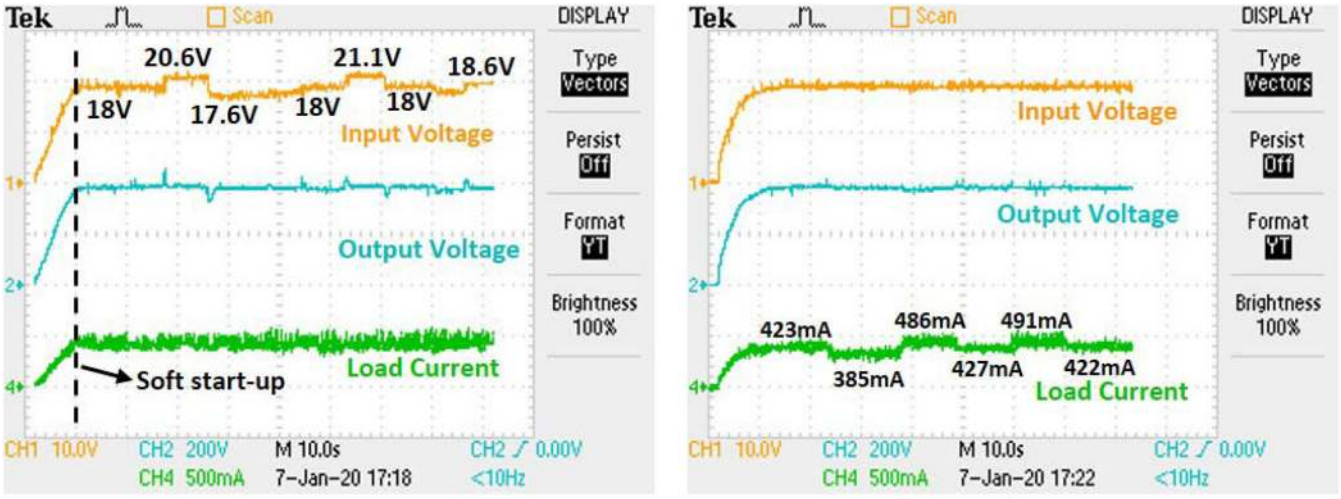


Fig. 13 *Waveforms depicting the dynamic response of the C³BC under the closed-loop condition*
(a) Demonstration of output voltage (CH2) regulation when the input voltage (CH1) varies, ***(b)*** Practical regulation of load voltage (CH2) when the load current (CH4) undergoes a step-change

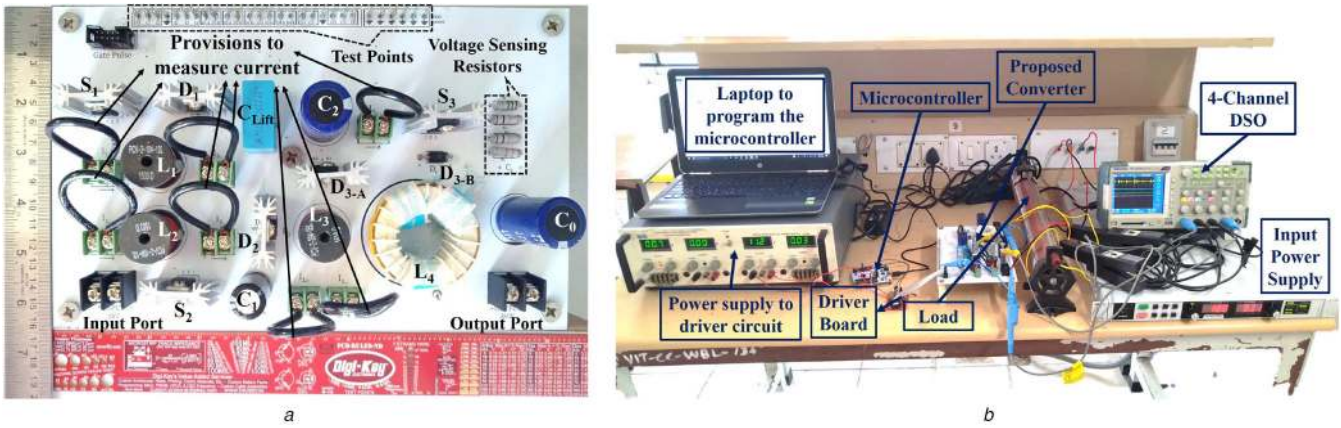


Fig. 14 *Photograph of the proposed C³BC*
(a) Top view, ***(b)*** Experimental setup used to validate the proposed concept

Table 4 Brief comparison of the C³BC with some recent converters

Attributes	Converters presented in references			
	[17]	[20]	[22]	Proposed C³BC
gain (*M*)	11.11	16.55	10.9	21.11
switch stress (% of V_0)	33	12.5	35.6	$S_{1,2}$ = 9.4, S_3 = 100
NCU	11	15	14	15
M/NCU	1.01	1.1	0.77	1.4

$$\eta = \frac{V_0 \times I_0}{(V_0 \times I_0) + P_{\text{total\_loss}}} \times 100\% \tag{34}$$

By implementing a simple PID controller, the output voltage obtained from the proposed C³BC is regulated to provide 380 V to the load when the input voltage and load current values undergo a step change.

Fig. 13*a* shows the output voltage profile of the proposed converter when the input voltage varies in the range between 17.6 and 21.1 V. The output voltage quickly settles down to the required 380 V. Fig. 13*b* portrays the load voltage which is regulated to provide a constant voltage of 380 V when the load current undergoes a step change. When the current is varied over 385 to 491 mA range, the output voltage remains constant. The photographs of the prototype converter and the experimental setup are depicted in Figs. 14*a* and *b*, respectively.

6 Benchmarking the proposed C³BC

In this section, the proposed C³BC is benchmarked by comparing some of its key performance attributes with the recent state of art converters. The converters that are chosen for comparison are presented in various references as outlined in Tables 4 and 5. The converters that are compared in Table 4 belong to single-switch variants while the proposed C³BC uses three switches. They employ CIs and some gain extension mechanisms to provide a voltage gain which is >10. The proposed C³BC is superior to the other converters in terms of its high-voltage gain capability and an excellent ratio of voltage gain (*M*) to the number of components used (NCU).

To obtain a detailed and fair comparison on the key performance attributes, converters which belong to the QBC family are picked and compared in Table 5.

6.1 Voltage gain (M)

The proposed C³BC provides the highest voltage gain of 21.11 while the converter presented in [28] provides the lowest voltage conversion ratio. Since a two-phase IBC with C_{Lift} is employed along with a cascaded QBC, the proposed converter offers the highest voltage gain value. The voltage gain of the converter used in [28] is dependent on the number of stackable switching stages. In the other converters presented in [23–25], the voltage gain depends on the turns ratio of the CIs. Notably, without using CIs, the proposed C³BC yields the highest voltage gain at safe duty

Table 5 Detailed comparison of the proposed C^3BC with state of art variants of QBC

Attributes	Converters presented in references				
	[23]	[24]	[25]	[28]	Proposed C^3BC
voltage gain (M)	8.3	16.6	12.7	5	21.1
duty ratio (δ)	0.45	0.66	0.58	0.55	$\delta_0 = 0.50$ $\delta_3 = 0.57$
no. of magnetic elements	2 (one simple inductor, one CI)	2 CIs	2 (one multi-winding CI, one simple inductor)	two simple inductors	four simple inductors
number of switches	1	1	1	1	3
number of diodes	5	5	5	3	5
NCU	11	12	14	8	15
M/NCU	0.75	1.38	0.98	0.625	1.40
voltage stress on switches as percentage of V_0 (V_{sw})	65	45	45.8	100	$S_{1,2} = 9.4$ $S_3 = 100$
voltage stress on diodes as percentage of V_0 (V_{diode})	Min = 21 Max = 80	Min = 15 Max = 37.5	Min = 21 Max = 52	Min = 44 Max = 100	Min = 9.4 Max = 100
input current ripple	yes	yes	yes	yes	no
gain extension technique adopted	QBC with CI	QBC with CI	QBC with CI and voltage doubler	stackable QBC	IBC with C_{Lift} cascaded to QBC

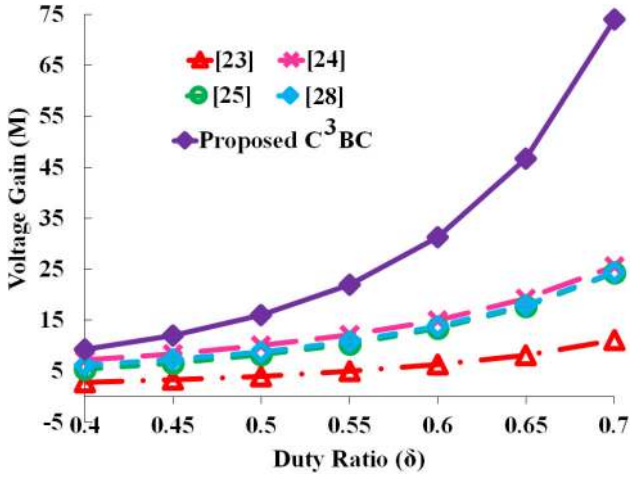


Fig. 15 *Voltage gain plot of the proposed C^3BC and some state of art QBC-based converters*

ratio values. The superior voltage gain capability of the proposed C^3BC is demonstrated using Fig. 15.

6.2 Voltage stress on semiconductor devices

The proposed converter uses three switches while all the other converters are single-switch versions. Two switches are located in stage 1 and are subjected to the least voltage stress value which is only 9.4% of V_0. The switches used in the other converters experience a fairly higher voltage stress level. In the converter presented in [28], due to the location of the switch in the QBC structure, its voltage stress magnitude is equal to the output voltage. Similarly, in the proposed C^3BC, S_3 experiences a voltage stress which is equal to V_0.

The converter described in [28] uses the least number of diodes; all the other converters use five diodes. The diodes employed in [24] are subjected a moderate voltage stress magnitude. The minimum voltage stress value on the diodes used in the converters presented in [23, 25] is about one-fifth of the output voltage. In the proposed C^3BC, one diode is subjected to the least voltage stress (9.4% of V_0). Since two stages are cascaded, the diodes experience a gradual increase in their voltage stress values. The maximum voltage stress is experienced by D_0 which is located very close to the output port. However, by carefully choosing fast-recovery diodes with low ON-state voltage drops, good operating efficiency value is retained.

6.3 NCU and M/NCU ratio

The converter presented in [28] uses the least number of components and provides a minimum voltage gain of 5. Hence, the M/NCU value is also found to be minimum and equal to 0.625. The converters elaborated in [23, 25] offer a moderate voltage gain and use 11 and 14 components, respectively. Their M/NCU values are also moderate. The converter described in [24] uses 12 components and yields a voltage gain of 16.6. The M/NCU value is high (1.38) and very close to the value obtained in the proposed C^3BC. Although its NCU value is the maximum, since it offers the maximum voltage gain, its highest M/NCU ratio is clearly justified.

6.4 Input current ripple

Due to the interleaving technique used in stage 1 and complimentary operation S_1 and S_2 with a fixed duty ratio of 0.5, the current ripple at the input side is completely eliminated in the proposed C^3BC. All the other converters draw pulsating current with ripples from the input side. The proposed C^3BC draws a smooth current from the input and lends itself for easier implementation of maximum power point tracking algorithms.

7 Conclusion

A high gain DC–DC converter which operates from 18 V input and yields 380 V to the load is presented in this paper. The proposed converter is built by employing interleaved structure, voltage-lift technique and cascading with a QBC. Since the two switches in the interleaved structure are operated with a fixed duty ratio of $\delta_0 = 0.5$ and with a phase shift of 180°, the proposed converter draws continuous and ripple-free current from the input. Moreover, by controlling the switch located in the QBC structure, the required voltage gain of 21.11 is achieved while drawing smooth current from the input. As the voltage conversion ratio is observed to be a cubic function of the value obtained from a CBC, the proposed converter easily delivers 160 W power to the output at 95.6% efficiency under experimental conditions. Two switches employed in the proposed C^3BC are subjected to minimal voltage stress of just 9.4% of V_0 despite practically providing the required high-voltage gain at safe duty ratio values. Likewise, except the output diode D_0, all the other fast-recovery diodes experience lower voltage stress levels only. Using a simple closed-loop control, the output voltage of the proposed converter is practically regulated.

Under dynamic conditions (input voltage and load current changes), the voltage output of the proposed C^3BC quickly settles down to the required 380 V level. Considering the beneficial features, the proposed C^3BC is a viable and promising converter for interfacing the low voltage PV input to the 380 V DC bus which is normally preferred in a DC microgrid.

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