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Non-isolated multi-input DC-DC converter with current sharing mechanism

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ABSTRACT

In this paper, a non-isolated multi-input DC-DC converter (MIC) topology is presented to integrate renewable energy sources (RES) with the load. The proposed MIC consists of two identical high gain DC-DC converters which are supplied from two sources. In each high gain converter, the required voltage gain to meet the standard DC bus voltage in a DC microgrid is obtained by cascading the output of a classical boost converter with two voltage multiplier cells. Further, ORing diodes are employed in the identical converters to facilitate current sharing between them. Moreover, when one of the RES is available, either of the identical converters provide the required load demand. The proposed concept is validated by conducting experimental results using a laboratory prototype. The operational modes, characteristic waveforms, design details, simulation and experimental results of the 36 V/380 V, 200 W DC-DC converter are also presented.

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Current sharing; multi-input converter; power converter; power electronics; voltage multiplier cells

I. Introduction

In recent times, renewable energy sources (RES) like photovoltaic (PV) systems, fuel cells, wind energy conversion systems, etc., are providing the much needed impetus to the existing electrical power system network. RES aids in meeting the ever increasing electrical energy demand besides reducing or meeting the stringent pollution norms (Ahmed et al., 2018).

Generally, the voltage output from RES (say PV systems) is low and requires to be stepped-up considerably before connecting the loads or integrating with the grid. Power electronic converters, particularly high gain DC-DC converters play a pivotal role in efficiently and smoothly utilising the available RES (Zhou et al., 2012).

The voltage gain capability of a classical boost converter (CBC) is restricted by the incremental loss across the semiconductor devices when the switch is operated at extreme duty ratio ($D > 0.8$). Therefore, gain extension cells like capacitor-diode voltage multiplier (Prudente et al., 2008), switched-inductor (Zhu et al., 2017), switched-capacitor (Ye et al., 2017), voltage-doubler (Hu & Gong, 2014) and voltage-lift technique (Chen et al., 2014) are adopted in conjunction with CBC to meet the required high voltage gain.

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Besides increasing the power output and sharing the load current equally between parallel connected converters (Shi et al., 2015), the utility level of RES enhances due to the adoption of multiple-input converters (MICs). A comprehensive review of various multi-input converters is presented in Khosrogorji et al., (2016); Rehman et al., (2015). Various methods to couple the output obtained from individual converters are discussed in Babaei et al. (2016). Guidelines for synthesising dual-input single-output circuits and designing power stages to achieve optimised efficiency are provided in Yang et al. (2015).

The use of multiple low power converters enables easier distribution of heat generated within them. The MIC proposed in Banaei et al. (2014) operates from two sources. The converter continues to operate and provides reduced output voltage (and limited voltage gain) if one source fails. The voltage gain of the MIC proposed in Mohammadi et al. (2019) is about 27 and fails to operate if any one input fails. The MIC proposed in Hamid Behjati & Davoudi (2013) operates from parallel input sources and provides parallel outputs during Buck mode. The converter proposed in Hou et al. (2016) suffers from high current stress. The simulation results of the converter presented in Vargil Kumar & Veerachary (2014) has low voltage conversion ratio of about 6 and operates for specific duty ratio condition. The MIC proposed in Erdal Irmak (2017) provides a voltage gain of 3.33, operates at low switching frequency and its output depends on both the input sources. The circuit proposed in Danyali et al. (2014) utilises minimum number of power switches and battery is autonomously charged or discharged to balance the power flow. Though some MICs have advantageous features like continuous input current and operate at low duty ratio values, their voltage gain is either limited (Babaei & Abbasi, 2016), (Ye Yuan-mao & Cheng, 2013) or gets reduced even further if one of the sources is unavailable (Haghighian et al., 2017; Kumar & Jain, 2013b).

The converter discussed in Deihimi et al. (2017) yields a voltage gain of about 8. Further, the voltage gain is extendable based on the number of input sources. Hence, the power handling and voltage gain capability of the converter is limited especially under fault condition. A non-isolated high step-up multi-input DC-DC converter proposed in (Faraji et al., 2019) acts as an interface for hybrid power sources. In the multi-input converter presented in (Vural et al., 2010), fuel-cell and ultra-capacitors are the sources. The converter topology is used to share the active power and stabilise the DC link voltage for the intended vehicular power supply. A non-isolated series multi-input DC-DC converter operating from three input sources is proposed in Hema Rani et al. (2019). The triple input converter yielded a maximum voltage conversion ratio of 9.16 when one input is available. An isolated MIC is proposed in Dusmez et al. (2016) for power sharing. The duty ratio provided to the switches is restricted based on the transformer design, inductors are operated in DCM mode and proper selection of inductors is important for power sharing.

In MICs, power sharing and regulating the output voltage is an interesting challenge. An effective switching strategy to regulate the output voltage obtainable from MIC is presented in Onwuchekwa & Kwasinski (2012). The converter proposed in Khadem Haghighian & Hosseini (2015) employs power management algorithm to regulate power flow and model-based predictive current control strategy to improve the dynamic response of the system. In the converter presented in Sijo et al. (2015, 2016), the proposed droop index algorithm with R_{droop} shifting minimises the circulating current and current sharing difference between the parallel converters. However, the voltage conversion ratio of the converter is about 4 only.

In parallel connected converters, voltage-current (V–I) droop control technique is essential to maintain the microgrid stability (Li & Fan, 2017). For power sharing purposes, several techniques like droop control (Anand & B G, 2012; J. B. Wang, 2011, 2012), common duty ratio control (Shi et al., 2015, 2012) and embedded virtual based I–V droop control are proposed (H. Wang et al., 2018).

As the voltage gain of the existing MICs is limited, this paper aims to design a high gain MIC. In this paper, a non-isolated multi-input DC-DC converter is proposed with high voltage gain of 10. The proposed converter has two identical structures connected in parallel. The proposed topology uses ORing diodes rated at full load current for (i) current sharing when both the sources are present and (ii) allows either of the power converter to operate carrying the full load current when any one of the source is present. The modes of operation, analysis, characteristic waveforms, design details, simulation and hardware results of the proposed converter are presented in the following sections.

Circuit description

Power circuit

Figure 1 shows the power circuit of the proposed converter. The proposed power circuit is aimed to operate from two sources and meet the load requirement through a common DC bus. The basic converter structure is obtained by cascading a classical boost converter

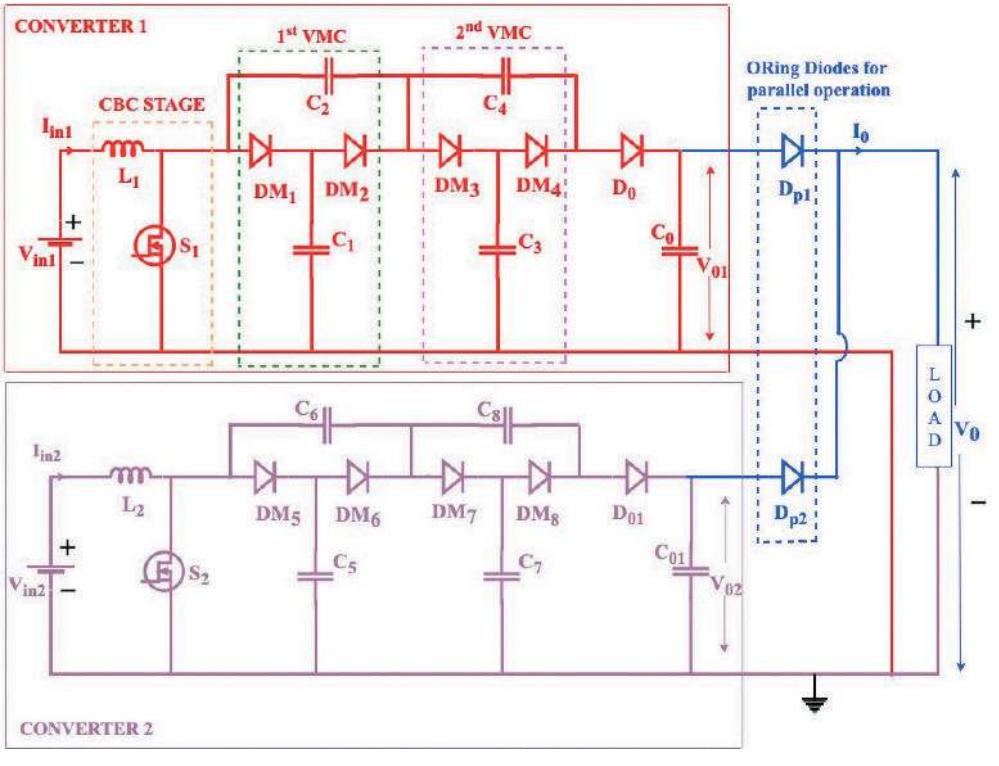

Figure 1. Power circuit of the proposed MIC.

(CBC) to two voltage multiplier cells (VMC). Two such structures are adopted to utilise the output voltage obtained from two RES, namely V_{in1} and V_{in2}. Converter 1 is powered from input source V_{in1} while Converter 2 is used to interface the input source V_{in2} to the load. The CBC stage in Converter 1 comprises inductor L_1 and switch S_1. The two VMC stages are formed using four diode-capacitor pairs namely DM_1-C_1, DM_2-C_2, DM_3-C_3 and DM_4-C_4. The output from Converter 1 is connected to the DC bus through the output diode D_0, output capacitor C_0 and ORing diode D_{p1}. The structure of Converter 2 is exactly similar to that of Converter 1. Thus, the two converters are operated in parallel so as to utilise the output from the two sources and supply the load demand. The operating principle is detailed in the next section.

Modes of operation

The operating principle of the proposed multi-input DC-DC converter (MIC) is explained using four modes in one switching cycle. As the operation of VMC stage is well understood from Prudente et al. (2008), the operation of Converters 1 and 2 alone is discussed in detail. For easier understanding, the following assumptions are made:

(i) All the switches and diodes are ideal.
(ii) All the passive elements are ideal and lossless.
(iii) Converters 1 and 2 operate in continuous conduction mode.

Mode 1(t_0 to t_1)

In Mode 1, switches S_1 and S_2 are turned ON at time $t = t_0$. As the switches are ON, current through the inductors L_1 and L_2 increase linearly. Therefore, the stored energy in the inductors also rises and the voltage across them builds up towards the supply voltage levels V_{in1} and V_{in2} respectively. The VMC stages aid in enhancing the voltage gain obtained from both the converters. As the switches are ON, diodes D_0 and D_{01} are reverse biased. The load requirement is taken care by the capacitors C_0 and C_{01}; the capacitors transfer their stored energy to the load through the diodes D_{p1} and D_{p2} respectively. Mode 1 comes to an end when the current through L_2 reaches its maximum value at time $t = t_1$. Figure 2a shows the circuit operation during Mode 1.

Mode 2(t_1 to t_2)

Mode 2 starts at time $t = t_1$, switch S_1 is continued to ON and S_2 is turned OFF. Since the switch S_1 remains ON, D_0 is still in reverse biased condition and the inductor L_1 continues to charge from V_{in1} and store energy. As the switch S_2 is OFF, D_{o1} is forward biased and load is connected to the second source V_{in2}. The current through the inductor L_2 starts decreasing and discharges the stored energy to capacitor C_{01} and load through D_{p2}. Capacitor C_o discharges the stored energy through D_{p1} to load. Mode 2 comes to an end when S_2 is turned ON at time $t = t_2$. Figure 2b shows the circuit operation during Mode 2.

Mode 3(t_2 to t_3)

Mode 3 is similar to Mode 1. At time $t = t_2$, switch S_2 is turned ON again. As the switches are ON, current through the inductors L_1 and L_2 raise linearly and inductors begin to store energy. As the switches are ON, diodes D_0 and D_{01} are reverse biased. Capacitors C_0 and

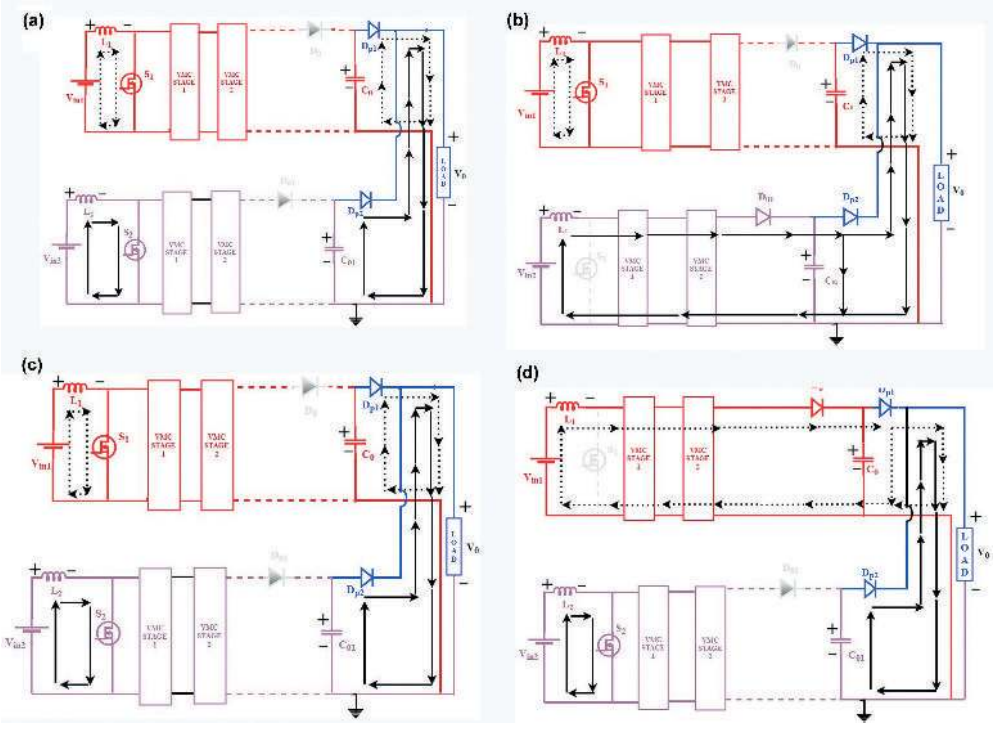

Figure 2. (a).Equivalent circuit in Mode 1. (b). Equivalent circuit for Mode 2, (c). Equivalent circuit during Mode 3. (d). Equivalent circuit during Mode 4.

C_{01} discharges through D_{p1} and D_{p2} to meet the load requirement. Mode 3 ends at time t = t_3. Figure 2c shows the equivalent circuit during Mode 3.

Mode 4(t_3 to t_4)

In Mode 4, S_1 is turned OFF and S_2 remains ON at time t = t_3. As the switch S_1 is OFF, D_o is forward biased and load is connected to the first source V_{in1}. Since the switch S_2 remains ON, D_{01} is still in reverse biased condition, the inductor L_2 still continues to charge from V_{in2} and store energy. The current through the inductor L_1 starts decreasing. Inductor L_1 transfers its stored energy to capacitor C_0 and load through D_{p1}. Capacitor C_{o1} discharges through D_{p2} to load. Mode 4 comes to an end when S_1 is turned ON at time t = t_4 and cycle repeats. Figure 2d shows the equivalent circuit during Mode 4. The operating modes are listed in Table 1 and characteristic waveforms are shown in Figure 3.

Table 1. Modes of operation of the converter.

	Devices in Converter 1					Devices in Converter 2				
Mode	S_1	DM_1, DM_3	DM_2, DM_4	D_0	Dp_1	S_2	DM_5, DM_7	DM_6, DM_8	D_{01}	Dp_2
Mode 1	ON	RB	FB	RB	FB	ON	RB	FB	RB	FB
Mode 2	ON	RB	FB	RB	FB	OFF	FB	RB	FB	FB
Mode 3	ON	RB	FB	RB	FB	ON	RB	FB	RB	FB
Mode 4	OFF	FB	RB	FB	FB	ON	RB	FB	RB	FB

FB-Forward Biased, RB-Reverse Biased

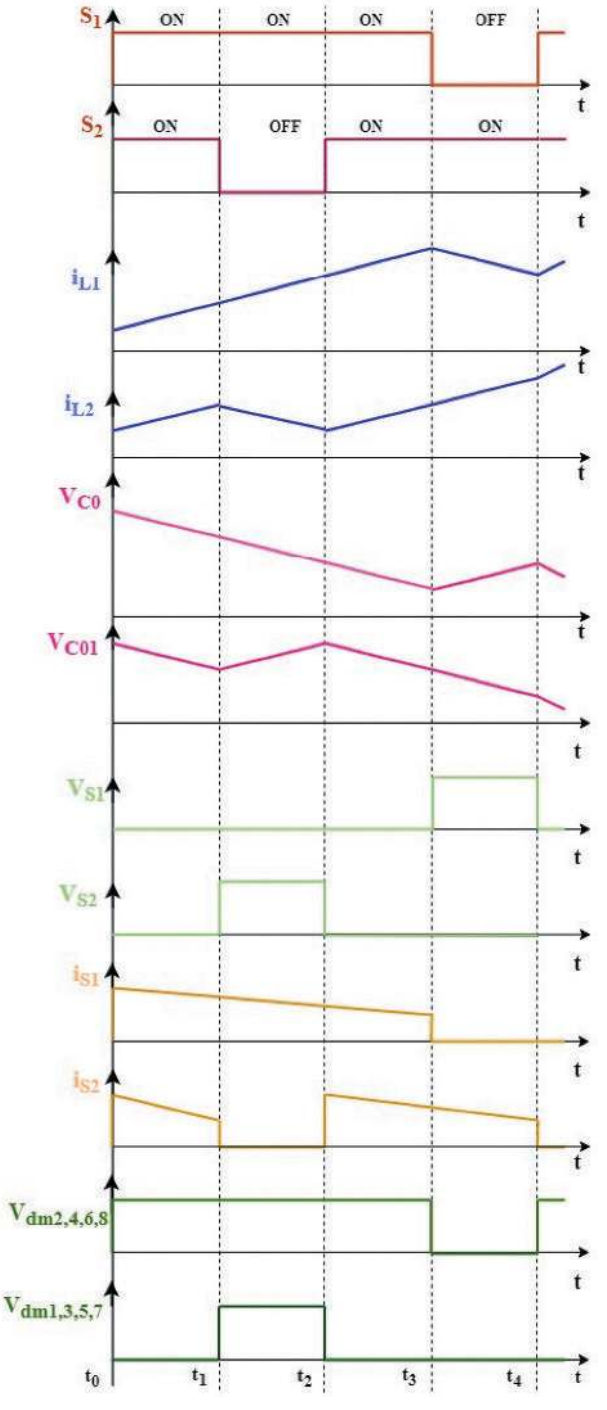

Figure 3. Characteristic waveforms of the proposed MIC.

Steady-state analysis and design

The proposed MIC is developed by operating two high gain DC-DC converters in parallel. The voltage gain from each high gain converter is obtained from the simple boost stage and VMCs. The voltage gain of each converter is derived by applying inductor volt-second balance over one cycle.

During Mode 2, S_1 is ON and S_2 is OFF. Applying KVL for the loop V_{in1}, L_1 and S_1 of converter 1,

$$V_{L1,ON} = V_{in1} \tag{1}$$

where $V_{L1,ON}$ is the voltage induced across L_1 when S_1 is ON and V_{in1} is the voltage magnitude of first source.

During Mode 4, S_1 is OFF and S_2 is ON. Applying KVL for the loop involving V_{in1}, L_1 and the CBC stage of Converter 1,

$$V_{L1,OFF} = V_{in1} - V_{CBC} \tag{2}$$

where $V_{L1,OFF}$ is the voltage induced across L_1 when S_1 is OFF and V_{CBC} is the voltage magnitude obtained at CBC stage of Converter 1.

Applying inductor volt-sec balance,

$$\int_0^T V_{L1}(t)dt = \int_0^{T_{ON}} V_{L1,ON}dt + \int_{T_{ON}}^{T_{OFF}} V_{L1,OFF}dt = 0 \tag{3}$$

where V_{L1} is the voltage induced across L_1.

Substituting (1) and (2) in (3), we get

$$V_{in1}T_{ON} + (V_{in1} - V_{CBC})T_{OFF} = 0 \tag{4}$$

where T_{ON} is the ON time of switch S_1, T_{OFF} is the OFF time of switch S_1 and T is the total time period.

Upon taking the average over one cycle,

$$\frac{V_{in1}T_{ON}}{T} + \frac{(V_{in1} - V_{CBC})T_{OFF}}{T} = 0 \tag{5}$$

Rearranging in terms of duty cycle

$$V_{in1}D_1 + (V_{in1} - V_{CBC})(1 - D_1) = 0 \tag{6}$$

Simplifying

$$\frac{V_{CBC}}{V_{in1}} = \frac{1}{1 - D_1} \tag{7}$$

where D_1 is the duty ratio of switch S_1.

The net voltage gain of Converter 1 is obtained by summing up the voltage gain of the CBC stage and two VMC cells. The gain of CBC stage is given by

$$M_c = \frac{1}{1 - D_1} \tag{8}$$

where M_c is gain of the CBC stage

The gain of VMC is given by

$$M_v = \frac{N}{1 - D_1} \tag{9}$$

where M_v is voltage gain at each VMC stage and N represents the number of VMCs. In the proposed MIC, since two VMCs are employed, $N = 2$. Combining equations (8) and (9), the overall voltage gain of Converter 1 is derived as

$$M_1 = M_c + M_v = \frac{1 + N}{1 - D_1} \tag{10}$$

where M_1 is gain of the Converter 1.

By substituting N = 2 in equation (10)

$$M_1 = \frac{3}{1 - D_1} \tag{11}$$

Similarly, Converter 2 is analysed using Modes 2 and 3. The overall voltage gain of Converter 2 is obtained as

$$M_2 = \frac{1 + N}{1 - D_2} \tag{12}$$

By substituting N = 2 in equation (12)

$$M_2 = \frac{3}{1 - D_2} \tag{13}$$

where D_2 = duty ratio of S_2 and M_2 is net voltage gain of Converter 2.

Since the two converters are connected in parallel, the total gain of the proposed MIC is given by

$$M = \frac{3}{1 - D} \tag{14}$$

where D represents the duty ratio of the switches employed in MIC and $D_1 = D_2 = D$.

The value of inductors are designed from basic principles and given by equations (15) and (16).

$$L_1 = \frac{V_{in1} D_1}{f \Delta i_{L_1}} \tag{15}$$

$$L_2 = \frac{V_{in2} D_2}{f \Delta i_{L_2}} \tag{16}$$

where f is the switching frequency and Δi_L represents the respective inductor ripple current.

The value of output capacitors depends on voltage ripple impressed across them and given by equations (17) and (18).

$$C_0 = \frac{I_0 D_1}{f \Delta v_0} \tag{17}$$

$$C_{01} = \frac{I_0 D_2}{f \Delta v_0} \tag{18}$$

where I_0 is output current and is Δv_0 the output voltage ripple.

The voltage stress on the switches S_1 and S_2 is given by

$$V_{S_1} = \frac{V_{in1}}{1 - D_1} \tag{19}$$

$$V_{S_2} = \frac{V_{in2}}{1 - D_2} \tag{20}$$

where $V_{S_1}$and V_{S_2} are the voltage stress magnitudes impressed across S_1 and S_2 respectively.

The diodes employed in VMC experience the same voltage stress and given by

$$V_{DM} = \frac{V_{in}}{1 - D} \tag{21}$$

Where V_{DM} is voltage across VMC stage diodes.

Simulation and hardware results

The proposed converter is simulated in MATLAB/Simulink and tested using a laboratory prototype version with specifications provided in Table 2. The photographs of the prototype converter and the experimental setup are shown in Figures 4 and 5 respectively. Gate pulses at the specified duty ratio and frequency are generated using PIC18F45K20 microcontroller.

The proposed MIC is analysed for open loop and closed loop using PI controller for the following cases: (i) when both the input sources are available and (ii) when only one of the input sources is available.

Case (i): when both the input sources are available: ($V_{in1} = V_{in2} = 36$ V)

a) For open loop: Figure 6 shows experimental results obtained from Converter 1. When S_1 is turned OFF, the energy stored in the input inductor L_1 is transferred to the multiplier capacitors C_1–C_3 through the diodes DM_1–DM_3 and output capacitor C_0 through the

Table 2. Specifications of the proposed MIC along with component details which were used for simulation and experimentation.

Parameter	Value
Input Voltage V_{in1}, V_{in2}	36 V
Output Voltage	380 V
Output Power	200 W
Switching Frequency	50 kHz
Duty ratio	0.716
Inductors L_1 and L_2	375µH, 10A
Voltage Multiplier Capacitors C_1, C_5	10µF, 250 V
Voltage Multiplier Capacitors C_3, C_7	10µF, 450 V
Voltage Clamping Capacitors C_2, C_4, C_6, C_8	10µF, 250 V
Output Capacitors	10µF, 450 V
Diodes DM_1 to DM_8	U15A40, 400 V, 15A
Output Diodes D_0, D_{01}	MUR 460, 400 V, 4A
ORing Diodes D_{p1}, D_{p2}	MUR 460, 400 V, 4A
Switches S_1, S_2	FQP34N20, 200 V, 31A

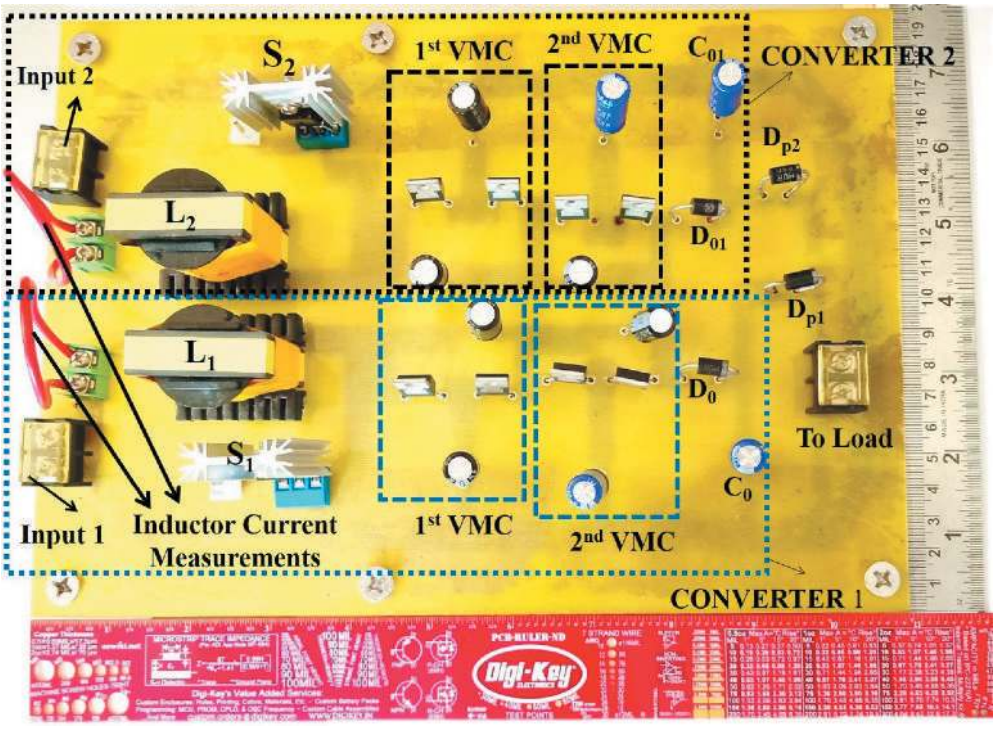

Figure 4. Photograph showing the top view of proposed converter with ORing diodes.

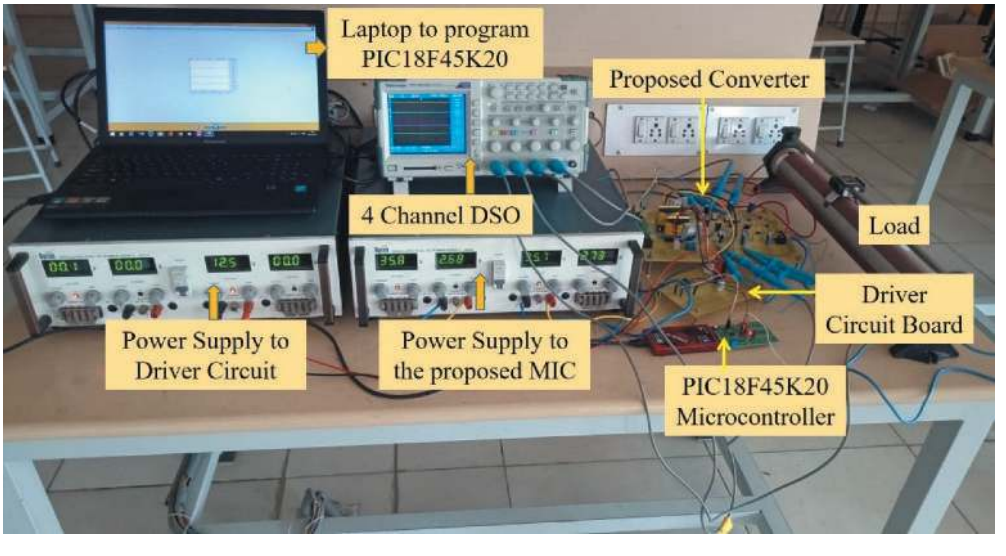

Figure 5. Photograph of the experimental setup used to test the proposed MIC.

output diode D_0. Since S_1 is OFF, the voltage stress experienced by S_1 is similar to that of a CBC and is equal to $\frac{V_{in1}}{1-D_1}$. In Figure 6, the experimental value of voltage stress on S_1 (CH2) and the voltage stress impressed on diode DM_1 (CH3) is observed to be 128 V which matches very closely with the analytically computed value. Further, the proper operation

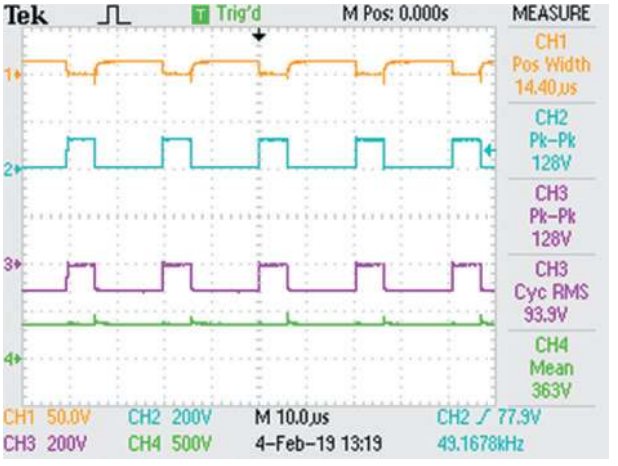

Figure 6. Experimental results of gate pulse to S_1 (CH1), voltage stress on S_1 (CH2), voltage stress on DM_1 (CH3) and output voltage (CH4).

of the switch and the odd numbered diode is also validated. When the gate pulse is applied to switch S_1, D_{M1} is OFF and D_{M2} is ON. Thus, a path is provided for $C1$ to transfer its stored energy to C_2.

Figure 7 shows the experimental results obtained from each VMC stage employed in Converter 1. When an input voltage of 36 V is applied, the output at first VMC stage is 128 V followed by 240 V at the second stage. The practical results are in accordance with the expected output voltage which is analytically presented in equation (11).

Figure 8 shows the experimental results of voltage across clamping capacitors. They are charged to a voltage magnitude given by $\frac{V_{in1}}{1-D_1}$.

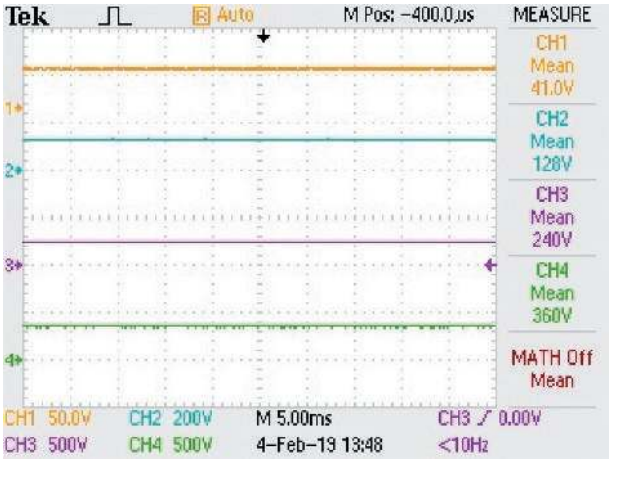

Figure 7. Experimental results obtained from Converter 1; input voltage V_1 (CH1), voltage across multiplier capacitors: C_1 (CH2), C_3 (CH3) and output voltage (CH4).

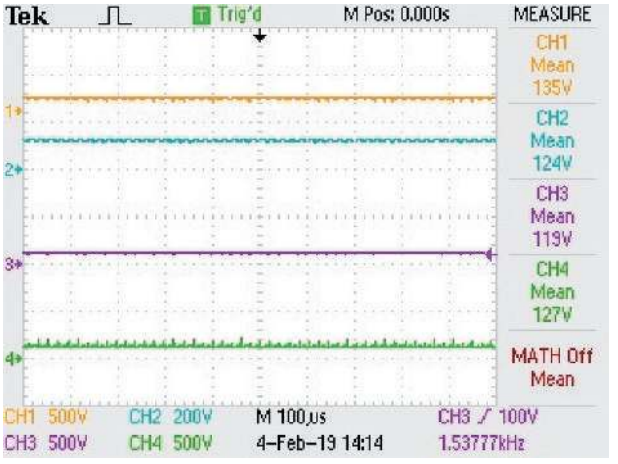

Figure 8. Experimental results showing the voltage across clamping capacitors: C_2 (CH1), C_4 (CH2), C_6 (CH3), C_8 (CH4).

Figures 9 and 10 respectively portray the voltage stress impressed on the odd and even numbered diodes employed in Converters 1 and 2. When S_1 and S_2 are ON, the output diodes D_0 and D_{01} are turned OFF due to the reverse voltage. Meanwhile, even numbered diodes DM_2, DM_4 conduct and transfer the energy stored in C_1 to C_2 and C_3 to C_4 respectively. Similarly, in Converter 2, multiplier diodes DM_6 and DM_8 conduct to charge the capacitors C_6 (charges from $C5$) and C_8 (charges from C_7). Based on the operating principle of the VMC network, the odd and even numbered diodes operate in a complimentary manner. Further, the voltage stress impressed across all the multiplier diodes is similar to that of the voltage gain obtainable from CBC. These two facts are clearly validated through Figures 9 and 10. Thus, the proposed voltage gain extension concept using VMC is validated.

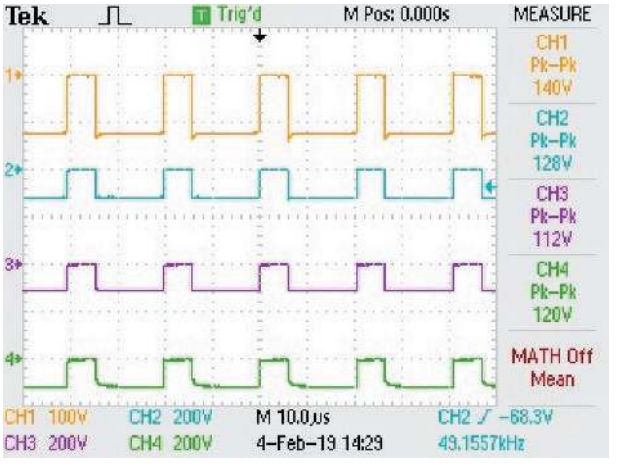

Figure 9. Practical results showing the voltage stress across odd numbered multiplier diodes employed in Converters 1 and 2: DM_1 (CH1), DM_5 (CH2), DM_3 (CH3) and DM_7 (CH4).

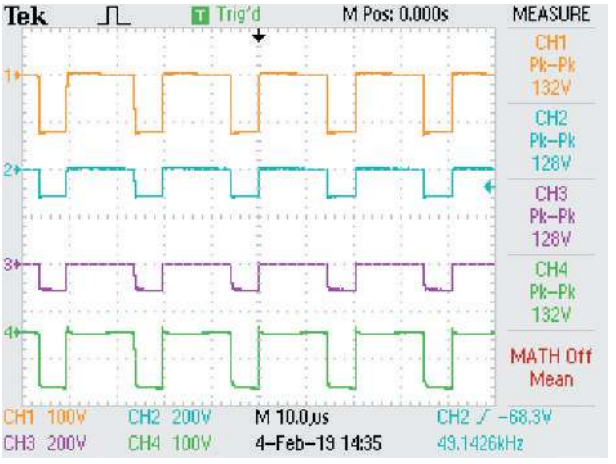

Figure 10. Experimental results of voltage stress on the even numbered diodes in Converters 1 and 2: DM_2 (CH1), DM_6 (CH2), DM_4 (CH3), DM_8 (CH4).

Figure 11 shows experimental results of the gate pulses of switches S_1, S_2 and input currents. The gate pulses are generated at 50 kHz with specified duty ratio. The gate pulses are generated in phase. For the two applied inputs (V_{in1} = 36 V, V_{in2} = 36 V), the corresponding input current drawn by Converter 1 is I_{in1} = 2.89 A (CH2) while Converter 2 draws I_{in2} = 2.85 A (CH4) from V_{in2}. Thus, the total current is almost equally shared by both Converters 1 and 2.

Figure 12 shows the experimental results of input voltages (V_{in1}, V_{in2}), output current (I_0) and output voltage (V_0). Two input voltages of 36 V are applied in parallel and an output voltage of 372 V is obtained. The practical value of total load current is realised to be 519 mA at the output side of the proposed MIC. Thus, the proposed MIC provides

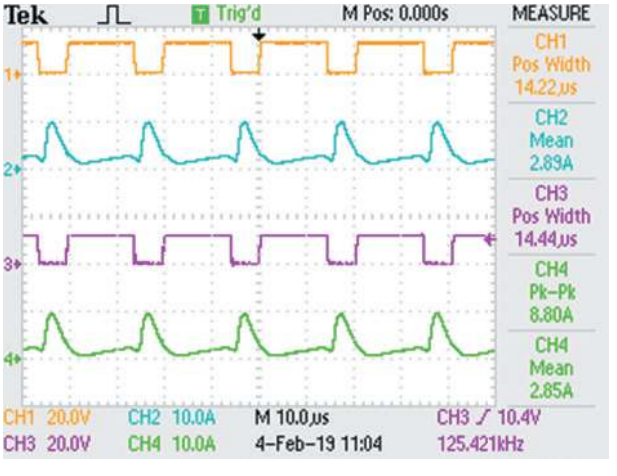

Figure 11. Experimental results showing the gate pulses to S_1 and S_2 (CH1, CH3 respectively) and current drawn by Converters 1 and 2 (CH2 and CH4 respectively).

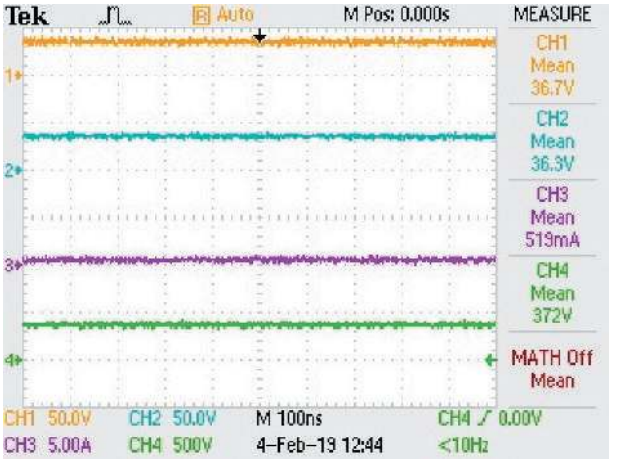

Figure 12. Experimental results to measure the full-load efficiency; input voltages V_{in1} and V_{in2} (CH1, CH2 respectively), total output current (CH3) and output voltage V_0 (CH4).

a voltage gain of 10.33 and delivers 192 W with a full-load efficiency of 93.43% under practical conditions.

B) For closed loop: The output voltage obtained from the proposed MIC is regulated and maintained constant at 380 V by implementing a simple closed-loop control. The actual output voltage is sensed and applied as feedback signal which is in turn compared with the reference value. Based on the error signal, PI controller generates an actuating signal to the sequence generator. The output from the sequence generator adjusts the duty ratio of the switches employed in each high gain DC-DC converter and controls the output voltage of the proposed MIC. By using trial and error method, the proportional and integral constants of the PI controller are set at $K_p = 30$ and $K_i = 3$, respectively.

Figure 13 shows the input voltages of sources 1 and 2 along with the input currents drawn by both the converters. Figure 14 shows output voltage, output current of each converter and total output current. The output current is equally shared among the converters by employing ORing diodes at the output of each converter followed the load causes load sharing among Converters 1 and 2.

The dynamic performance of the proposed MIC when the load varies is obtained and presented in Figures 15 and 16. The output voltage variation (under open loop condition) of the proposed MIC when the load varies from 75% to 125% of full load is shown in Figure 15. Under open-loop conditions, the output voltage undergoes oscillations and settles down. However, when closed-loop is implemented, the output voltage remains fairly a constant as depicted in Figure 16. Thus, the system is stable when there is a step up or step down in output load.

The dynamic response and the regulation characteristics of the prototype converter for step changes in input voltage and load current are portrayed in Figures 17 and 18, respectively. During start-up condition, the converter responds linearly and smoothly. The energy storage elements employed in the proposed converter absorb the initial spike or sudden change in output voltage during start-up condition and

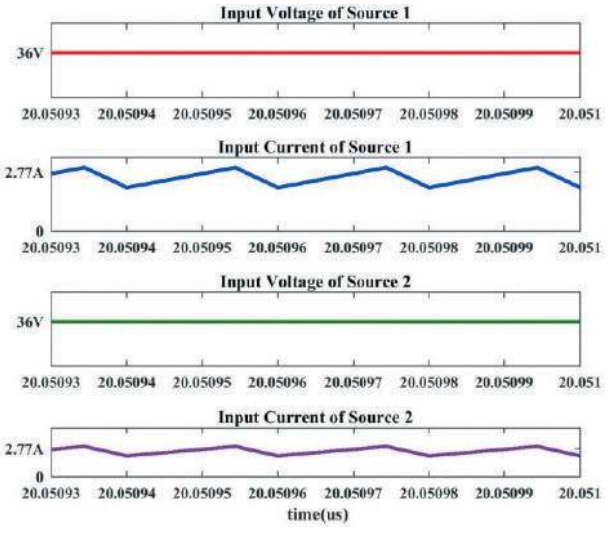

Figure 13. Simulated waveforms showing the input voltage and current of both sources.

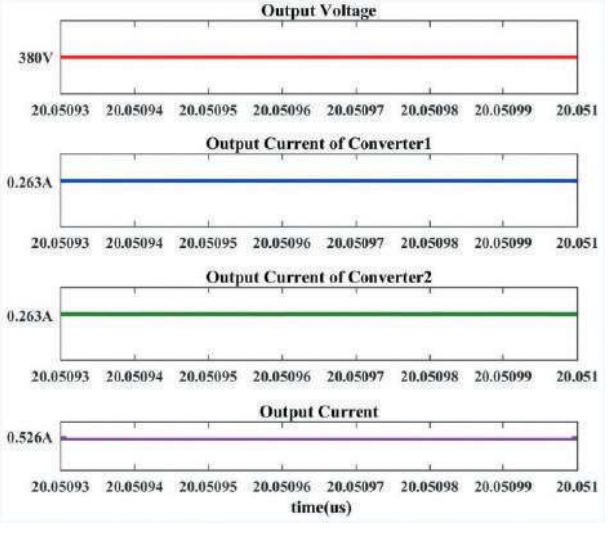

Figure 14. Simulated waveforms of the output parameters of Converters 1 and 2.

results in a fairly linear response. Expectedly, the load current also follows the load voltage behaviour as depicted in Figure 17. Whenever the input voltage undergoes a step change, due to the adopted closed-loop control strategy, the converter also responds quickly and settles down to the required 380 V level. Overall, when the input voltage varies over a range of 30 V to 38 V, the variation in output voltage is well within the acceptable ±5% range.

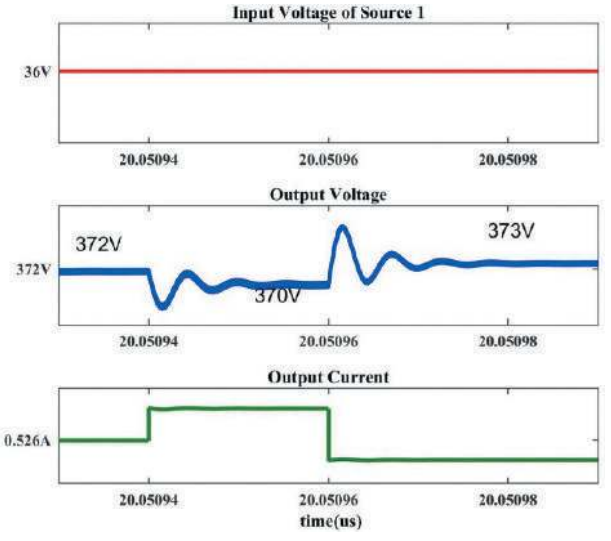

Figure 15. Dynamic performance of the proposed MIC under open-loop condition.

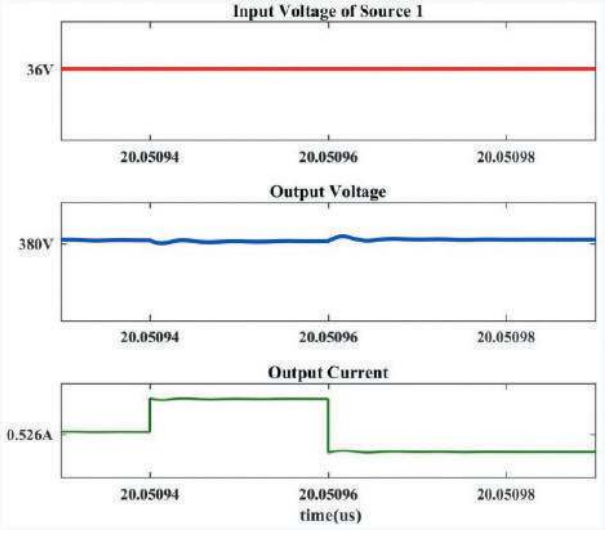

Figure 16. Closed-loop response of the proposed MIC.

The load current regulation characteristics of the experimented converter are depicted in Figure 18. The input voltage is maintained constant at 36 V and the load current is varied from 468 mA to 603 mA. When the load on the converter is increased, the load voltage is slightly reduced. The slight reduction exists only for a very short-time duration and the output voltage is regulated to the nominal value of 380 V swiftly. On similar lines, when the load current is decreased, the output voltage exhibits a slight increase before settling down to the required 380 V level.

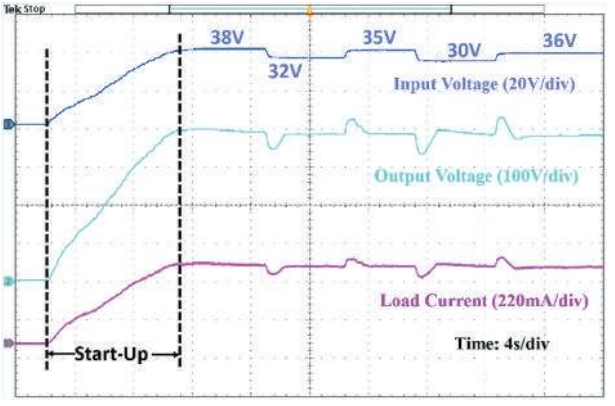

Figure 17. Response of the experimental prototype converter during start-up and for step change in input voltage.

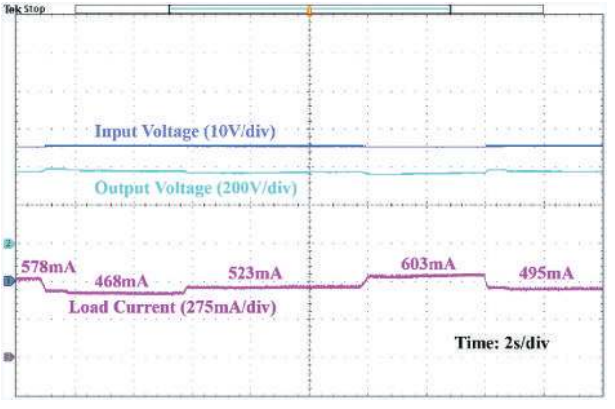

Figure 18. Dynamic response and regulation characteristics of the experimented prototype converter for step change in load current.

During both the load current variations (more and less than the rated current value), the swing in the output voltage remains within the acceptable band.

Case2: (i) when only one input source is available: (V_{in1} = 36 V, V_{in2} = 0 V)

a) For open loop: Figure 19 shows input voltage applied to converters 1 and 2 and their corresponding input currents. Converter 1 is supplied with 36 V at its input while Source 2 is nullified; no voltage is applied to Converter 2. Since Converter 1 alone acts, it draws 5.54A from the input. Figure 20 shows the output voltage, output currents of Converter 1 and 2 and load current waveforms. An output voltage of 372 V is obtained at the output port. As the load is designed to operate at 200 W power level, Converter 1 provides the required load current of 526 mA. However, as Converter 2 is not operating, its output current is 0A. Therefore the total load is supplied by Converter 1 alone.

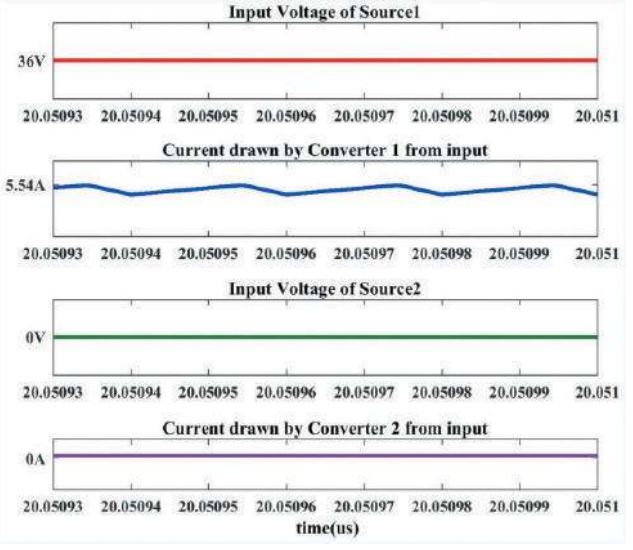

Figure 19. Simulated waveforms showing the voltage and current magnitudes of both sources.

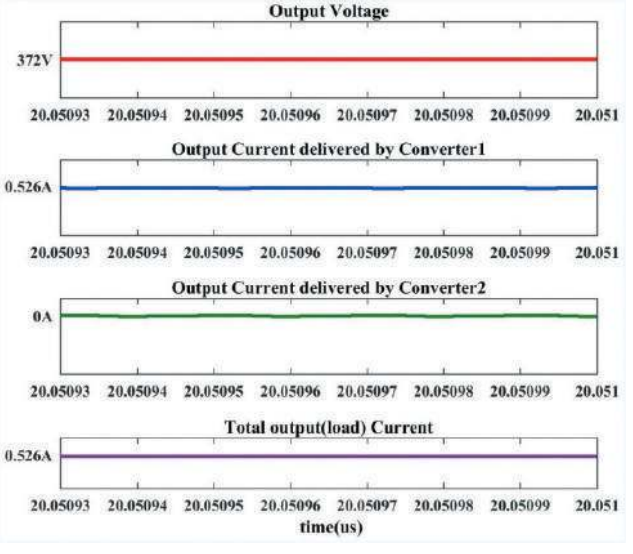

Figure 20. Simulated waveforms demonstrating the load supplied by Converter 1 and source 1 alone when source 2 is inactive.

b) For closed loop: Figures 21 and 22 show the simulated results under closed-loop condition when any one of the sources is unavailable (inactive). An input voltage of 36 V is applied from source 1 while source 2 is considered to be inactive. Converter 1 delivers the required load power at the desired output voltage level. Thus, the net load current is supplied by Converter 1 alone during both open and closed-loop conditions.

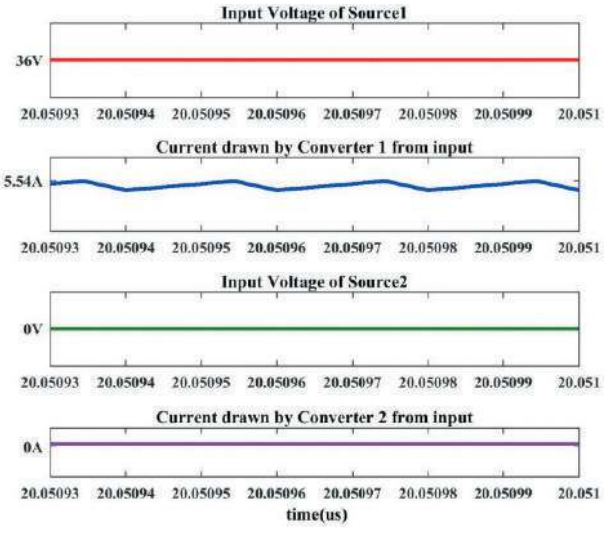

Figure 21. Waveforms corresponding to the two sources obtained during simulation.

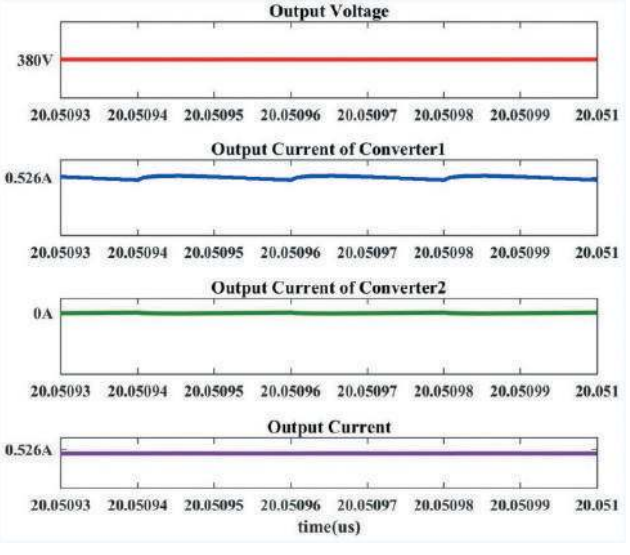

Figure 22. Simulated waveforms showing the load current being delivered by Converter 1 alone when source 2 is not available.

Performance comparison of proposed converter

High voltage transfer ratio

The proposed converter yields a high voltage gain of 10.33, operates at high switching frequency of 50 kHz and yields 372 V at the output. The proposed MIC uses ORing diodes to share the load current when both sources are active. Even when only one source is available, the full load is supplied by the other active converter. Under this circumstance

Table 3. Comparison of the proposed MIC with other similar converters.

Converters presented in	Attributes								
	A	B	C	D	E	F	G	H	I
(Banaei et al., 2014)	20 V, 30 V	95 V	$V_0 = \frac{V_{in2}}{1-D2} + \frac{D_1 D_2 V_{in1}}{(1-D_1)(1-D_2)}$	8	0.6, 0.5	25 kHz	$V_{s1} = \frac{V_{in1}}{1-D_1} V_{s2} = V_{out} + \frac{V_{in1} D_1}{1-D_1}$	$I_{S_2} = I_{L_2} + \frac{D_{2\max}}{L_2 f_s}(Vin_2 + \frac{D_1 V_{in1}}{1-D_1})$ $I_{S_1} = I_{L_1} + \frac{V_{in1} D_{1\max}}{2L_1 f_s}$	$I_{D_2} = I_{L_2} + \frac{D_{2\max}}{L_2 f_s}(Vin_2 + \frac{D_1 V_{in1}}{1-D_1})$ $I_{D_1} = I_{L_1} + \frac{V_{in1} D_{1\max}}{2L_1 f_s}$
(Kumar & Jain, 2013b)	24 V,12 V	53 V	$V_0 = \frac{V_1 d_1 + V_2 d_2}{1-d_3}$	8	0.6, 0.6, 0.6	10 kHz	$V_s = V_1 + V_2$	-	-
(Vargil Kumar & Veerachary, 2014)	12 V	24 V,72 V	$V_0 = \frac{[V_{g1}(1+d_1-2d_2) + V_{g2} d_2 (1-d_1)]}{(1-d_1)(1-d_2)}$	13	$d_1 > d_2$	-	$V_{s1} = \frac{V_{g1}(1-d_1-d_2)}{(1-d_1)}$ $V_{s2} = \frac{V_{g2}(1-d_1-d_2)}{(1-d_1)}$	$I_{S_1} = \frac{V_0(1+d_1-2d_2)}{2R(1-d_2)}$ $I_{S_2} = \frac{V_0 d_2 (1+d_2)}{R(1-d_2)}$	-
(Mohammadi et al., 2019)	15 V, 15 V	409 V	$V_0 = \frac{V_{in1}}{(1-d_1)^2} + \frac{V_{in2}}{(1-d_2)^2}$	18	0.73	40 kHz	$V_{s1} = \frac{V_{in1}}{(1-d_1)^2}$ $V_{s2} = \frac{V_{in2}}{(1-d_2)^2}$ $V_{s3} = 0$	-	- $I_D = \frac{I_{1\max}}{2C} \cos(\frac{1}{\sqrt{2L_1C}}t) - \frac{U_{c\min} - U_{in1}}{\sqrt{2L_1C}} \sin(\frac{1}{\sqrt{2L_1C}}t)$
(Hou et al., 2016)	33 to 50 V	400 V	$U_0 = \frac{3U_{in1}}{(1-D)} U_0 = \frac{3U_{in2}}{(1-D)}$	17	0.2 to 0.5	30 kHz	$U_{vps1} = \frac{U_{in1}}{(1-D)} U_{vps2} = \frac{U_{in2}}{(1-D)}$	$I_{S_2} = \frac{I_{1\max}}{2C} \cos(\frac{1}{\sqrt{2L_1C}}t) - \frac{U_{c\min} - U_{in1}}{\sqrt{2L_1C}} \sin(\frac{1}{\sqrt{2L_1C}}t)$ $I_{S_1} = \frac{3U_0}{R(1-D)} + \frac{U_{in1} D T_s}{2L_1}$	
(Babaei & Abbasi, 2016)	60 V, 40 V, 20 V	135 V	$V_0 = \frac{m}{(1-D_4)} [D_1 V_1 + (D_2 - D_1)V_2 + (D_3 - D_2)V_3]$	16	0.1, 0.3, 0.5, 0.6	10 kHz	-	-	-
(Faraji et al., 2019)	36 V, 42 V	400 V	$V_0 = \frac{(n+1)V_{IN}}{(1-D_{s1})}$	17	0.5	F_{s1} = 50 kHz, F_{s2} = 830 kHz	$V_{s1} = \frac{V_{in2}}{(1-D_{s1})}$ $V_{s2} = \frac{V_{in2}}{(1-D_{s1})} - V_{in1}$ $V_{s3} = \lvert V_{in2} - V_{in1} \rvert$	$I_{s1} = D_{s1} I_{in} I_{s2} = \frac{D_{s1} V_{in2}}{(1-D_{s1}) Z_0} I_{s3} = I_{in}$	$I_{D1} = I_{D2} = I_0$ $I_{D3} = (1-D) I_{in}$ $I_{D4} = \frac{D_{s1} V_{in2}}{(1-D_{s1}) Z_0}$
(Haghighian et al., 2017)	50 V, 24 V	95 V	$V_0 = \frac{d_1 V_{in1}}{(1-d_1)} + (d_1 + d_3) V_{ESS}$	11	-	40 kHz	$V_{s1} = V_0 + V_{c1}$ $V_{s2} = V_0 + V_{c1} - V_{ESS}$ $V_{s3} = V_{ESS}$	-	-
(Hema Rani et al., 2019)	18 V, 24 V, 30 V	110 V	$V_0 = \frac{V_1 d_1 + V_2 d_2 + V_3 d_3}{(1-d_3)}$	10	0.5	10 kHz	-	-	-

(*Continued*)

Table 3. (Continued).

	Attributes								
Converters presented in	A	B	C	D	E	F	G	H	I
(Deihimi et al., 2017)	22 V, 27 V	100 V	$V_0 = \frac{E_1}{(1-d_1)} + \frac{E_2}{(1-d_2)}$	11	0.5	15 kHz	$V_{S_1} = \frac{E_1}{(1-d_1)} V_{S_2} = \frac{E_2}{(1-d_2)}$	$I_{S_1} = I_{L_1}\sqrt{d_1} I_{S_2} = \sqrt{\frac{I_{L_2}^2 d_2 + I_{L_2} I_0 + \frac{2V_{ap} I_0}{3(t_D+t_S)}}{}}$	$I_{D_1} = \frac{I_0}{\sqrt{(1-d_1)}} I_{D_2} = \sqrt{\frac{2V_{ap} I_0}{3(t_D+t_S)}} I_{D_3} = \frac{I_0}{\sqrt{(1-d_2)}}$
proposed	36 V,36 V	372 V	$\frac{V_0}{V_{in1}} = \frac{V_0}{V_{in2}} = \frac{3}{1-D_1} = \frac{3}{1-D_2}$	26	0.716	50 kHz	$V_{s1} = \frac{V_{in1}}{1-D_1} V_{s2} = \frac{V_{in2}}{1-D_2}$	$I_{S_1} = I_{in1} I_{S_2} = I_{in2}$	$I_{DM} = \frac{}{I_{in}(1-D)}$ $I'_{DM} = \frac{}{I_{in}(2-D)}$

A – input voltage (V_{in}), B – output voltage (V_0), C – output voltage expression when both sources are available, D – total component count, W, E – duty ratio (D), F – switching frequency, G – voltage stress on switch, H – Current stress on switch, I – current stress for diodes.

also, the proposed MIC provides the required voltage gain output voltage. The ability of the proposed MIC to operate satisfactorily even when only one source is available is one of its main advantages.

The voltage gain for the converter in Banaei et al. (2014) varies from 3 to 5 while the converter presented in Kumar & Jain (2013b) operates with a voltage conversion ratio in the range of 2 to 5. The converter proposed in Vargil Kumar & Veerachary (2014) has low-voltage gain of 6. The converter presented in Hou et al. (2016) has a moderate voltage gain ranging between 8 and 12. The output voltage of converters presented in Banaei et al. (2014), (Deihimi et al., 2017; Haghighian et al., 2017; Hema Rani et al., 2019; Mohammadi et al., 2019) and Kumar & Jain (2013b) reduce if any one of the input sources is unavailable.

Voltage stress on the switches

The voltage stress across switches for the converter presented in (Banaei et al., 2014; Mohammadi et al., 2019) is half of its output voltage and for the converter presented in Kumar & Jain (2013b) is 70% of its output voltage. The voltage stress experienced by the switches employed in the proposed MIC is only 33.33% of the output voltage. Moreover, the proposed MIC yields a voltage gain of 10.33 and provides the required output voltage even if any one of the sources become inactive.

Figure 23 shows plots for various parameters like voltage gain, voltage stress across switch and VMC diodes under simulation and experimental conditions. The switches are operated at 71% duty ratio to achieve the required voltage gain of 10.33. The voltage stresses across switch and diodes are 127 V under simulation and 128 V under experimentation. The experimental results match very closely with the simulated values (Table 4) and validate the proposed concept.

Figure 24 demonstrates the progressive increment in voltage gain when traversing from the input port to the output port through the VMC stages. The voltage gain values obtained at each VMC stage during simulation and experimentation are in accordance with each other.

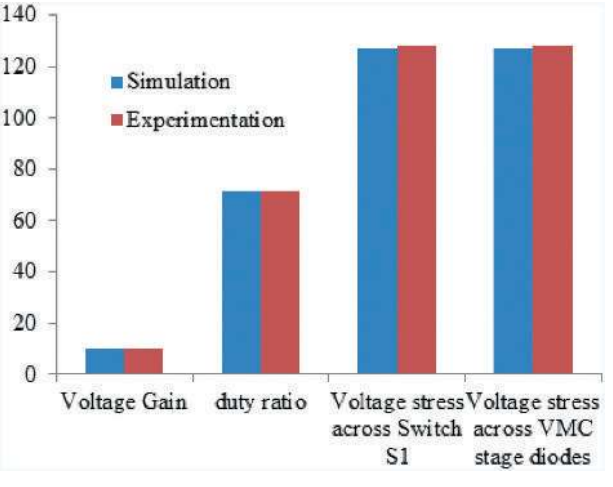

Figure 23. Plots showing the voltage gain, duty ratio, voltage stress on S_1 and VMC diodes employed in the proposed MIC under simulation and experimentation.

Table 4. Comparison of simulation and experimental results of the proposed MIC.

S.No.	Parameter	Simulation results	Experimental results
1	Input Voltage	36 V	36 V
2	Output at VMC stage 1	127 V	128 V
3	Output at VMC stage 2	254 V	240 V
4	Converter Output Voltage	372 V	372 V
5	Voltage Gain	10.33	10.33
6	Duty ratio	0.716	0.716
7	Voltage stress across Switch S_1	127 V	128 V
8	Voltage stress across VMC stage diodes	127 V	128 V

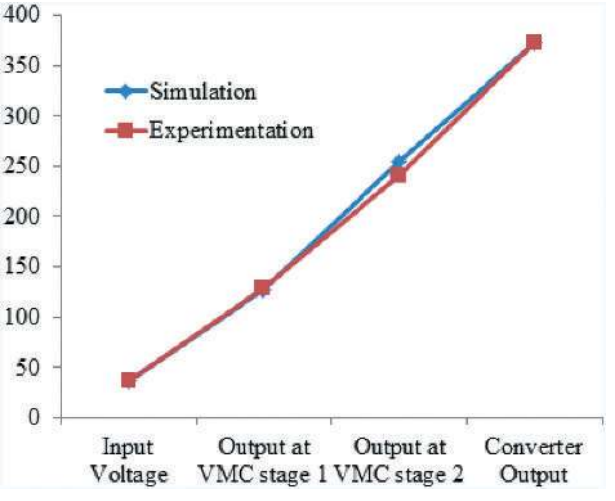

Figure 24. Graphical plot showing the progressive increment in voltage levels obtained at each stage of the proposed MIC.

Reliability

Due to the intermittent nature of RES, reliability of the overall system needs to be evaluated carefully. Further, the use of semiconductor devices in the power electronic converters affects the overall reliability. In the proposed MIC, each converter consists of one CBC and 2 VMCs. For parallel operation, ORing diodes are used. The proposed converter is supplied from two parallel sources and is designed to handle 200 W at the output. When both the sources are available, both the individual converters share the total load power. However, when any one of the input fails, the load is supplied by the other active converter. The active converter delivers the required power of 200 W to the load at 380 V (Figure 22). Thus, the overall system continues to operate reliably and satisfactorily.

Challenges and opportunities

Though multi-input converters enhance the overall power handling capability of the system (due to paralleling), some challenges do exist. For equal load sharing between the multiple converters, control signals must be perfectly synchronised. Asynchronous control leads to load mismatch between the multiple converters. Consequently, the

semiconductor devices may be subjected to additional voltage and current stress besides increment in temperature. Thus, the overall reliability of the system is reduced. Novel synchronising mechanisms which are redundant and efficient may be employed in future to enhance the reliability of the overall system.

Loss analysis of the proposed converter

In this section, the loss occurring across all the components employed in the proposed MIC are theoretically analysed. The power loss across the main switches S_1 and S_2 are given by equations (22)-(24).

$$P_{loss-in-switches} = P_{loss-conduction} + P_{loss-switching} \tag{22}$$

$$P_{loss-conduction} = I_{sw-RMS}^2 * R_{sw-ON} \tag{23}$$

$$P_{loss-switching} = P_{sw-ON} + P_{sw-OFF} = \frac{V_{in} I_0 t_{dON} f_{sw}}{2} + \frac{V_{in} I_0 t_{dOFF} f_{sw}}{2} \tag{24}$$

Since fast-recovery diodes are employed, the loss during switching (turn ON and turn OFF) interval is generally very less and insignificant. Therefore, the power loss in diodes is computed from equation (25).

$$P_{loss-diode} = V_{d-ON} * I_{d-AVG} + \frac{V_{d-OFF} * I_{rr}}{2} \tag{25}$$

The power loss experienced by the inductors comprises the copper loss and iron loss as given by equation (26).

$$P_{loss-inductor} = I_L^2 * R_L + P_{iron} \tag{26}$$

where $P_{loss\text{-}in\text{-}switches}$ is total power loss in switches, $P_{loss\text{-}conduction}$ is power loss in switches during conduction, $P_{loss\text{-}switching}$ is power loss in switches during switching, $P_{sw\text{-}ON}$ and $P_{sw\text{-}OFF}$ are power loss in switches during turn ON and OFF process, I_{sw} is current flowing through the switches, R_{sw} is the resistance of switches, $P_{loss\text{-}diode}$ is power loss occurring in diodes, $P_{loss\text{-}inductor}$ is power loss in inductors, I_d and I_L are currents flowing through diode and inductor, respectively.

The appropriate values which are necessary to compute the losses are obtained from the datasheet of each semiconductor device. The stray resistance of the custom-made inductors is practically measured. Using these values, the loss distribution profile is obtained and depicted in the pie-chart in Figure 25.

Conclusion

In this paper, a non-isolated multi-input DC-DC converter was designed, simulated and experimentally verified. The proposed MIC was intended to operate from two sources. The proposed converter used ORing diodes whose forward resistances helped in sharing the load current of the individual converters. When the converter was powered from two equal voltage sources of 36 V each, an output voltage of 372 V and output current of

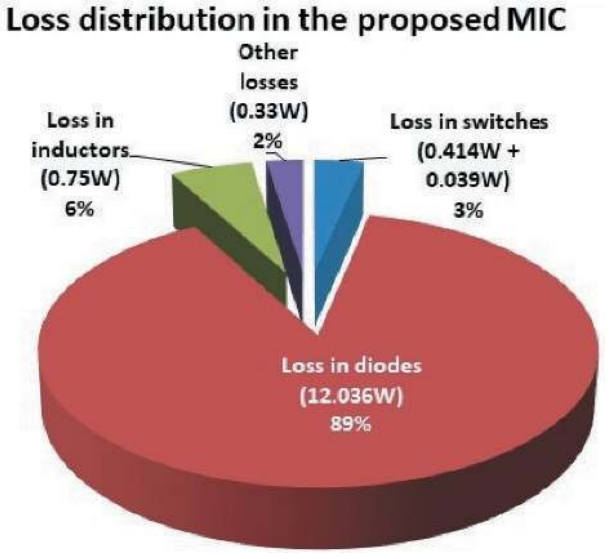

Figure 25. Loss distribution profile of the proposed MIC.

519 mA were obtained translating to a practical power output of 193 W. When one source was not available (V_{in2}), the other active source (V_{in1}) delivered the required load power through its power electronic interface (Converter 1). The proposed converter provided the required voltage gain of 10.33. The voltage and current stress on the switches was only a fraction of the output voltage (34.14% of V_o) and input current (10.65% of I_{in}) respectively. Based on the experimental results obtained from the prototype MIC, the proposed converter is expected to serve as an appropriate interface between the RES and the load or common DC bus.

Disclosure statement

No potential conflict of interest was reported by the authors.

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References

Ahmed, I. M. A., Mahmoud, A. S., & Essam, E. M. M. (2018). Modified efficient perturb and observe maximum power point tracking technique for grid-tied PV system. *International Journal of Electrical Power and Energy Systems*, (99), 192–202. https://doi.org/10.1016/j.ijepes.2017.12.029

Anand, S., & Fernandes, B. G. (2012). Modified droop controller for paralleling of dc – Dc converters in standalone dc system. *IET Power Electronics*, *5*(6), 782–789. https://doi.org/10.1049/iet-pel.2011.0346

Babaei, E., & Abbasi, O. (2016). Structure for multi-input multi-output dc – Dc boost converter. *IET Power Electronics*, *9*(1), 9–19. https://doi.org/10.1049/iet-pel.2014.0985

Babaei, E., Abbasi, O., & Sakhavati, S. (2016). An overview of different topologies of multi-port dc/dc converters for dc renewable energy source applications. *2016 13th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, ECTI-CON 2016*, Chiang Mai, Thailand. *2*, 1–6.

Banaei, M. R., Ardi, H., Alizadeh, R., & Farakhor, A. (2014). Non-isolated multi-input – Single-output DC/DC converter for photovoltaic power generation systems. *IET Power Electronics*, *7*(11), 2806–2816. https://doi.org/10.1049/iet-pel.2013.0977

Behjati, H., & Davoudi, A. (2013). A multiple-input multiple-output DC – DC converter. *IEEE Transactions on Industry Applications*, *49*(3), 1464–1479. https://doi.org/10.1109/TIA.2013.2253440

Chen, Y., Tsai, M., & Liang, R. (2014). DC – DC converter with high voltage gain and reduced switch stress. *IET Power Electronics*, *7*(10), 2564–2571. https://doi.org/10.1049/iet-pel.2013.0589

Danyali, S., Hosseini, S. H., & Gharehpetian, G. B. (2014). New extendable single-stage multi-input DC – DC/AC boost converter. *IEEE Transactions on Power Electronics*, *29*(2), 775–788. https://doi.org/10.1109/TPEL.2013.2256468

Deihimi, A., Mir, E. S. M., & Iravani, R. (2017). A new multi-input step-up DC – DC converter for hybrid energy systems. *Electrical Power Systems Research*, *149*, 111–124. https://doi.org/10.1016/j.epsr.2017.04.017

Dusmez, S., Li, X., & Akin, B. (2016). A new multi-input three-level DC/DC converter. *IEEE Transactions on Power Electronics*, *31*(2), 1230–1240. https://doi.org/10.1109/TPEL.2015.2424246

Erdal Irmak, N. G. (2017). Application of a boost based multi-input single-output DC/DC converter. *6th International Conference on Renewable Energy Research and Applications*, San Diego, CA, USA. *5*, 1–7.

Faraji, R., Adib, E., & Farzanehfard, H. (2019). Soft-switched non-isolated high step-up multi-port DC-DC converter for hybrid energy system with minimum number of switches. *International Journal of Electrical Power and Energy Systems*, *106*(March 2019), 511–519. https://doi.org/10.1016/j.ijepes.2018.10.038

Haghighian, S. K., Tohidi, S., Feyzi, M. R., & Mehran, S. (2017). Design and analysis of a novel SEPIC-based multi-input DC/DC converter. *IET Power Electronics*, *10*(12), 1393–1402. https://doi.org/10.1049/iet-pel.2016.0654

Hema Rani, P., Navasree, S., George, S., & Ashok, S. (2019). Fuzzy logic supervisory controller for multi-input non-isolated DC to DC converter connected to DC grid. *International Journal of Electrical Power and Energy Systems*, *112*, 49–60. https://doi.org/10.1016/j.ijepes.2019.04.018

Hou, S., Chen, J., Sun, T., & Bi, X. (2016). Multi-input step-up converters based on the switched-diode-capacitor voltage accumulator. *IEEE Transactions on Power Electronics*, *31*(1), 381–393. https://doi.org/10.1109/TPEL.2015.2399853

Hu, X., & Gong, C. (2014). A high voltage gain DC – DC converter integrating coupled-inductor and diode – capacitor techniques. *IEEE Transactions on Power Electronics*, *29*(2), 789–800. https://doi.org/10.1109/TPEL.2013.2257870

Khadem Haghighian, S., & Hosseini, S. H. (2015). A novel multi-input DC/DC converter with a general power management strategy for grid connected hybrid PV/FC/battery system. *6th Annual International Power Electronics, Drive Systems, and Technologies Conference, PEDSTC 2015 (February)*, Tehran, Iran, 1–6.

Khosrogorji, S., Ahmadian, M., Torkaman, H., & Soori, S. (2016). Multi-input DC/DC converters in connection with distributed generation units – a review. *Renewable and Sustainable Energy Reviews*, *66*, 360–379. https://doi.org/10.1016/j.rser.2016.07.023

Kumar, L., & Jain, S. (2013a). A multiple source DC/DC converter topology. *International Journal of Electrical Power and Energy Systems*, *51*, 278–291. https://doi.org/10.1016/j.ijepes.2013.02.020

Kumar, L., & Jain, S. (2013b). Multiple-input DC/DC converter topology for hybrid energy system. *IET Power Electronics*, *6*(8), 1483–1501. https://doi.org/10.1049/iet-pel.2012.0309

Li, Y., & Fan, L. (2017). Stability analysis of two parallel converters with voltage – current droop control. *IEEE Transactions on Power Delivery*, *32*(6), 2389–2397.doi:10.1109/TPWRD.2017.2656062.

Mohammadi, S., Dezhbord, M., Babalou, M., Azizkandi, M. E., & Hosseini, S. H. (2019). A new non-isolated multi-input dc-dc converter with high voltage gain and low average of normalized

peak inverse voltage. *2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC)*, Shiraz, Iran, Iran. 515–520.

Onwuchekwa, C. N., & Kwasinski, A. (2012). A modified-time-sharing switching technique for multiple-input DC – DC converters. *IEEE Transactions on Power Electronics*, *27*(11), 4492–4502. https://doi.org/10.1109/TPEL.2011.2180740

Prudente, M., Pfitscher, L. L., Emmendoerfer, G., Romaneli, E. F., & Gules, R. (2008). Voltage multiplier cells applied to non-isolated DC-DC converters. *IEEE Transactions on Power Electronics*, *23*(2), 871–887. https://doi.org/10.1109/TPEL.2007.915762

Rehman, Z., Al-Bahadly, I., & Mukhopadhyay, S. (2015). Multiinput DC-DC converters in renewable energy applications - an overview. *Renewable and Sustainable Energy Reviews*, *41*, 521–539. https://doi.org/10.1016/j.rser.2014.08.033

Shi, J., Liu, T., Cheng, J., & He, X. (2015). Automatic current sharing of an input-parallel output-parallel (IPOP) connected DC-DC converter system with chain-connected rectifiers. *IEEE Transactions on Power Electronics*, *30*(6), 2997–3016. https://doi.org/10.1109/TPEL.2014.2334896

Shi, J., Zhou, L., & He, X. (2012). Common-duty-ratio control of input-parallel output-parallel (IPOP) connected DC–DC converter modules with automatic sharing of currents. *IEEE Transactions on Power Electronics*, *27*(7), 3277–3291. https://doi.org/10.1109/TPEL.2011.2180541

Sijo, A., Mishra Mahesh, K., & N, L. (2015). Adaptive droop control strategy for load sharing and circulating current minimization in low-voltage standalone DC microgrid. *IEEE Transactions on Sustainable Energy*, *6*(1), 132–141. https://doi.org/10.1109/TSTE.2014.2360628

Sijo, A., N, L., & Mahesh Kumar, M. (2016). Control of photovoltaic-based low-voltage dc microgrid system for power sharing with modified droop algorithm. *IET Power Electronics*, *9*(6), 1132–1143. https://doi.org/10.1049/iet-pel.2015.0325

Vargil Kumar, E., & Veerachary, M. (2014). Modeling and analysis of two-input DC-DC converter. *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Mumbai, India, 7–11.

Vural, B., Erdinc, O., & Uzunoglu, M. (2010). Parallel combination of FC and UC for vehicular power systems using a multi-input converter-based power interface. *Energy Conversion and Management*, *51*(12), 2613–2622. https://doi.org/10.1016/j.enconman.2010.05.027

Wang, H., Han, M., Han, R., Guerrero, J. M., & Vasquez, J. C. (2018). A decentralized current-sharing controller endows fast transient response to parallel DC-DC converters. *IEEE Transactions on Power Electronics*, *33*(5), 4362–4372. https://doi.org/10.1109/TPEL.2017.2714342

Wang, J. B. (2011). Design a parallel buck derived converter system using the primary current droop sharing control. *IET Power Electronics*, *4*(5), 491–502. https://doi.org/10.1049/iet-pel.2010.0042

Wang, J. B. (2012). Parallel DC/DC converters system with a novel primary droop current sharing control. *IET Power Electronics*, *5*(8), 1569–1580. https://doi.org/10.1049/iet-pel.2012.0216

Yang, P., Tse, C. K., Xu, J., & Zhou, G. (2015). Synthesis and analysis of double-input single-output DC/DC converters. *IEEE Transactions on Industrial Electronics*, *62*(10), 6284–6295. https://doi.org/10.1109/TIE.2015.2424396

Ye, Y., Cheng, K. W. E., & Chen, S. (2017). A high step-up PWM DC-DC converter with coupled-inductor and resonant switched-capacitor. *IEEE Transactions on Power Electronics*, *32*(10), 7739–7749. https://doi.org/10.1109/TPEL.2016.2633381

Yuan-mao, Y., & Cheng, K. W. E. (2013). Multi-input voltage-summation converter based on switched-capacitor. *IET Power Electronics*, *6*(9), 1909–1916. https://doi.org/10.1049/iet-pel.2013.0015

Zhou, L.-W., Zhu, B.-X., & Luo, Q.-M. (2012). High step-up converter with capacity of multiple input. *IET Power Electronics*, *5*(5), 524–531. https://doi.org/10.1049/iet-pel.2011.0177

Zhu, X., Zhang, B., Li, Z., Li, H., & Ran, L. (2017). Extended switched-boost DC-DC converters adopting switched-capacitor/switched-inductor cells for high step-up conversion. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *5*(3), 1020–1030. https://doi.org/10.1109/JESTPE.2016.2641928