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On Chip DC-DC Converter with High Switching Frequency and Low Ripple Voltage

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Abstract

Objectives: A novel On Chip switched capacitor architecture to produce multiple voltages with high switching frequency and low ripple voltage. **Methods**: The proposed architecture uses integration of more than one converter topology to produce the scalable output voltage. The converter consists of MOSFET switches and MOS charge-transfer capacitors. The control circuitry was designed completely with digital domain to reduce static power consumed. **Findings:** The simulation of the scalable DC-DC converter was performed using TSMC 90nm Technology. The maximal efficiency of 80% was achieved for different topologies with 364 MHz switching frequency. **Improvements**: The load driving capacity of this converter was up to 5uW.

Keywords: DC-DC, DVS, High Frequency, Ripple Voltage, Voltage Converter

1. Introduction

In today's VLSI industry, the critical task is to ensure that energy consumed by the battery is minimal. The Dynamic Voltage Scaling (DVS)[1] provides the optimum results to maximize the energy efficiency when the performance requirement variations are high. The DVS system controls the circuit in such a way that the desired performance can be achieved by providing just sufficient voltage. This results in the overall summed up power saving. As voltage delivered by the supply declines, the current which is used to drive the transistor reduces, causing the degradation of overall speed of a circuit. In the sub-threshold, the same system works effectively at the voltages with reduced energy consumption. The voltage supply dithering using distinct frequency pairs was used in the design of Ultra-DVS[1] but it requires well organized and systematic system controller. The controller role is to share the time between discrete voltage levels which add to the complexity of the system. The architecture proposed in the[2] uses the implementation of more than one topology. The voltage range is divided amongst different topologies where they name it as T4, T6, T8, T9 andT12. Although it has advantage of increased efficiency, its major drawback is the complex and much larger control circuitry. The suffix in front of the T describes the output voltage provided by that particular topology (i.e. T4 means it provides output voltage of 400mV). The architecture used in[3] uses the concept of Digital Capacitance Modulation (DCM). Advantage of this technique is, it infers in coarse and fine grain tuning. The implementation done in[4] was slightly modified concept of Frequency Interleaving to suppress the variations present in the output voltage and ripple voltage. In[4] managed to get high power density with high efficiency which is one of the basic needs of the DC-DC. The high power density is censorious as it directly affects the overload imposed on area[5,6].

This paper gives emphasis on a DC-DC converter with scalable voltage having integration of multiple topologies which can generate output voltage of 0.6V, 0.8V, 1V, 1.2V by monitoring the requirement of a load. The implementation of voltage scalable DC-DC converter designed with the charge transfer and topology switches is outlined in. In this work, DC-DC converter is implemented using TSMC

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90nm with the on chip MOS capacitors used as charge transfer capacitors to achieve the efficiency of >80% when the load current is variable.

2. Scalable Voltages Methodology

This segment describes the methodology to generate varied range of voltages from the voltage source V in equal to 1.2V which is the off-chip battery source. The role of a charge-transfer capacitor is to fetch the charge from battery and deliver it to the load. The $\varphi_1$and φ_2 are the two clocks which are 180^0 out of phase are used for the implementation in this paper. The various topologies make use of only capacitors and charge transfer switches. Simple MOSFET is used as a switch. Consider VL = VNL– δV, where the no-load voltage is defined by VNL and δV is ripple voltage. The maximal achievable efficiency is limited for a DC-DC converter and it is given by η = (1 – δV/VNL). Hence higher the δV, efficiency is smaller. The use of only capacitors and switches for charge transfer poses this underlying drawback. Hence, it is mandatory to switch between distinct topologies to enhance the efficiency whose load current requirement is satisfied by the output voltage. The scalable range of output voltage is between 600 mV to 1.2V. As a convention, the names to the topologies viz. suffixes are given according to the output voltage.

3. Converter Topologies

Consider the T6 topology is shown in Figure 1 as the name suggests it can ideally supply the maximal load voltage of 0.6V, but practically results may vary due to losses in the system which is explained in the section 2. During the initial phase φ_1, the capacitors get charged from the off-chip battery to Vin/2. During φ_2 phase, capacitors discharges and hence load L gets the charge which was stored in the capacitors. Considering the no load condition, the T6 topology attempts to retain the output voltage equal to 0.6V.

For T8 topology, as shown in Figure 2, during phase φ_1, the capacitors gets charged serially from the off-chip battery. During φ_2 phase, they discharge in parallel and hence load L gets the charge which was deposited on the capacitor. Considering the no load condition, the T8 topology attempts to retain the output voltage equal to 0.8V. A 2/3 voltage ratio is obtained from the supply of 1.2V.

Similarly T10 topology which is shown in Figure 3 delivers no load voltage of 1V. It uses 5 capacitors. Considering the no load condition, the T10 topology attempts to retain the output voltage equal to 1V.

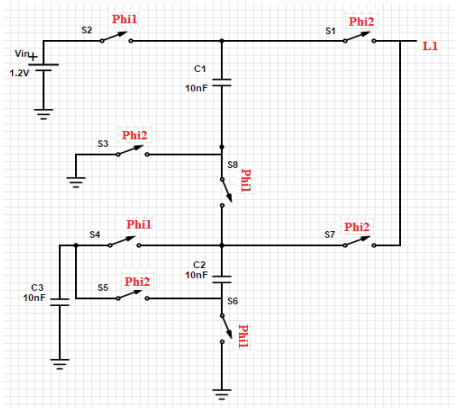

Figure 2. T8 topology.

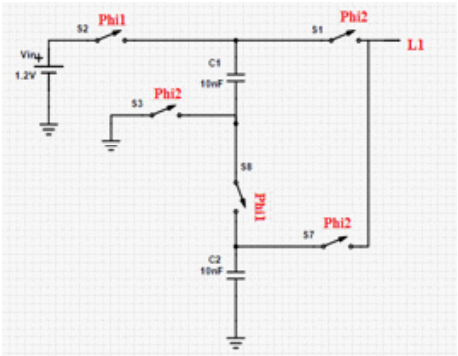

Figure 1. T6 topology.

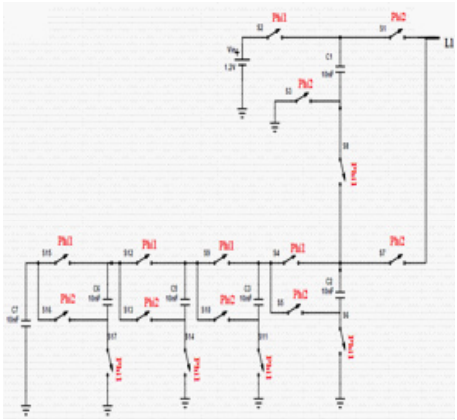

Figure 3. T10 topology.

The no-load voltage of 1.2V is provided by T12 topology. The working of this topology is similar to that of linear regulator which provides the voltages in the range of 1V to 1.2V.

4. Integration of Topologies

The proposed architecture generates stable scalable voltage depending on the load requirement. Different topologies are integrated as shown in Figure 4. Different voltages generated by switching between the different converter topologies. To sense the need of load current, feedback path is required from the output of the topology. Operating different switches for particular topology is the crucial task. This task is proposed in this paper with the help of control logic. The combinational logic makes use of basic blocks like Multiplexer. φ_1 and φ_2 are given as inputs to these basic gates. This control circuitry will operate on select line. Select line is the output of comparator which will compare load voltage with some predefined reference voltage. Depend on three select lines topologies will switch between 0.6, 0.8 and 1v topologies.

5. Simulation Results and Discussion

The proposed DC-DC converter is simulated using TSMC 90nm with on chip MOS capacitors used as charge transfer capacitors. Results of individual topologies are shown below in Figures 5, 6, 7 and 8. All these results are taken

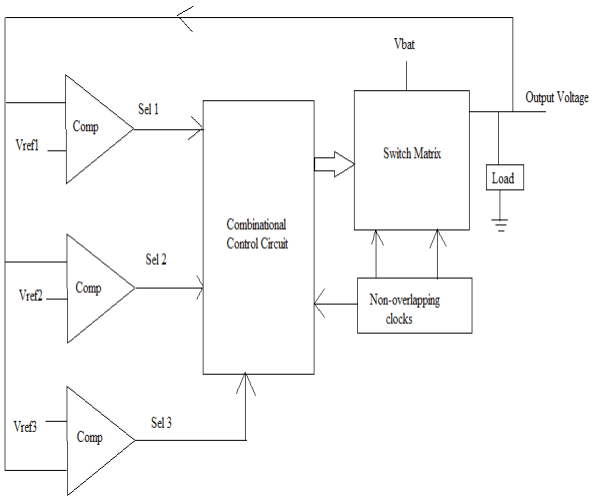

Figure 4. Integration of topologies.

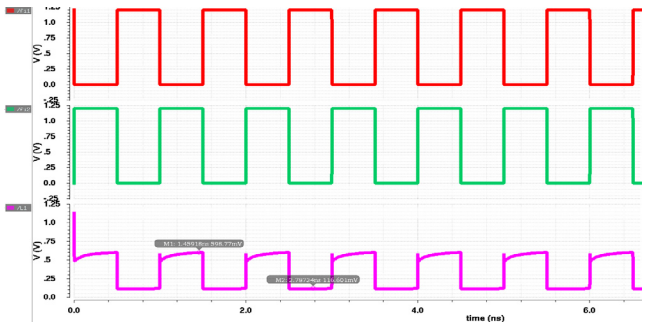

Figure 5. Output of T6 topology.

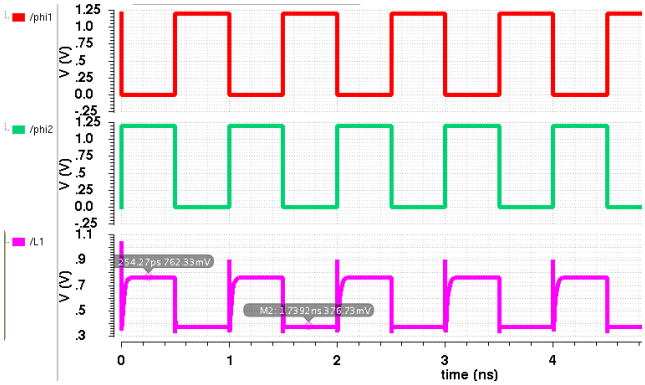

Figure 6. Output of T8 topology.

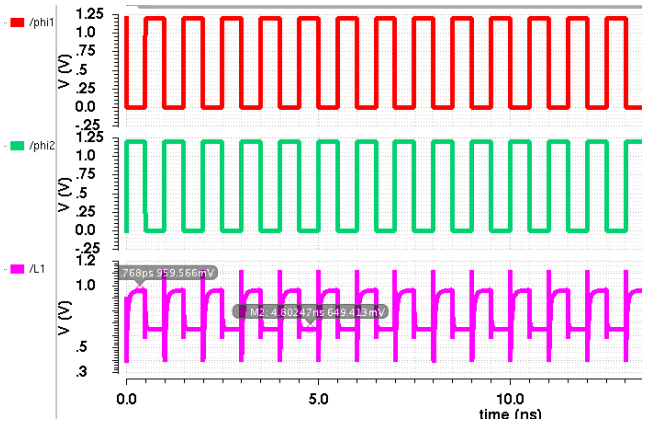

Figure 7. Output of T10 topology.

at 100pF load condition. Input voltage used for all topologies is 1.2V. Each C *fly* is of value 10nF and *CL* is of value 100pF. All topologies work at 1GHz frequency.

The comparison of integrated topology with previous work is shown in Table 1. At full load condition, T6 topology gives 593mV at the output node. Maximum efficiency achieved for T6 is 84% at full load. T8 topology gives

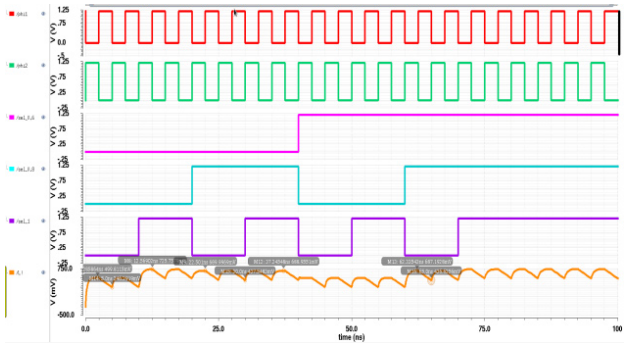

Figure 8. Output of integrated topology.

Table 1. Comparison with previous work

Parameter	Our Work			Ref.	
				[1]	[2]
Technology	90nm bulk			180 nm bulk	32 nm SOI
Input Voltage (V)	1.2			1.2	2
Conversion Ratio	1/2	2/3	5/6	1/3,1/2,2/3,3/4	1/3 to 1/3
Output Voltages (V) @ No Load	0.59	0.76	0.87	0.35,0.57,0.75,0.85	0.7 to 1.15
Ripple Voltage (mV) @ Full Load	93	80	135	<50	-----
Efficiency η (%)	84	89	84	> 70	79.76
Switching Frequency (MHz)	364			--------	-------

768mV at no load and gives efficiency 89.58% at full load. T10 topology gives 870mV at no load and at full load it achieves 84.48% efficiency. This efficiency calculation is done without considering losses. The non-overlapping clock frequency used to implement the integrated circuit is 1 GHZ for which topology switching frequency of 364 MHz is obtained switching between the voltages.

6. Conclusion

This paper has described a switched capacitor DC-DC converter with on-chip charge-transfer capacitors that can deliver scalable load voltages from 600mV to 1.2V. Various topologies were implemented in the Switched Capacitor DC-DC converter to minimize conduction and switching losses. These topologies were obtained by suitably combining segments of the charge-transfer capacitors. The switched topology DC-DC converter was able to achieve >80% efficiency over a wide range of load voltages 0.6V to 1.2V.

7. References

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