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Real-Time Implementation of a 31-Level Asymmetrical Cascaded Multilevel Inverter for Dynamic Loads

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ABSTRACT Among the renewable energy applications, the most popular inverters are cascaded multilevel inverters. Irrespective of numerous benefits these inverters face reliability issues due to the presence of more circuit components in the design. This has been a critical challenge for researchers in designing inverters with enhanced reliability by reducing the total harmonic distortion (THD). This paper proposes a 31-level asymmetric cascaded multilevel inverter for renewable energy applications. The proposed topology produces waveforms consisting of the staircase with a high number of output levels with lesser components with low THD. The investigations on the feasibility and performance of MLI under steady-state, transient, and dynamic load disturbances. The results are validated from a 1.6kW system which provides the proposed inverter.

INDEX TERMS Multilevel inverter (MLI), total harmonic distraction (THD), staircase modulation technique.

I. INTRODUCTION

In high power applications, like variable frequency drives, electric vehicles, HVDC, FACT, active power filters and hybridization of renewable energy sources, multilevel inverter played an important role. It is mainly effective for medium voltage motor drive system based applications, due to their less switch voltage stress. Multilevel converters, with different topologies, have been used in various industrial processes. These topologies are Cascaded H-Bridge (CHB), Flying Capacitor Converter(FCC) and Neutral Point Clamped(NPC) topologies [1]. The simple structures of CHBs makes it popular in varieties of applications. Also CHBs can be configures to operate in symmetrical and asymmetrical configurations [2]. In symmetrically configured CHBs, values of all the DC-voltages are equal and in case of asymmetrically configured CHBs, the values of DC-voltage sources are unequal in order to achieve required higher voltage levels. CHB methods are employed for medium and higher voltage levels, whereas under DCC and FCC topologies, balancing the voltages and sharing them is a complex task for higher voltage levels [2]. A survey of topologies, controls and applications of multilevel inverters was done in 2002 [3]. The investigation of cascaded MLIs with asymmetric, symmetric, multi-cell and hybrid configurations were presented in [4]. In which, a new symmetric dc-source hybrid MLI topology with minimal number of switch counts was proposed [5]. It is possible to extend this topology to higher number of levels. Multi - carrier pulse width modulation techniques [5] are adopted for triggering the gate pulses. The operation of the proposed topology is explained with the 15-level output voltage. Following it, a novel Proportional-Integral(P+I) control strategy for resistive and motor loads using genetic algorithm(GA) was proposed [6], here the controller constants generated maintains the stable output voltage at steady state under load disturbances and transient conditions [6].

Cascaded multilevel inverter with improved characteristics was presented by [7]. In the enhanced CMLI topology, the number of switching devices are marginally increased. However, the level of the MLI obtained is doubled for the same number of switching devices [7], [8]. A novel family

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of H Bridge MLI with transistor clamp to increase the number of output levels was presented by [10]. The proposed topology was able to achieve operation at a higher voltage (HV) and higher power level without increasing the device rating [9]. This topology is controlled by carrier-based Pulse Width Modulation (CBPWM) which reduce switching losses at higher switching frequencies and thereby improving the energy efficiency of the system [11]–[15]. A Total Harmonic Distortion and efficiency improvement in multilevel inverters through an open end wind configuration were analyzed in 2016 [16].

High-frequency switching causes high power loss in high power applications [16]–[19]. Most of the proposed topologies use more switches in the configuration which makes the circuit bulky and the generation process of gate pulses also is complex. This also results in higher THD and hence poor efficiency. The topology proposed in this article overcomes this problem significantly [20], [21]. The thirty-one level single phase asymmetric cascaded multilevel inverter is suggested in the present study. Several advantages have resulted from the reduced number of circuit components in the suggested topology. These advantages include few DC sources with low THD, fewer number of switches, and the generation of higher number of output voltage levels. Additionally, the dynamic condition is also examined [22], [23]. The suggested multilevel inverters are suitable for renewable energy and industrial [18] applications.

This article organized in the following manner. The succeeding section disuses the details of the proposed seven-level topology. Section III presents the particulars of thirty-one level inverter along with simulation results, section IV presents the comparison, section V presents the loss & efficiency calculations, VI presents the experimental results respectively.

II. PROPOSED TOPOLOGY

The configuration of the suggested seven-level single-phase inverter is depicted in Figure.1 [24]. Two switching elements are connected to two DC power supplies and are added in the conventional full-bridge inverter. The two DC voltages are represented as V_{A1}, V_{B1} and the power switches are represented as S_{A1}, S_{A2},S_{B1}, S_{B2}, S_P,S_Q. The simultaneous turning (ON/OFF) of the power switches (S_{A1}, S_{A2}) and (S_{B1}, S_{B2}) causes a short circuit and must be prevented. Furthermore, the simultaneous switching ON of S_P and S_Q must be avoided. V_{A1} = 1P.U and V_{B1} = 2P.U are the DC voltage sources, whose magnitude is illustrated in Figure.1. As depicted in Figure.1, seven switching states constitute the proposed inverter functioning. The levels of output voltage are as per the switch-ON and switch-OFF conditions (Table 1) and Figure.2 to Figure.8 depict the conventional inverter states of functioning. The generation of gate signals, by using a staircase modulation technique, constitutes the proposed switching strategies as shown in Figure.9. In this proposed topology, all the input voltage sources are fixed as V_{A1} = 135 V and V_{B1} = 270 V for acquiring the maximum peak voltage of 405 V at the load terminals. The load used for testing is 100 ohm resistor and 175 *mH* respectively. Figure.10 and Figure.11 depicts the simulation and experimental output voltage and current of seven-level inverter. The design of circuit parameters is discussed in the next sub-section.

TABLE 1. Switching states of proposed seven-level inverter.

Sl.no	S_{A1}	S_{A2}	S_{B1}	S_{B2}	S_P	S_Q	V_O
1	1	0	0	1	0	1	V_{A1}
2	1	0	0	1	1	0	-V_{B1}
3	1	0	1	0	0	1	V_{A1}+V_{B1}
4	1	0	1	0	1	0	0
5	0	1	1	0	1	0	-V_{A1}
6	0	1	1	0	0	1	V_{B1}
7	0	1	0	1	1	0	-(V_{A1}+V_{B1})

A. DESIGN OF CIRCUIT PARAMETERS

These sub-section discuss the method of choosing the number of sources, switches, and output voltage levels.

The quantity of output levels can be estimated as follows:

$$N_{levels} = 2^{k+1} - 1 \tag{1}$$

where k is the number of DC voltage sources on each leg Number of switches can be obtained using

$$N_{switches} = 2k + 2 \tag{2}$$

Number of sources can be estimated using

$$N_{sources} = k \tag{3}$$

Maximum blocking voltage of all switches can be represented as

$$V_{block} = V_{A1} + V_{B1} \tag{4}$$

Maximum output voltage of inverter can be represented as

$$V_{o,max} = V_{Ak} + V_{Bk} \tag{5}$$

The value of the switch blocking voltages and the magnitude of the DC voltage sources constitute the other significant parameters in the evaluation of a multilevel inverter's total cost. The total cost of inverter decreases with the reduction in value of the switch blocking voltages, reduction in DC voltage variations, and reduction in number of DC voltage sources.

$$K_{variation} = 2k \tag{6}$$

The maximum magnitude of the power switch blocking voltages is computed by using the following pattern. The blocking voltages of V_{SA1}, V_{SA2}, V_{SB1}, and V_{SB2} are estimated as follows (Fig.1).

$$V_{SA1} = V_{SA2} = V_{A1} \tag{7}$$

$$V_{SB1} = V_{SB2} = V_{B1} \tag{8}$$

where V_{SA1}, V_{SA2},V_{SB1} and V_{SB2} are the blocking voltage of S_{A1}, S_{A2}, S_{B1} and S_{B2} respectively. The following is used to

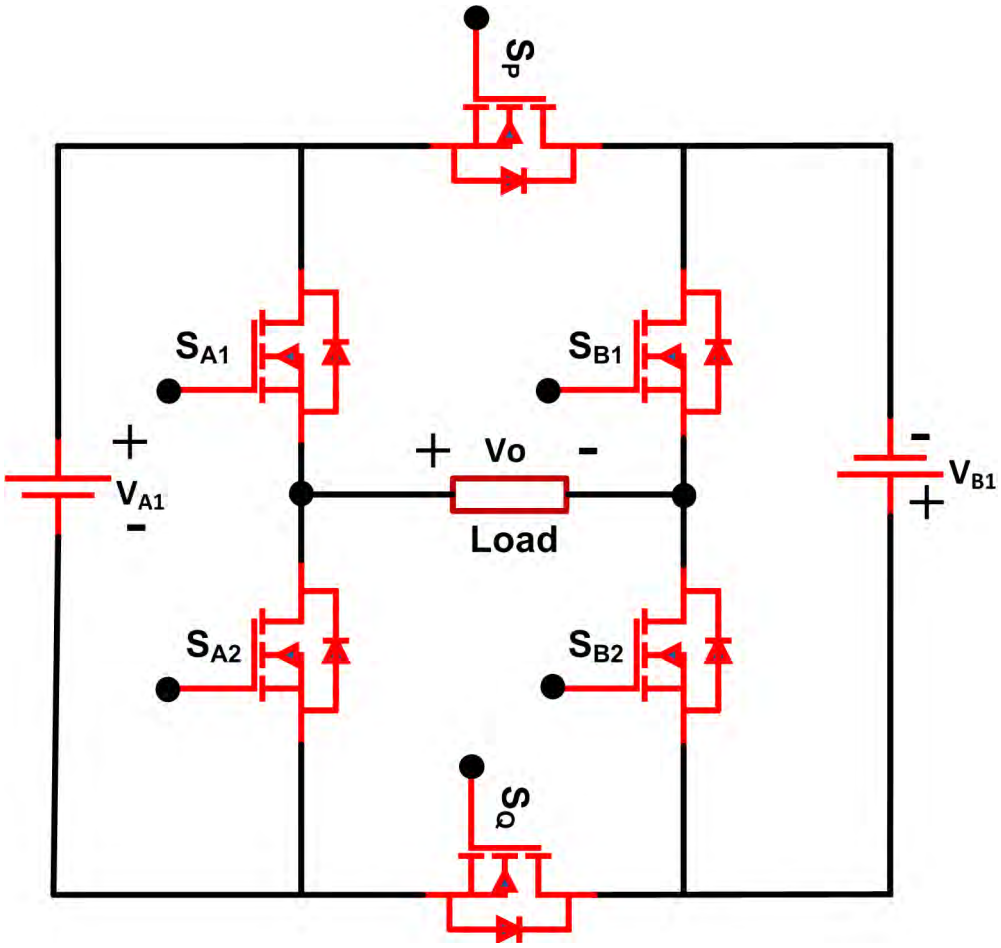

FIGURE 1. Basic proposed seven-level inverter.

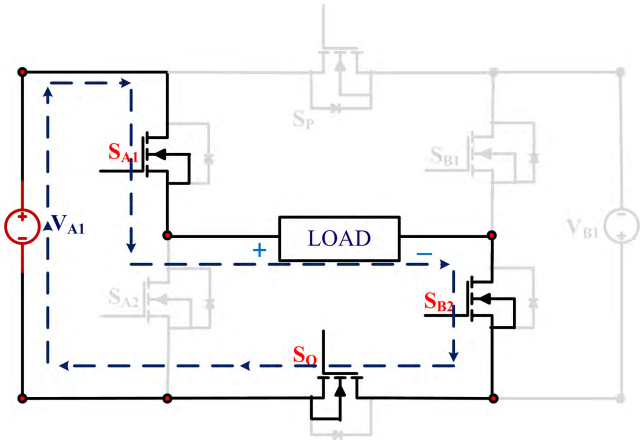

FIGURE 2. Mode 1.

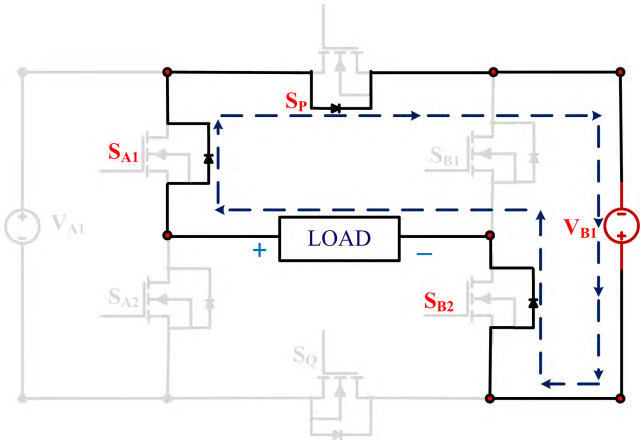

FIGURE 3. Mode 2.

estimate the maximum blocking voltage of all of the proposed seven-level inverters switches.

$$V_{block,1} = V_{SA1} + V_{SA2} + V_{SB1} + V_{SB2} + V_{SP} + V_{SQ} = 4(V_{A1} + V_{B1}) \quad (9)$$

For the presented seven-level multilevel inverter, the number of voltage levels, number of switches and magnitude of output voltage shall be inferred from the following equations (1), (2), (3) and (5) respectively. The number of output voltage levels can be calculated using equation (1).

$$N_{levels} = 2^{k+1} - 1 = 2^{2+1} - 1 = 7 \quad (10)$$

where $k = 2$ is the number of DC voltage sources on each leg, then the number of switches, sources shall be calculated using equation.(2) and (3) respectively.

$$N_{switches} = 2 * 2 + 2 = 6 \tag{11}$$

and

$$N_{sources} = k = 2 \tag{12}$$

Maximum output voltage of inverter can be represented by using equation (5).

$$V_{o,max} = V_{Ak} + V_{Bk} = V_{A1} + V_{B1} = 135 + 270 = 405V \tag{13}$$

III. PROPOSED THIRTY-ONE LEVEL ASYMMETRIC MULTILEVEL INVERTER

Four power switches and two additional DC voltage sources are added to the seven-level inverter to obtain the suggested topology that can be used for the thirty-one level inverter configuration. the thirty-one level limitation is found to be existing in the asymmetric type of cascade h-bridge multi-level inverter, shown in Figure.12. The proposed topology is utilized for producing more number of voltage levels, without increasing the quantity of DC voltage sources and switches. Ten unidirectional power switches and four DC voltage sources comprise the suggested topology. The power switches were represented as S_{A1}, S_{A2}, S_{A3}, S_{A4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}, S_P, S_Q and four DC voltage source represented as V_{A1}, V_{A2}, V_{B1}, V_{B2}. The DC voltage sources if (V_{A1}, V_{A2}, V_{B1}, V_{B2}) would be initially short-circuited, if the power switches of (S_{A1}, S_{A2}) (S_{A3}, S_{A4}) (S_{B1}, S_{B2}) and (S_{B3}, S_{B4}) are simultaneously turned ON. Hence, the power switches must not be turned ON simultaneously. Similarly, the simultaneous turning-ON of S_P and S_Q must be avoided. DC voltage sources magnitude was considered, where $V_{A1} = 1$P.U, $V_{A2} = 5$P.U, $V_{B1} = 2$P.U, and $V_{B2} = 10$P.U. The pulses are generated individually and fed to the switches to obtain the required output voltage as shown in Figure.22 and Figure.23 respectively. The control states of the power switches are illustrated in Table 2. As depicted in Figure.12, thirty-one switching states constitute the proposed inverter functioning. A few output voltage levels are generated according to the switch-ON and switch-OFF conditions as shown in Figure.13 to Figure.20, which depict the conventional inverter states of functioning. In this proposed topology, all the input voltage sources are fixed as $V_{A1} = 22.5$ V, $V_{A2} = 45$ V,$V_{B1} = 112.5$ V and $V_{B2} = 225$ V for acquiring the maximum peak voltage of 405 V at the load terminals. The load used for testing is 100 ohm resistor and 175 mH respectively. Figure.24 and Figure.25 depicts the simulation output voltage, current and THD of thirty-one level inverter.

For the proposed thirty-one level multilevel inverter, the number of voltage levels, number of switches and magnitude of output voltage shall be inferred from the following equations (1), (2), (3) and (5) respectively. The number of output voltage levels can be calculated using equation (1)

$$N_{levels} = 2^{k+1} - 1 = 2^{4+1} - 1 = 31 \tag{14}$$

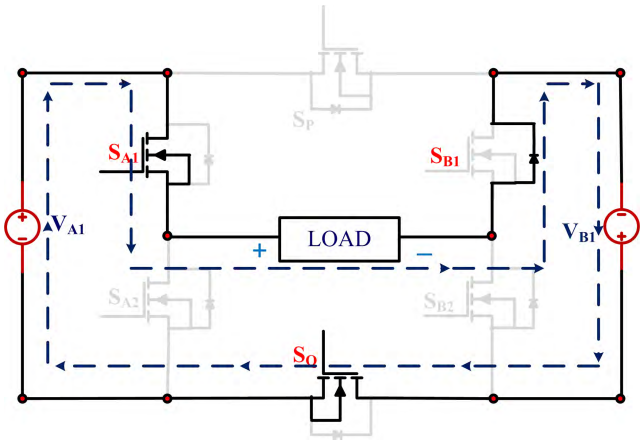

FIGURE 4. Mode 3.

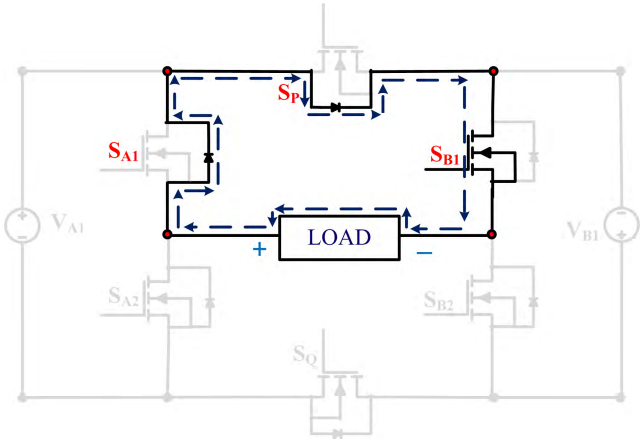

FIGURE 5. Mode 4.

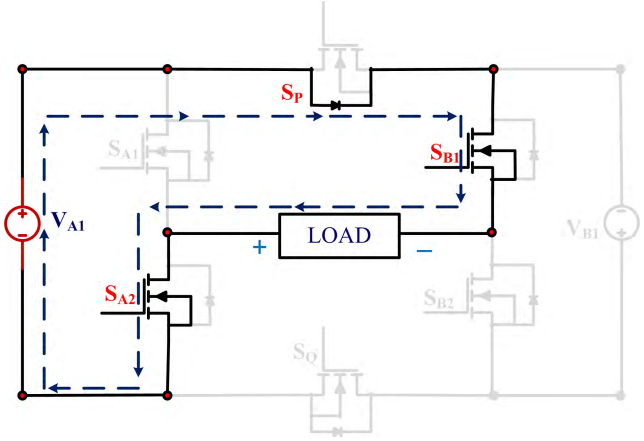

FIGURE 6. Mode 5.

where $k = 4$ is the number of DC voltage sources on each leg, then the number of switches, sources shall be calculated using equation.(2) and (3) respectively.

$$N_{switches} = 2 * 4 + 2 = 10 \tag{15}$$

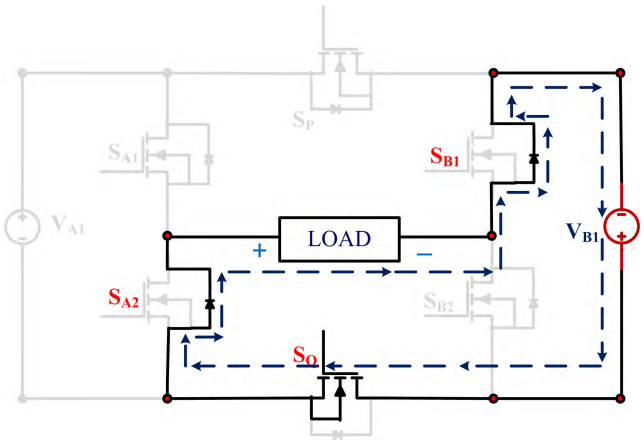

FIGURE 7. Mode 6.

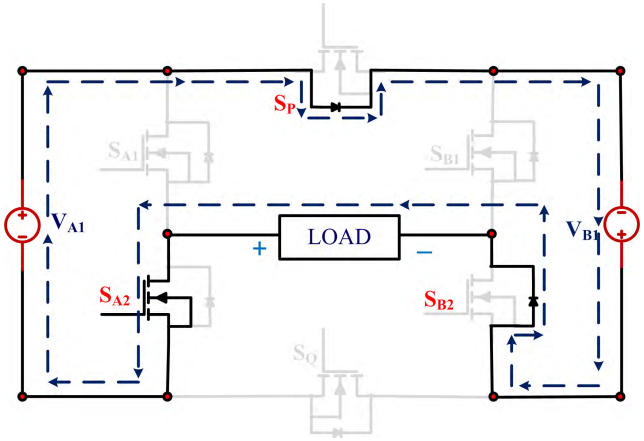

FIGURE 8. Mode 7.

and

$$N_{sources} = k = 4 \tag{16}$$

Maximum output voltage of inverter can be represented as by using equation (5).

$$V_{o,max} = V_{Ak} + V_{Bk} = 22.5 + 45 + 112.5 + 225 = 405V \tag{17}$$

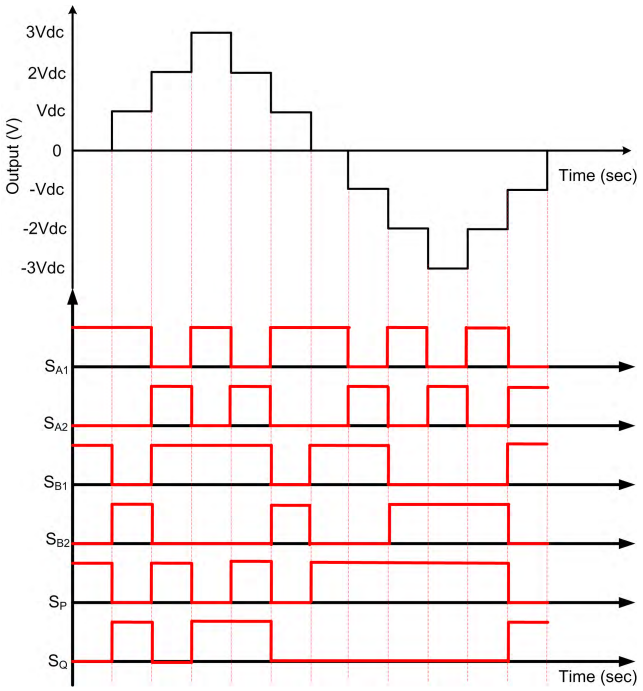

FIGURE 9. Typical output and gate pulses of seven-level inverter.

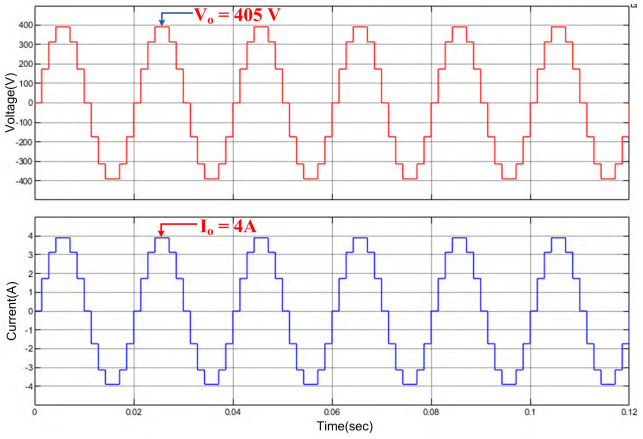

FIGURE 10. Simulation output waveform of seven-level inverter.

IV. COMPARISON

The recommended topology employs only ten power switches and four DC sources. Henceforth, the number of gate driver modules are identical to the number of power switches. Then, the proposed asymmetric topology is compared with conventional MLIs (DCMLI, FCMLI and CHBMLI) in Table 3. In Table 3, every component is deliberate for a similar number of voltage levels. Although all the conventional topologies need 60 switches to provide a 31-level output voltage levels, the proposed topology involves only 10 switches. The significantly compact size of switches in the proposed topology compared with the conventional topology to products enhanced results creates it additional anticipated for a future renewable application. Since, the DC-link capacitors are not essential for the proposed topology, it is free from voltage balancing problem. In addition to that, it does not require any clamping capacitor and clamping diodes. However, each topology has its own merits and demerits. The recommended topology has several benefits, such as fewer number of switching devices, DC source count and driver circuits and a least number of conducting switches per voltage level. Also, the value of 3.7% total harmonic distortion (THD) in asymmetric topology satisfies the IEEE 519 standard. Therefore, it can be concluded that the proposed topology requires smallest switch count using both high and fundamental switching frequencies, thereby reducing the power losses and cost. In the next sub section, losses and efficiency are discussed.

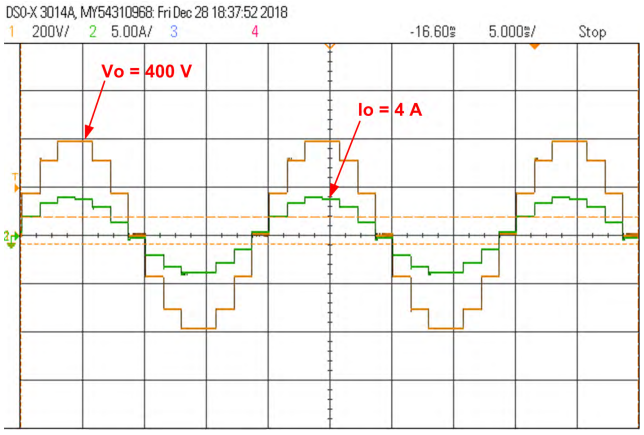

FIGURE 11. Experimental output waveform of seven-level inverter.

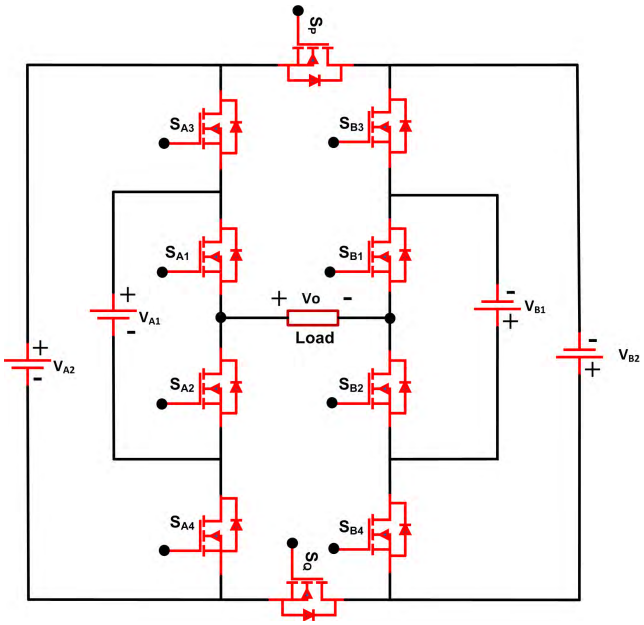

FIGURE 12. Proposed thirty-one level inverter.

V. LOSSES AND EFFICIENCY CALCULATION

The losses can be determined as follows Switching losses and conduction losses are the two primary losses that are associated with switches. The conduction loss of an switches (Pc,Switch(t)) and the conduction loss of switch (IGBT/MoSFET) is estimated.

$$P_{c,switch}(t) = \left[V_{switch} + R_{switch} i^{\beta}(t)\right] i(t) \quad (18)$$

$$P_{c,mosfet}(t) = \left[V_{mosfet} + R_{mosfet} i^{\beta}(t)\right] i(t) \quad (19)$$

where Vswitch(IGBT/MOSFET) is the forward voltage drop of IGBT/MOSFET and V_d is the forward voltage drop of diodes. b is a constant with regards to the IGBTs/MOSFET specification [25], and Rswitch(IGBT/MOSFET) is the IGBTs/MOSFET equivalent resistance and R_d is the diodes equivalent resistance. The average value of the multilevel inverter's conduction power loss (Pc) can

TABLE 2. Switching states of proposed thirty-one level inverter.

Sl.no	Switches On States	Output Voltage
1	$S_{A1}, S_{A3}, S_{B1}, S_{B3}, S_Q$	V_{A2}+V_{B2}
2	$S_{A1}, S_{A3}, S_{B2}, S_{B3}, S_Q$	V_{A2}+V_{B2}-$VA1$
3	$S_{A2}, S_{A3}, S_{B1}, S_{B3}, S_Q$	V_{B2}+V_{A2}-V_{B1}
4	$S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_Q$	V_{A2}+V_{B2}-V_{A1}- V_{B1}
5	$S_{A1}, S_{A3}, S_{B1}, S_{B4}, S_Q$	V_{A1}+V_{B2}
6	$S_{A1}, S_{A3}, S_{B2}, S_{B4}, S_Q$	V_{B2}
7	$S_{A2}, S_{A3}, S_{B1}, S_{B4}, S_Q$	V_{A1}-V_{B1}+V_{B2}
8	$S_{A2}, S_{A3}, S_{B2}, S_{B4}, S_Q$	V_{B2}-V_{B1}
9	$S_{A1}, S_{A4}, S_{B1}, S_{B3}, S_Q$	V_{A2}+V_{B1}
10	$S_{A1}, S_{A4}, S_{B2}, S_{B3}, S_Q$	V_{A2}+V_{B1}-V_{A1}
11	$S_{A2}, S_{A4}, S_{B1}, S_{B3}, S_Q$	V_{A2}
12	$S_{A2}, S_{A4}, S_{B2}, S_{B3}, S_Q$	V_{A2}-V_{A1}
13	$S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_Q$	VA1+VB1
14	$S_{A1}, S_{A4}, S_{B2}, S_{B4}, S_Q$	V_{B1}
15	$S_{A2}, S_{A4}, S_{B1}, S_{B4}, S_Q$	V_{A1}
16	$S_{A1}, S_{A3}, S_{B1}, S_{B3}, S_P$	0
17	$S_{A1}, S_{A3}, S_{B2}, S_{B3}, S_P$	- VA1
18	$S_{A2}, S_{A3}, S_{B1}, S_{B3}, S_P$	- V_{B1}
19	$S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_P$	-(VA1+VB1)
20	$S_{A2}, S_{A3}, S_{B1}, S_{B4}, S_P$	- (V_{A2}-V_{A1})
21	$S_{A1}, S_{A4}, S_{B1}, S_{B3}, S_P$	-V_{A2}
22	$S_{A2}, S_{A4}, S_{B2}, S_{B4}, S_P$	-(V_{A2}+V_{B1}-V_{A1})
23	$S_{A2}, S_{A3}, S_{B2}, S_{B4}, S_P$	-(V_{A2}+V_{B1})
24	$S_{A1}, S_{A4}, S_{B2}, S_{B3}, S_P$	-(V_{B2}-V_{B1})
25	$S_{A1}, S_{A4}, S_{B2}, S_{B3}, S_P$	-(V_{A1}-V_{B1}+V_{B2})
26	$S_{A2}, S_{A4}, S_{B1}, S_{B3}, S_P$	-V_{B2}
27	$S_{A2}, S_{A4}, S_{B2}, S_{B3}, S_P$	-(V_{A1}+V_{B2})
28	$S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_P$	-(V_{A2}+V_{B2}-V_{A1}-V_{B1})
29	$S_{A1}, S_{A4}, S_{B2}, S_{B4}, S_P$	-(V_{B2}+V_{A2}-V_{B1})
30	$S_{A2}, S_{A4}, S_{B1}, S_{B4}, S_P$	-(V_{A2}+V_{B2}-V_{A1})
31	$S_{A2}, S_{A4}, S_B2, S_{B4}, S_P$	-(V_{A2}+V_{B2})

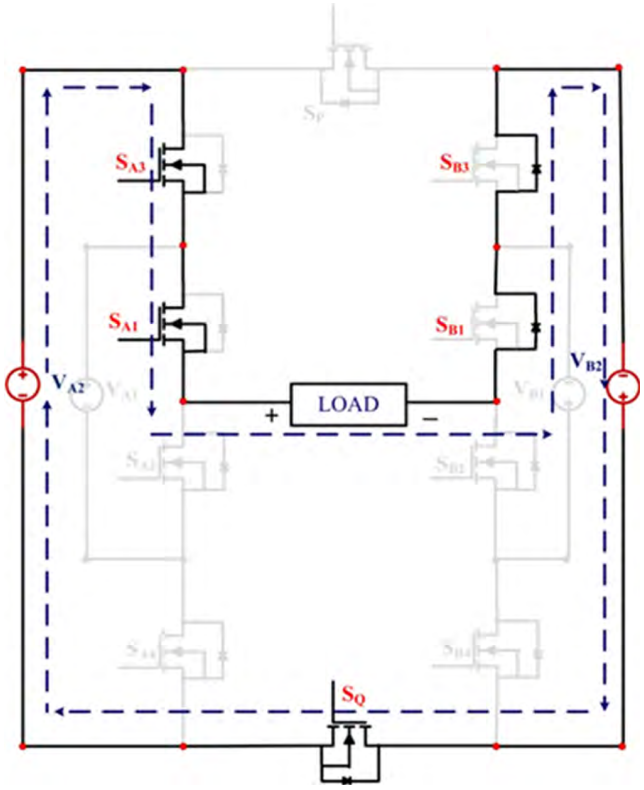

FIGURE 13. Mode 1: Vo = (V_{A2} + V_{B2}).

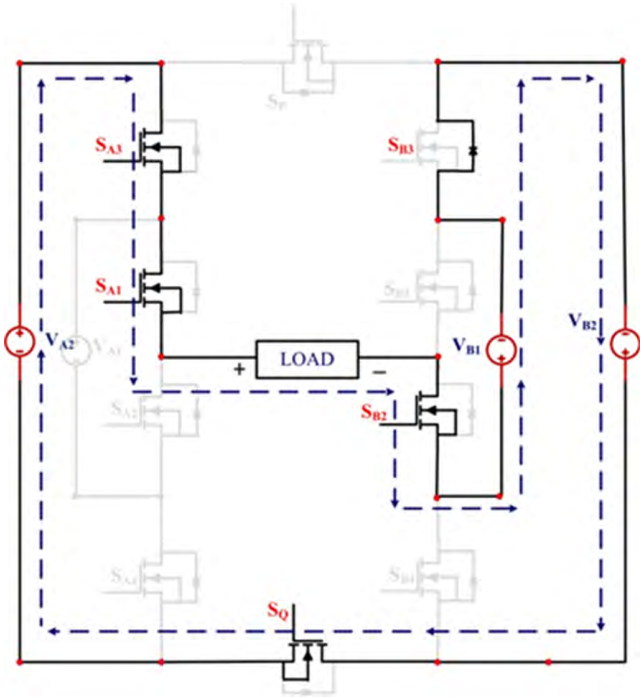

FIGURE 14. Mode 2: Vo = $(V_{A2} + V_{B2} - V_{A1})$.

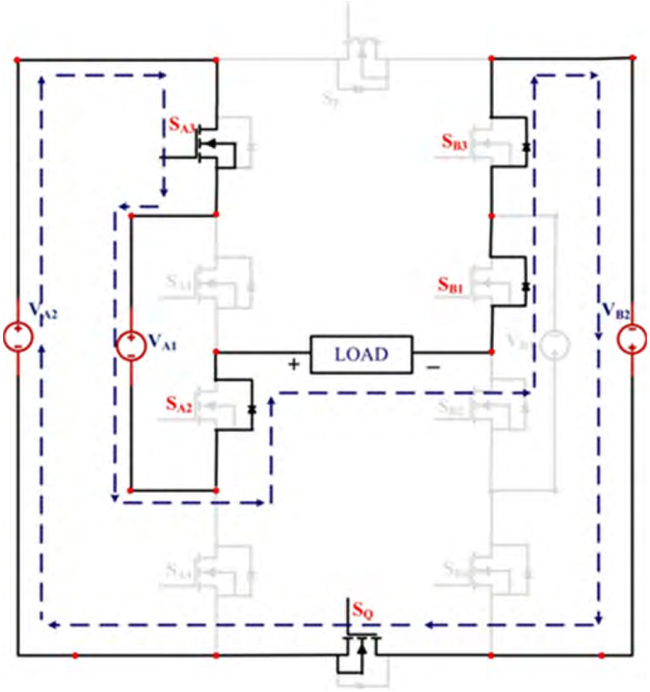

FIGURE 15. Mode 3: Vo = $(V_{B2} + V_{A2} - V_{B1})$.

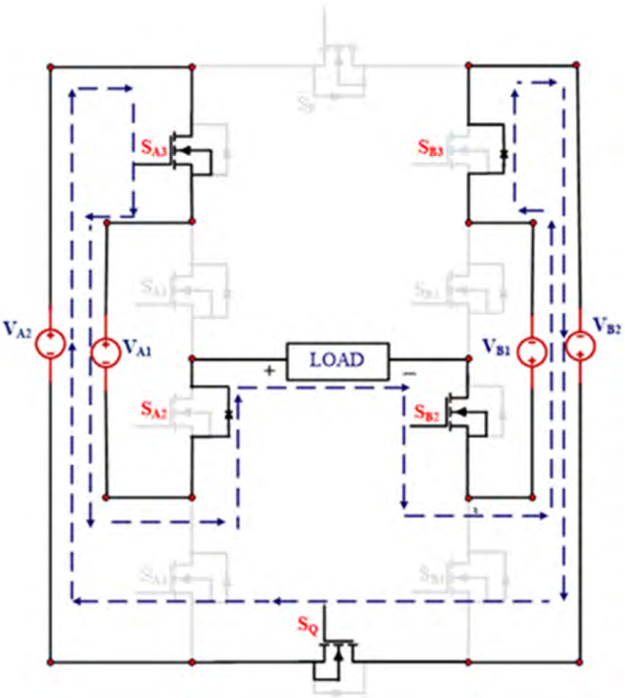

FIGURE 16. Mode 4: Vo = $(V_{A2} + V_{A1} + V_{B1} + V_{B2})$.

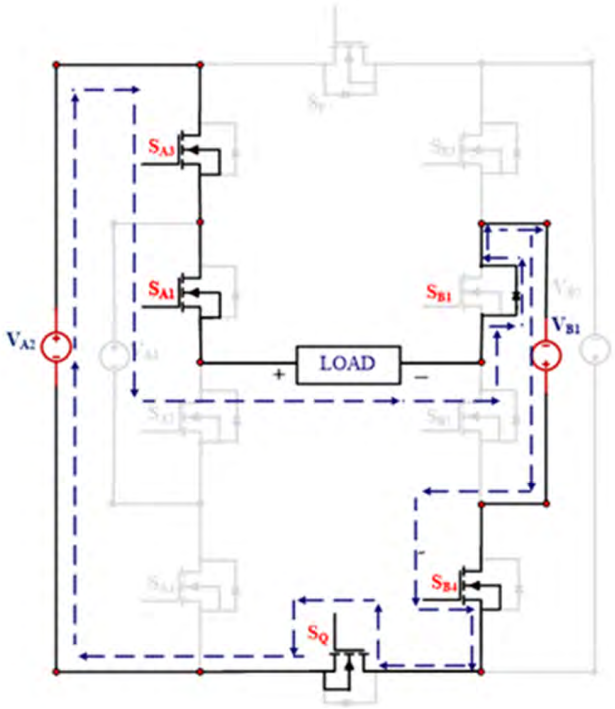

FIGURE 17. Mode 5: Vo = $(V_{A1} + V_{B2})$.

be given as follows [25], considering that there are Nswitch(IGBT/MOSFET) transistor and N_d diodes at time instant t in the current path.

$$P_c = \frac{1}{2}\left[N_{switch}(t)p_{c,T}(t) + N_D(t)p_{c,D}(t)\right]d(t) \qquad (20)$$

The estimation of the energy loss is utilized as the basis for calculating the switching losses. The turn-ON and the turn-OFF are the periods during which the occurrence of switching losses is witnessed. The linear variations of the switching current and voltage are considered to avoid complexities. The following relations are derived on the basis of this assumption.

$$J_{off,k} = \int_0^{t_{off}} v(t)i(t)d(t) = \frac{1}{6}V_{sw,k}It_{off} \qquad (21)$$

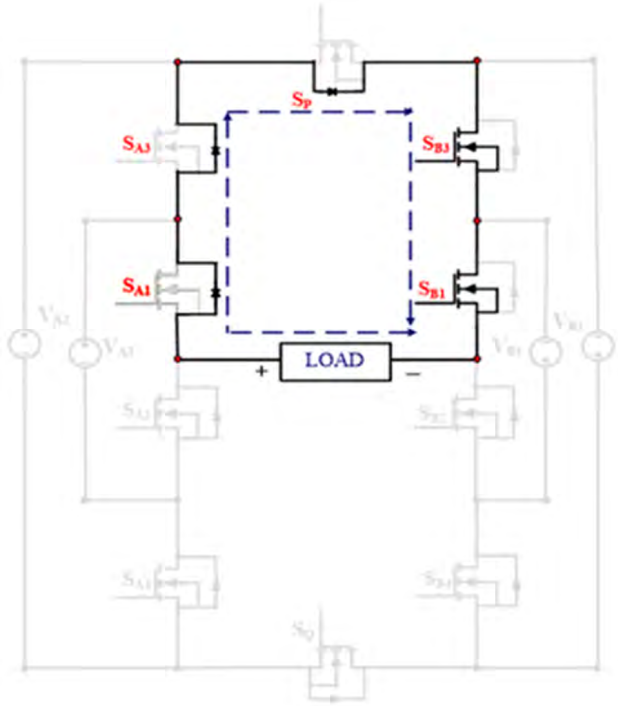

FIGURE 18. Mode 16: Vo = 0.

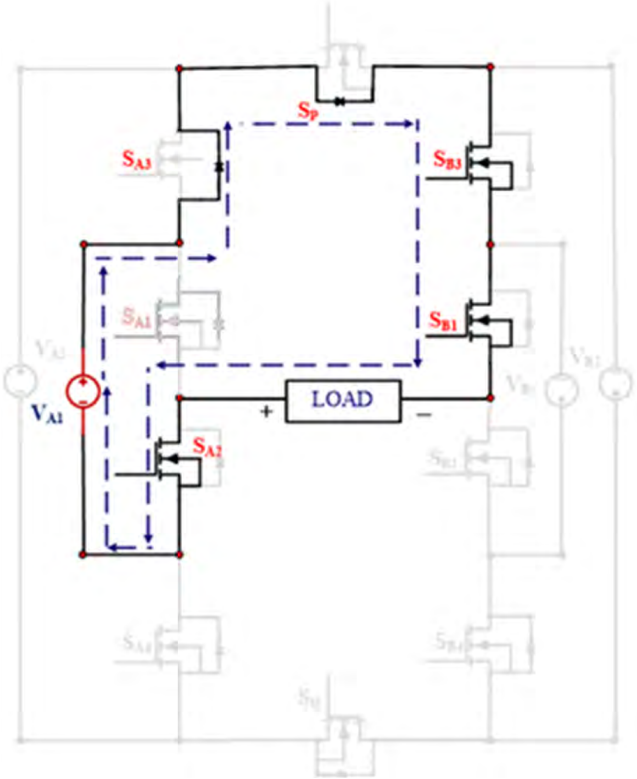

FIGURE 19. Mode 17: Vo = -(V_{A1}).

$$J_{on,k} = \int_0^{t_{on}} v(t)i(t)d(t) = \frac{1}{6}V_{sw,k}I't_{on} \tag{22}$$

where J_{kon} is the turn-ON loss and J_{koff} is the turn-OFF loss of the switch k [26]. Ton is turn-ON time and T_{off} is the

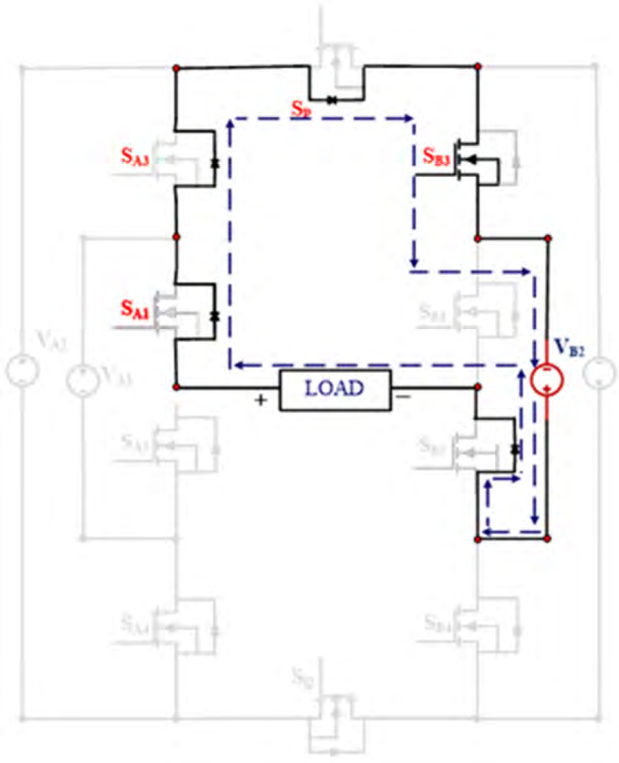

FIGURE 20. Mode 18: Vo = -(V_{B1}).

TABLE 3. Comparison with conventional topologies.

Items	DCMLI	FCMLI	CBMLI	Proposed 31-MLI
No. of Switches	60	60	60	10
No. of Sources	1	1	15	4
Output Voltage levels	31	31	31	31
Driver Circuits	60	60	60	10
Diodes	56	0	0	0
Capacitors	0	28	0	0
%THD	-	-	-	3.7
Total loss	-	-	-	32W
Efficiency	-	-	-	98 %

turn-OFF time of the switch k. $V_{sl,k}$ is the off-state voltage on the switch, I is the switch current before turning off, and I is the switch current after turning on. In the output voltages fundamental cycle, the sum of all turn-OFF and turn-ON energy losses is equivalent to the switching power loss (P_{sl}) [26].

$$P_{sl} = f \sum_{k=1}^{Nswitch} \left[\sum_{i=1}^{Non,k} J_{on,ki} + \sum_{i=1}^{Noff,k} J_{off,ki} \right] \tag{23}$$

where $N_{off,k}$ is the number of switches turned-OFF, $N_{on,k}$ is the number of switches turned-ON, and f is the fundamental frequency of the switch k, during a fundamental cycle. Moreover, $J_{k,off}$ is the energy loss of the switch k during the ith turn-OFF and $J_{on,ki}$ is the energy loss of the switch k during the i_{th} turn-ON. The sum of the switching losses and the conduction losses constitutes the multilevel converters total

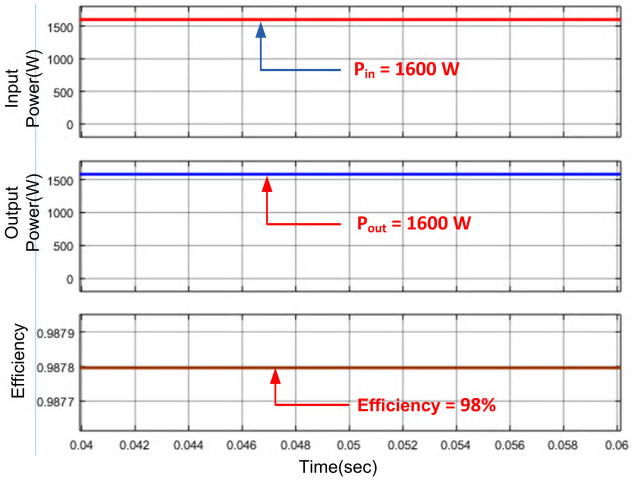

FIGURE 21. Simulation output waveforms of input power, output power & efficiency.

TABLE 4. Component specifications.

Item	Specification
DC Sources	0-300V
MOSFETs	IRF 840
Diodes	IN914
Controller	dSPACE RTI Controller, digital I/O ports
GATE Driver	TLP 250
RLoad	50 ohm,100 0hm
LLoad(Motor)	175 henry

loss (P_{loss}), which is as follows:

$$P_{loss} = P_c + P_{sl} \tag{24}$$

Eventually, the inverters efficiency (n) is computed as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{25}$$

where P_{out} denotes the inverters output power and P_{in} denotes the inverters input powers. The efficiency and total losses analysis is computed in the MATLAB simulation for the proposed thirty-one level inverter. In this inverter, IRF840 MOSFET is undertaken for the simulation. The values of Rds (on) is 0.85 â"ę and VDS (on) is 0.8V respectively are assigned for the switches, the net inputs power is fed into the inverter is 1600W. The load output power is obtained as 1568 W and efficiency is achieved as 98%. The simulation results of input power, output power and efficiency with respect to time are shown in Figure.21. and total obtained total losses is 32W(switching + conduction loss).

VI. EXPERIMENTAL RESULTS

The prototype hardware set-up for thirty-one level inverter systems is established and tested experimentally. Figure.33 depicts the prototype of the suggested multilevel inverter. The downloading of simulation block sets is done into dSPACE RTI 1104 digital I/O ports and the implementation of the staircase modulation PWM method (for gate pulses) is done

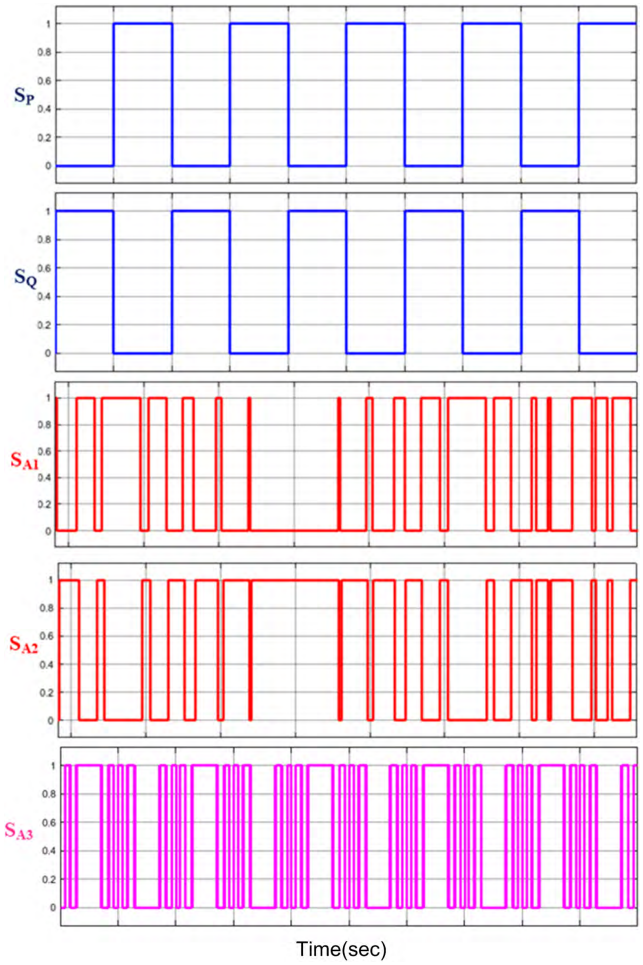

FIGURE 22. Gate pulses-1 of inverter.

in MATLAB-SIMULINK. In order to facilitate real-time interfacing application, 20 output pins are possessed by the digital I/O ports. TLP 250 driver generates the input pulses from the dSPACE RTI 1104. The PWM pulse pattern can be boosted by the gate driver from 5 V to 15 V. The power switches can be turned-ON by the 15 V pulse. The prototype model component specifications are given in Table 4, the prototype experimental results are validated at steady state, load disturbance conditions are performed with resistive, inductive loads and THD are shown in Figure.26 to Figure.32 respectively. The steady state testing is done with resistive load (unity power factor load) with 400 V output voltage. The output current is obtained with 4 A value. The RMS value of the output current and voltage are obtained with 282.78 V and current 2.828 A respectively. The hardware results are shown in Figure.26 and Figure.27 respectively. The prototype experimental results evidently show that with thirty-one level in the output voltage. The waveform visibly shows that the phase angle between the load current and the load voltage is zero. After the completion of steady-state testing with a resistive load, the inductive load (lagging power factor load) with 400 V output voltage is introduced. The output

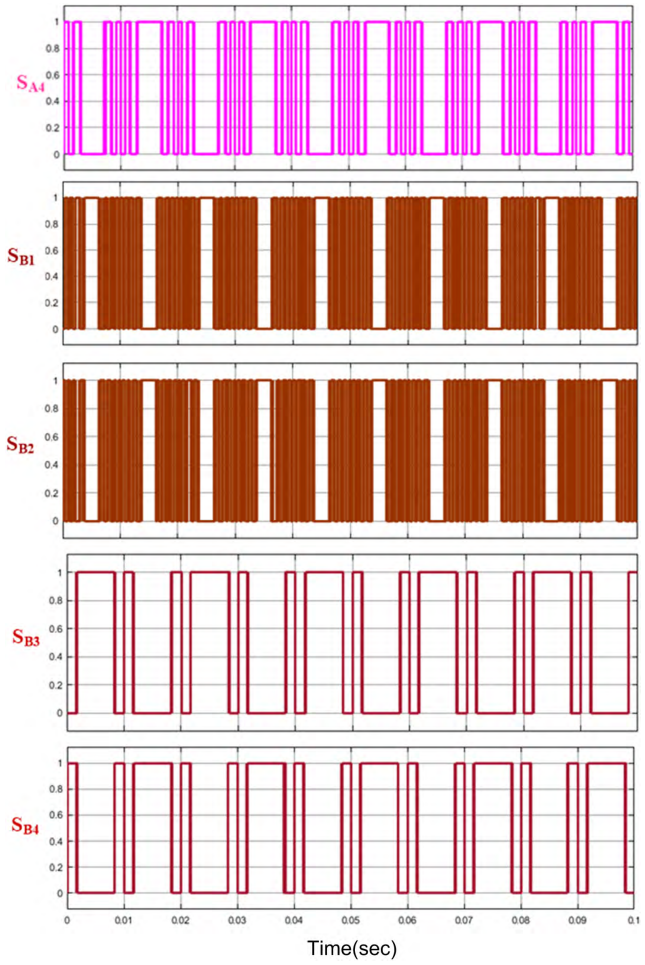

FIGURE 23. Gate pulses-2 of inverter.

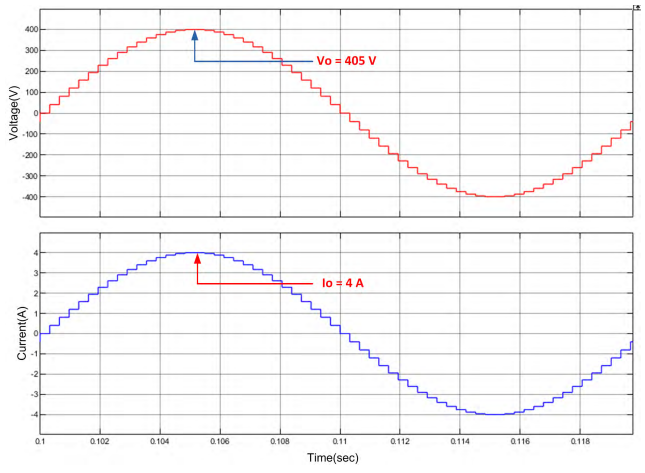

FIGURE 24. Simulation output voltage and current of thirty-one level inverter.

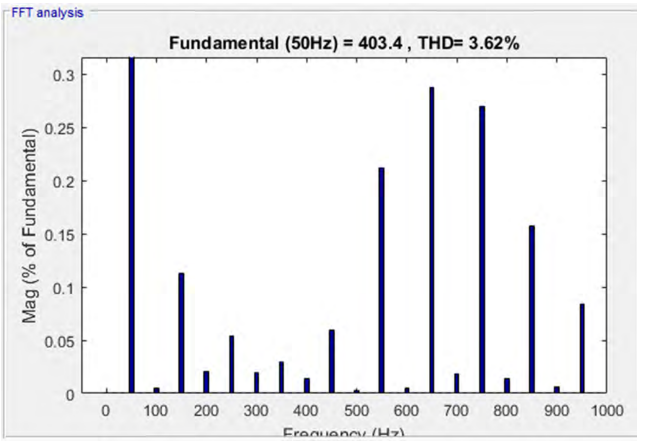

FIGURE 25. Simulation THD of thirty-one level inverter.

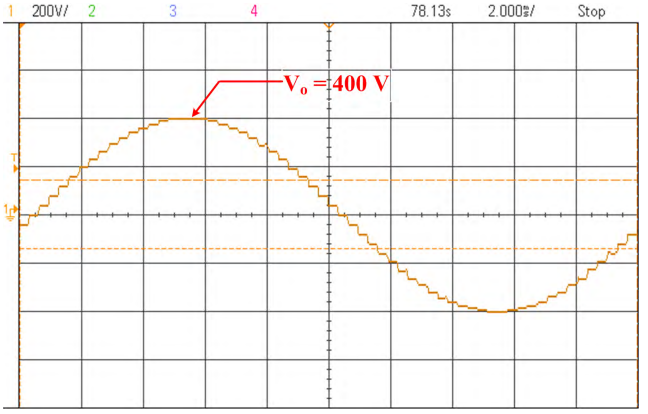

FIGURE 26. Experimental output voltage of thirty-one level inverter.

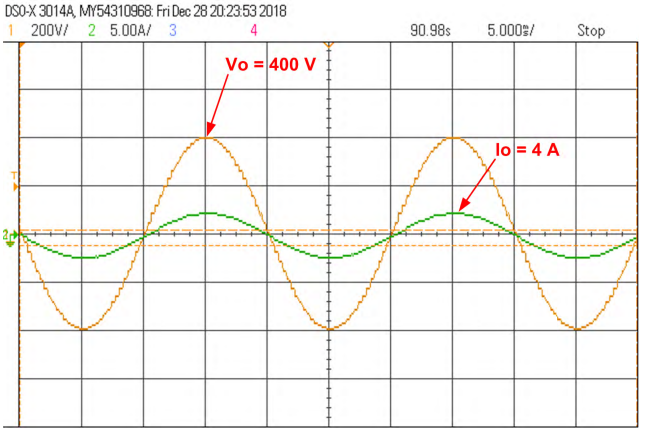

FIGURE 27. Steady-State voltage and current with resistive load.

current is found with 4 A value. The RMS value of the output current and voltage are attained with 282.78 V and current 2.828 A respectively, the achieved hardware results are tabulated in Table 5. The observed experimental results are given in Figure.28. The results evidently show that with thirty-one level in the output voltage. The waveform clearly shows that the phase angle between the load current and the load voltage is lagging. In certainty, loads rarely exist distinctly. They will always occur in a combination of resistive and inductive loads. Usually, in any particular place, when a resistive load

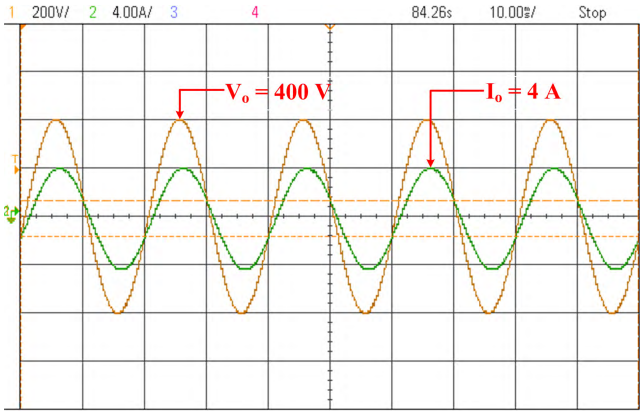

FIGURE 28. Steady-State voltage and current response with inductive load.

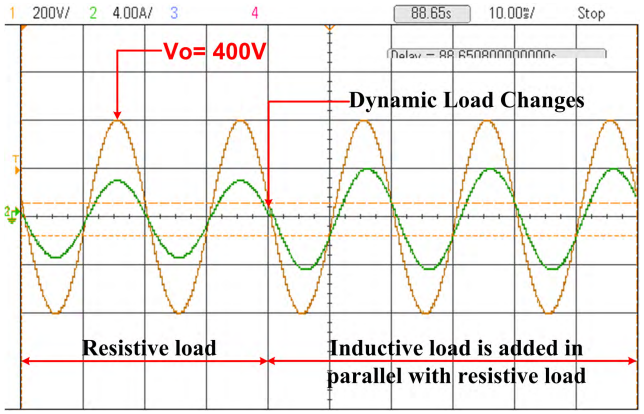

FIGURE 29. Unity power factor to lagging power factor load disturbance response.

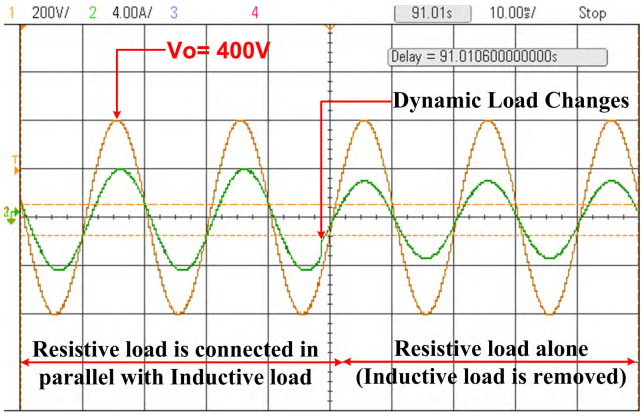

FIGURE 30. Lagging power factor to unity power factor load disturbance response.

is being utilized an abrupt accumulation of inductive load in parallel to the resistive load or vice versa is identical likely. Even at these circumstances, the output voltage must stay stable is shown in Figure.29 and Figure.30 respectively. The proposed inverter will generate higher output voltage levels and with fewer circuit components with relatively low THD

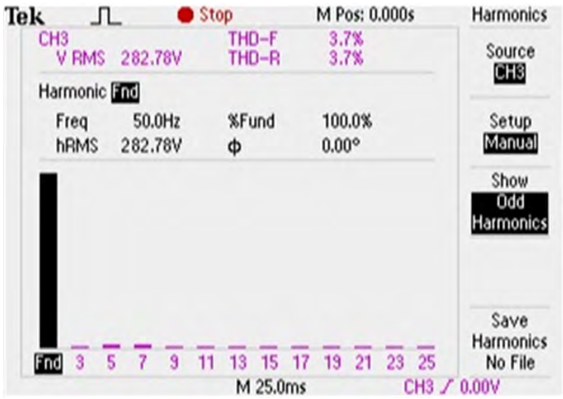

FIGURE 31. Experimental voltage thd of thirty-one level inverter.

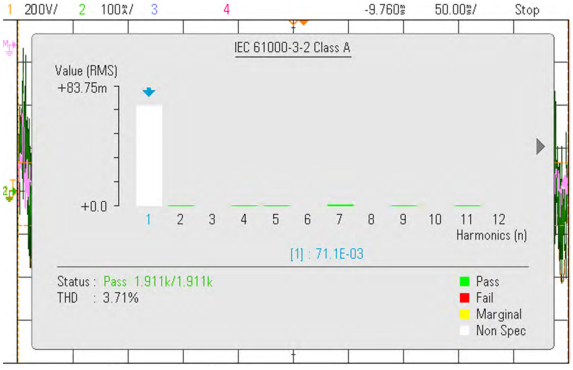

FIGURE 32. Experimental current thd of thirty-one level inverter.

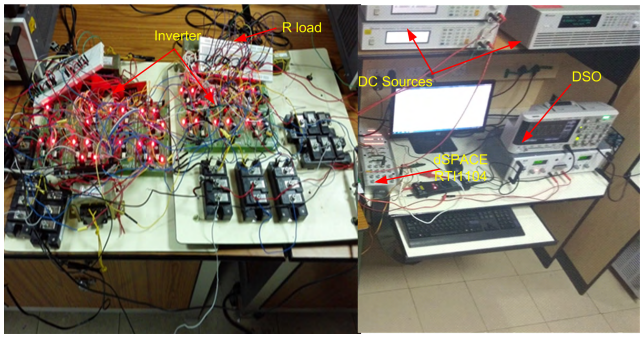

FIGURE 33. Experimental step-up of inverter.

as per IEEE standards are shown in Figure.31 and Figure.32 respectively.

The presented topology provides seven-level and thirty-one level output voltage with only 6 and 10 switches respectively in asymmetrical conditions. Under simulation a THD value of 3.62% is obtained using SIMULINK. under experimental conditions the computed THD value is 3.7%. The ability of presented multilevel inverter topology has been verified using both the experimental setup and the simulation and the outcomes are presented for both conditions. The experimental output parameters are shown in Table 5.

TABLE 5. Experimental output parameters.

Inverter	Load	Vo(V)	Io(A)	Po(W)	VTHD	ITHD
Theoretical values	RL	405	4	1.6kW	3.62	3.71
Simulation Values	RL	405	4	1.6kW	3.62	3.71
Experimental values	RL	400	4	1.568kW	3.7	3.71

VII. CONCLUSION

The proposed inverter is tested experimentally with resistive and inductive loads. The output waveforms obtained during the resistive load test clearly show that the phase angle between current and voltage is zero. And the inductive load testing results show that the current is lagging voltage. To test the robustness of the proposed scheme, a load disturbances test is conducted. It is observed that the proposed topology is well stabilized under load disturbances conditions. The presented topology provides seven-level and thirty-one level output voltage with only 6 and 10 switches respectively in asymmetrical conditions. Under simulation a THD value of 3.62% is obtained using SIMULINK. under experimental conditions the computed THD value is 3.7%. The ability of presented MLI topology has been verified using both simulation and experimental setups and the results are demonstrated for both conditions. The suggested topology is appropriate for the integration of medium-voltage renewable energy and power quality improvement in DVR, DStatcom and FACTs.

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