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Reinforced Droop for Active Current Sharing in Parallel NPC Inverter for Islanded AC Microgrid Application

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Abstract: The paper investigates the current sharing in parallel 3-level Neutral point clamped inverter for islanded AC microgrid application. In Distributed generation, parallel power electronic interface based microgrid suffers from power quality issues due to inaccurate output current sharing. To address the current sharing problem, the paper proposes an improved droop technique that reinforces the droop loop by infusing the incurred voltage drop accountable for inaccurate current sharing at the inverter output. The control based on droop reference is bounded with regard to output current since the output impedance influences the output current of the inverter largely. Besides that, the parallel NPC inverter also suffers from dc link voltage imbalance due to neutral currents. To address these issues a control strategy is proposed in the research work in which the processed DC offset is incorporated into the reinforced droop loop and the generated reference is utilized with feedback control to accurately share the currents under linear and nonlinear load conditions. The effectiveness of devised reinforced droop strategy is realized in MATLAB/Simulink environment and experimental validation is carried out with the field-programmable gate array as hardware interface to the hardware laboratory prototype of parallel NPC inverter.

Keywords: distributed power generation; 3-level Neutral point clamped inverter; reinforced droop control; field programmable gate array; islanded microgrid; circulating current

1. Introduction

In recent times, the demand of clean energy concerning the environmental issues and the expense involved in the power generation have brought drastic change in production of electrical power in terms of scale, system and economics of generation. With the penetration of renewable energy sources like photovoltaic (PV) systems, wind and fuel cells, the distributed generation (DG) proves to be impeccable as sustainable, self-reliant, semi-autonomous power distribution system for residential power applications [1,2]. Particularly, the photovoltaic based generation systems produce direct current (DC) which has to be converted to alternating current (AC) either to feed the AC loads or integrate with the grid. The power electronic interface like an inverter integrates the DG with the grid forming autonomous loads. The complete setup with at least one DG connected via power electronic interface feeding the load irrespective of connection to the grid is termed as microgrid [3]. The DG, being connected to utility grid is termed as grid connected mode of operation of microgrid that always follows the frequency and voltage destined by the utility grid. The DG, not connected to the utility grid corresponds to islanded mode of operation which demands ample capacity of DG to ensure frequency and voltage support [4,5]. The micro source fed system's voltage is limited by the maximum possible voltage of the solar panels and the current is limited to the maximum rating of the semiconductor devices connected [6]. To inherit the merits of flexibility, heterogeneous power quality,

reliability and increased power level at the output, the inverters are destined to be connected in parallel. The choice of inverter also plays a prominent role in expanding the power level of the power system. Probable solution is to step up the voltage and to limit the current for which multilevel inverters (MLI) are most suitable. Among different multilevel inverters, three level Neutral Point Clamped (NPC) inverter is widely considered due to its low voltage rating of switches, dynamic response, however the regulated dc link voltage yields distortion less output [7,8]. Although, in early 1980, the NPC inverters are used for high and medium power applications, with the huge technical advancement in power electronic switches, they are most widely used for low voltage application(<1kV) during the last decade. The applications include solar PVs, wind, low voltage drive and electric vehicle [9–11]. The patent [12] and the literature [13] investigates and proves that the utilization of NPC inverter for low voltage application is beneficial especially for switching frequencies 5 kHz and above. Moreover, the 3-level NPC inverter has been an attractive solution for transformer less grid integration [14]. Besides all these developments, very few research work reports the application of multi-level inverters as power electronic interface, especially NPC inverters in modular microgrid. To explore the research gap corresponding to application of MLI in microgrid, the current research work investigates the deployment of 3-level NPC inverter as power electronic interface. Different parallel structures of microgrid were proposed in the literature [15]. Figure 1 shows the structure of microgrid opted for current research. It proves to be prerogative in terms of its scalability, size and augmentation of microgrid.

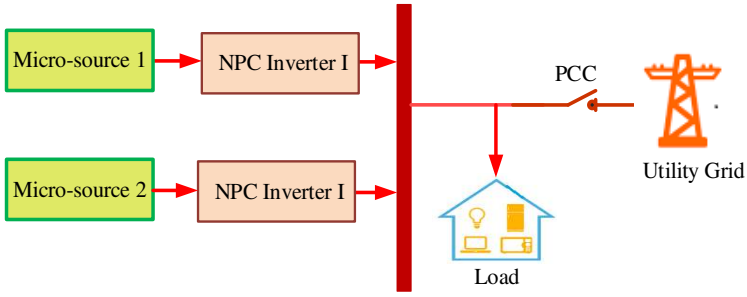


Figure 1. Structure of microgrid.

In the parallel inverter based microgrid, the circulating current at the output becomes a predominant problem which causes power loss, distortion and ineffective current sharing in the system [16]. Hence, it is necessary to break down the path of circulating current in parallel connected inverters. The traditional approach is to use a bulky isolation/frequency transformer or a reactor at the AC side which proves to be ineffective in efficiency prospective at high power levels [17]. The finest approach to minimize the circulating current is, to synchronize the parallel connected inverters with the appropriate control strategy. Different control strategies proposed in the literature [18–21] requires a control communication link between the parallel connected inverters. The control through communication link poses practical hardships like long communication line, additional costs, and reduced reliability. A wireless controller that could synchronize the parallel connected inverters are desired. A wireless droop control strategy is one such control that aims at load sharing through regulation of real and reactive power.

Nevertheless, conventional droop control strategy is good enough in power sharing, the parallel inverter control in islanded mode depends on the set point reference. Moreover, the conventional droop is incapable of controlling the inner dynamics of the inverter for step change in load and the current sharing is achieved at an expense of voltage. Hence, a droop control mechanism in combination with feedback control is required [22,23]. Besides that, the conventional droop mechanism exhibits slow dynamic response and inaccurate current sharing under nonlinear load conditions [24,25].

To improvise the performance of conventional droop strategy, different modified droop control strategies were proposed in the literature. To nullify the impedance effect of the both inverters,

adaptive virtual resistance-based droop strategy is implemented in which the line impedances are being added to the DG impedance. This method proves to be complicated due to the estimation of line impedance and at times require a communication link also [26,27]. As a further development, the literature [28] inoculates the effective design of virtual inductance and implementation of virtual adaptive control to suppress the circulating current among inverters of different capacities. In the presence of communication, Control Area Network (CAN) based compensation and an averaging technique during the absence of communication is suggested in [29] to improve the current sharing.

The current sharing control to reduce the harmonic currents was proposed in [30], creates a disturbance in frequency. The DC link protection ensured current sharing, is slow due to interdependence of the control variables [31]. To avoid the estimation of impedance, voltage compensation-based approach for accurate load sharing is proposed in [32] which can compensate the load effect alone. Recently, a compensatory approach through self-adjustment of droop gains for islanded microgrid application also suggest the same [33]. A robust droop control method proposed in [34,35] contributes proportionate power sharing and voltage regulation by adjusting droop gain, termed as amplification correction factor. The author further inoculates the root mean square (rms) factor that tends to compensate the droop effect along with load effect. Despite all the developments, the droop controllers are devoid of adherence to nominal voltage and frequency in process of accurate current sharing under influence of DC link voltage disturbance and nonlinear load condition. Although the effect of DC link voltage on the ac output of parallel inverter, and its droop- compensation to achieve the desired output, is inoculated in [36,37], it needs a nominal reference unchanged at the common load which is undermined during dynamic load conditions. The VI based droop technique emphasizes on current sharing over power sharing to ensure the overcurrent protection specifically under nonlinear load conditions [38].

Besides this, all the control strategies proposed in the literature was realized using a three-phase inverter and very few research works are being carried out on parallel NPC inverters for low voltage microgrid applications. Hence, the current research work emphasizes on the accurate current sharing control of parallel operated NPC inverters.

As NPC inverters are prone to unbalance DC link voltage, the effect of DC link voltage unbalance needs to be eliminated so as to achieve an undistorted output at the inverter. Hence, the paper contributes a simple and efficient droop control to enhance the accuracy of power sharing in parallel operated NPC inverters with balanced DC link capacitor voltage. The droop control strategy put forth in the current work reinforces the droop loop by infusing the visible voltage drop accountable for the voltage deviation at the common output terminal. The significance of active current sharing accuracy is determined by the P-V based droop loop reinforced by the compensatory voltage droop and reactive current sharing accuracy is ascertained by the Q-f droop.

To enhance the inner dynamics of the system under transient operation of inverters and transient load conditions, the voltage and current deviation need to be processed further to achieve accurate current sharing. The droop reference generated is utilized in Proportional–Integral (PI) controller and proportional–resonant controller in feed forward cascaded control loop to retain the stability [39,40].

The distinct feature of the proposed reinforced droop control:

- The droop function enables to share current accurately with both linear and nonlinear loads;
- The cascaded control loop improves the system dynamics;
- Robustness of the system is achieved;
- Performance analysis of NPC inverter with droop control is investigated.

The paper reports the system model and cross current analysis in islanded microgrid in Section 2. The proposed droop control strategy with the feedback control scheme is detailed in Section 3. The simulation and experimental validation results are analyzed in Section 4. The scope of research is limited to secondary control of parallel inverters pertaining to the availability of load at the laboratory. Section 5 concludes the research work in future direction.

2. System Model and Cross Current Analysis in Islanded Microgrid

The system model constitutes a parallel NPC inverter fed from independent isolated DC link whose output terminals are connected to common load as shown in Figure 2. Energy exchange between inverters necessitates the use of inductors for current sharing with an appropriate Pulse width modulation technique. When the parallel inverters operate in ideal conditions, the sharing inductor connected to each phase drastically reduces the zero sequence circulating (ZSC) current and the ZSC current could not find the path to flow through the parallel inverters. During non-ideal condition, the system experiences a finite phasor impedance difference between the sharing inductor and the inverter output voltage due to unique internal impedance of the device. The pole voltages of the inverters will also vary due to propagation delay in the gating technique. Aforementioned reasons tend to produce a voltage difference at the output of inverters. Unbalanced voltage gives rise to cross current that circulates as shown in Figure 3. In addition to that, the cross current drastically affects the voltage at the isolated DC link of the inverters. Hence the cross current needs to be eliminated in the parallel circuitry by the voltage regulation. Cross current analysis is carried out below.

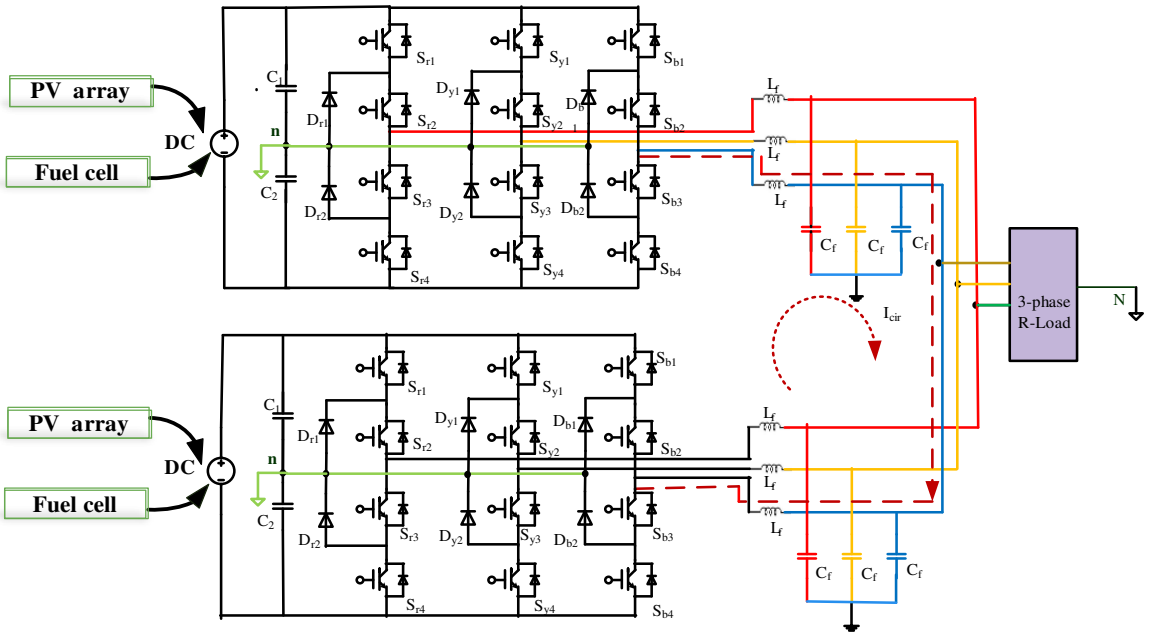


Figure 2. System model of parallel NPC inverter.

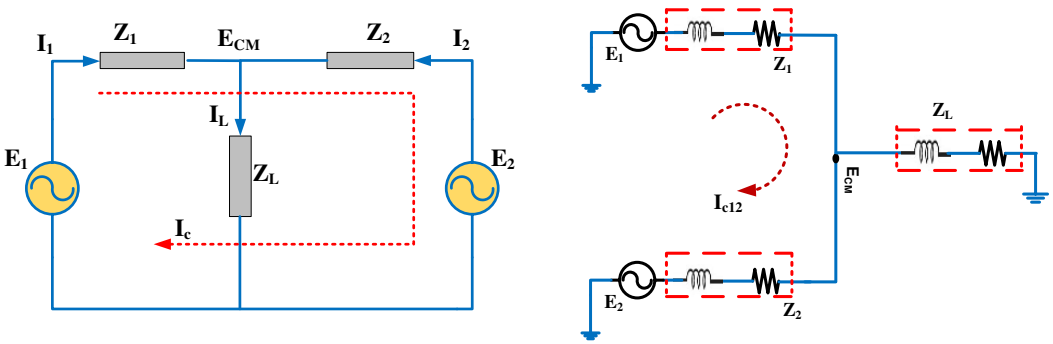


Figure 3. Equivalent model of parallel NPC inverter.

2.1. Circulating Current Analysis of Parallel NPC Inverter

Figure 3 represents the equivalent circuit of two inverters connected in parallel. The voltage E_1 and E_2 represents the output voltages of Inverter-1 and inverter-2 respectively. In general, if the

currents I_1 and I_2 be the output currents of Inverter-1 and Inverter-2, and Z_1 and Z_2 are the line impedances connected between the Inverter-1 and the common ac bus, Inverter-2 and the common bus respectively. I_L is the load current and Z_L is the load impedance. The small signal steady state analysis can be carried out based on the equivalent circuit of parallel inverters as shown in Figure 3 as follows. The mathematical analysis carried out in *s*- domain [41,42] is illustrated in this section.

The voltage at the common point, E_{CM} can be given as:

$$E_{CM}(s) = \left[\frac{\frac{E_1(s)}{Z_1(s)} + \frac{E_2(s)}{Z_2(s)}}{\frac{1}{Z_1(s)} + \frac{1}{Z_2(s)} + \frac{1}{Z_L(s)}} \right] \tag{1}$$

The currents of Inverter-1 and Inverter-2 can be expressed as:

$$I_1(s) = \frac{E_1(s) - E_{CM}(s)}{Z_1(s)} \tag{2}$$

$$I_2(s) = \frac{E_2(s) - E_{CM}(s)}{Z_2(s)} \tag{3}$$

Assuming the impedances of the Inverter-1 and Inverter-2 are equal then $Z_1 = Z_2 = Z$.

The circulating current is given as:

$$I_{c12}(s) = \frac{I_1(s) - I_2(s)}{2} \tag{4}$$

$$I_{c12}(s) = \frac{E_1(s) - E_2(s)}{2Z} \tag{5}$$

2.2. Conventional Droop Analysis

In islanded microgrid, although the frequency and voltage of parallel inverters are not destined by the utility grid, the parallel inverters should maintain a uniform voltage and operate at constant frequency at the output. The small deviation in voltage and frequency creates a large circulating current to flow through the terminals of parallel inverter. The most possible solution is to share the load equally among the inverters. Larger the current sharing error, larger the circulating currents. Droop strategy has been employed widely to share the load equally between the inverters. The droop strategy is based on the regulation of real and reactive powers. The droop strategy is inspired from the parallel operation of synchronous generators. Let P_1, Q_1 and P_2, Q_2 are the real and reactive powers of the Inverter-1 and Inverter-2. For low voltage applications, since the resistive component is also predominant. Hence the expression of real and reactive power is as follows:

$$P_i = \left[\left(\frac{E_i E_{CM}}{Z_i} \cos(\delta) - \frac{E_{CM}^2}{Zi} \right) \cos(\varphi) \right] - \left[\left(\frac{E_i E_{CM}}{Z_i} \sin(\delta) \right) \sin(\varphi) \right] \tag{6}$$

$$Q_i = \left[\left(\frac{E_i E_{CM}}{Z_i} \cos(\delta) - \frac{E_{CM}^2}{Zi} \right) \sin(\varphi) \right] - \left[\left(\frac{E_i E_{CM}}{Z_i} \sin(\delta) \right) \cos(\varphi) \right] \tag{7}$$

where $i = 1, 2, \ldots, n$; δ_i represents the phase angle of inverter impedance; Φ_i represents the angular difference between inverter and the load impedance.

Decoupling the above equations, by approximating the impedance to be inductive purely, the expressions (7) and (8) can be approximated as:

$$P_i = \left(\frac{E_i E_{CM} \sin(\delta)}{X_i} \right) \tag{8}$$

$$Q_i = \left(\frac{E_i E_{CM}}{Z_i} \cos(\delta) - \frac{E_{CM}^2}{Zi} \right) \tag{9}$$

Approximating the quantity $\sin(\delta)$ to δ and $\cos(\delta)$ to unity, the real and reactive power are given as:

$$P_i = \left(\frac{E_i E_{CM}(\delta_i)}{X_i} \right) \tag{10}$$

$$Q_i = \left(\frac{E_i E_{CM}}{X_i} - \frac{E_{CM}^2}{Xi} \right) \tag{11}$$

From the above expressions, it can be inferred that the deviation in load angle is directly proportional to the deviation in real power i.e.,

$$\Delta\delta \propto \Delta P \Rightarrow \Delta\delta \cong m\Delta P \tag{12}$$

Similarly, the reactive power aberration is directly proportional to the voltage deviation i.e.,

$$\Delta E \propto \Delta Q \Rightarrow \Delta E \cong m\Delta Q \tag{13}$$

The droop concept is thus established by inferring a linear relationship among the quantities P, Q, δ, E. Since the load angle is destined by the frequency, the droop equation can be established as given below:

$$f* = f - m_p P \tag{14}$$

$$E* = E - n_q Q \tag{15}$$

From the literature, the effect of droop coefficients m, n on the system stability plays a major role in the system performance. In islanded mode, the droop characteristics are configured based on the predefined loads, unlike the grid connected mode where it follows the dominant inductive line impedance [43]. The system considered for the research work operates in islanded mode and the predominant load impedance would be resistive, R_i. The real and reactive power of the system can be approximated as:

$$P_i = -\left(\frac{E_i E_{CM}}{R_i} - \frac{E_{CM}^2}{Ri} \right) \tag{16}$$

$$Q_i = \left(\frac{E_i E_{CM}(\delta_i)}{X_i} \right) \tag{17}$$

The literature [44] suggests that the conventional P-f and Q-V droop characteristics poses the problem of instability resulting in inaccurate power sharing. A negative feedback regulation facilitates the control loop to modify the output impedance of the system to be resistive. Hence the conventional droop control takes the form of P-V and Q-f droop termed as reverse droop.

The droop equation of the reverse droop are as follows:

$$E* = E - m_p P \tag{18}$$

$$f* = f - n_q Q \tag{19}$$

According to the Equations (16) and (17) the active power deviation is directly proportional to voltage deviation and same as the error.

3. Proposed Reinforced Multi Loop Control Strategy

3.1. Reinforced Droop

Figure 4 illustrates the proposed reinforced droop control strategy for current sharing in parallel inverters. The proposed droop strategy conceives a target to compensate the voltage deviation due to reverse droop effect and to ensure the system to share the currents accurately. Since an NPC inverter, is the power electronic interface in the current research work, the reference has to be generated such that the voltage at the dc link capacitors of the inverters are balanced during parallel operation.

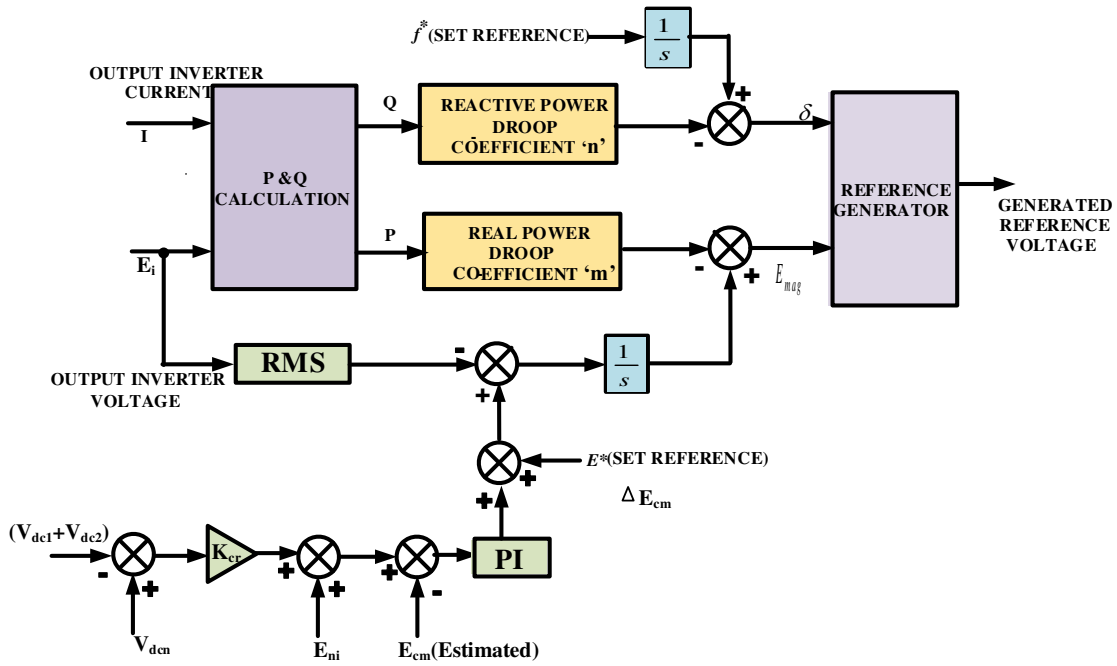


Figure 4. The proposed reinforced droop control.

The proposed droop controller's structure is being inspired by the robust droop controller proposed in [26]. A compensatory approach is carried out to guarantee the steady state deviations of voltage and frequency to be negligible. In general, the islanded micro grids, are characterized by absence of inertia, resistive line impedance and controllable power band due to the high penetration of renewable energy sources.

The control strategy exploits the advantage of the controllable bandwidth of the power delivered to the inverters. A dual droop regulation is put forth to estimate the compensating error. A slight deviation in voltage delivered to the inverter due to the imbalance of dc link capacitors at the source side triggers a huge variation in root mean square (RMS) voltage at the common load. This effects the active power delivered to the load. Hence a voltage based droop is proposed to extract the deviation in dc link voltage.

$$V_{dc} = V_{dc1} + V_{dc2} \tag{20a}$$

$$\Delta V_{dcn} = V_{dcn} - V_{dc} \tag{20b}$$

where V_{dc} is total DC link voltage; $V_{dc1,}$ V_{dc2} are dc link capacitor voltage, V_{dcn} is Nominal DC link voltage; ΔV_{dcn} is the deviation in dc link voltage.

The deviation pertaining to voltage being absorbed by the inverter and voltage being delivered to the inverters is processed by the droop gain. The proportionate voltage deviation is appended to

modify the nominal output voltage of the inverters thereby the RMS magnitude of set reference is modified. The mathematical expression is as follows:

$$E_{cm}{}^{*} = E_{ni} + K_{cr}(\Delta V_{dcn}) \tag{21}$$

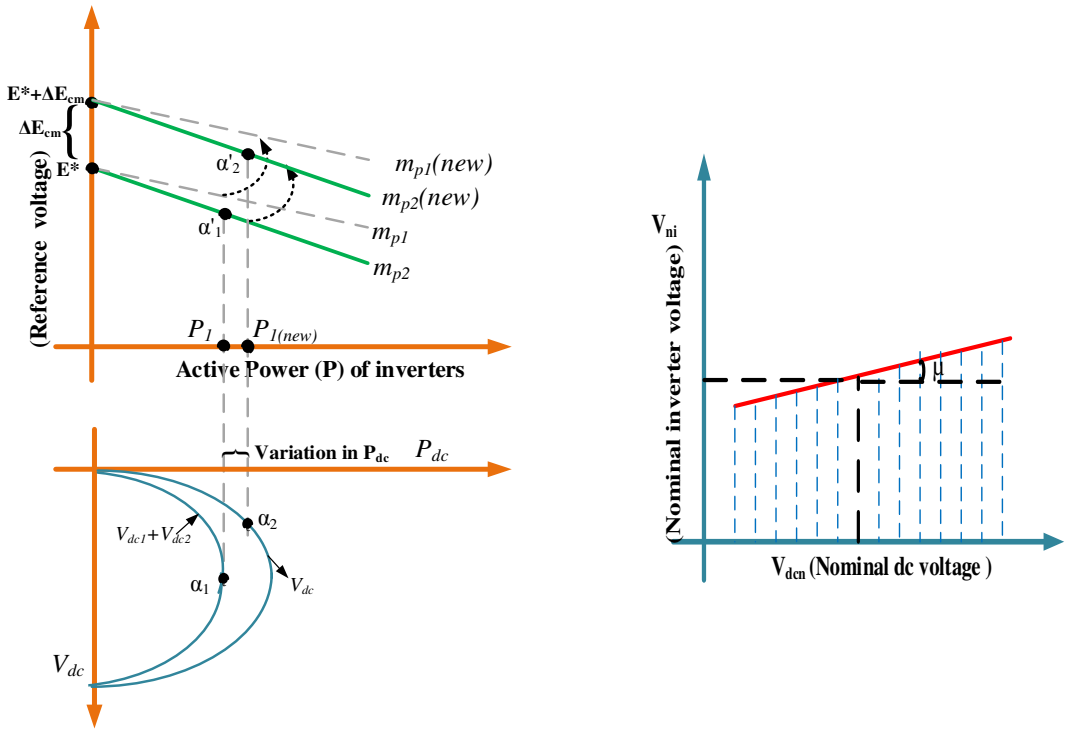
where E_{ni} is the nominal output voltage of inverter; K_{cr} is the droop correction factor; E_{cm}* is the modified reference generated at the common bus.

A considerable bandwidth of the droop gain is set, so as to avoid the influence of dc link voltage on the desired RMS AC magnitude in terms of power quality. This also helps in determining the droop error accurately. For a sudden change in load, the voltage and frequency deviation at the common point has to be restored in order to eliminate the circulating current between the inverters. Hence amplitude regulation is carried out by the evaluation of the voltage deviation and the same is processed via a PI controller. The regulated amplitude is appended to the set reference thereby restoring the output voltage amplitude and frequency at the common bus. The expression is as given in Equation (22).

$$\Delta E_{cm} = K_p(E_{cm}{}^{*} - E_{cm}) + \frac{K_i}{t}\int_0^t (E_{cm}{}^{*} - E_{cm}) \tag{22}$$

where ΔE_{cm} is the voltage deviation at common bus; K_p is proportional coefficient; K_i is Integral coefficient.

The supplementary loop reinforces the robust droop control in achieving the voltage and frequency deviation to be zero during both steady state and transient conditions. Figure 5a illustrates the bandwidth of the voltage-based droop loop and Figure 5b illustrates the droop characteristics of robust droop method and the influence of dc link voltage absorbed at the input of inverter.



(**a**) Bandwidth of voltage droop

(**b**) Droop graph of dc link voltage at the inverter

Figure 5. Characteristic droop analysis of proposed method.

Where m_{p1} and m_{p2} are coefficients of Inverter-1 and Inverter-2 with conventional droop method and m_{p1} (new) and m_{p2} (new) are coefficients of proposed droop method. Figure 5 illustrates the interaction of the dc link voltage variation, when the power delivered at the dc link of the inverter is greater than the power output of the inverter. The inverter 1 operates at a point α'_1 when the voltage absorbed at the dc link is less than the nominal voltage. The operating point of inverters shifts from α'_1 to α'_2 by the supplementary reinforced droop loop drop which shifts the droop line from E^* to $(E^* + \Delta E_{cm})$. Without loss of generality, the deviation pertaining to desired voltage at the common point is also included to achieve zero voltage and frequency deviation.

3.2. Multi Loop Feedback Control

The multi loop voltage and current control is necessary to suppress the total harmonic Distortion due to the distortions when loaded with linear and nonlinear load. The most commendable advantage of multi loop controller is that, it yields optimized best performance by being independent of relative errors. The control structure is modelled by the proportional–resonant (PR) controller and proportional–integral (PI) controller. The third harmonics are eliminated by the appropriate selection of sinusoidal pulse width modulation (SPWM) technique. Fundamental harmonic is suppressed by the tuning the controller by tracking the currents under different loads. The PR controller is implemented in the voltage loop to nullify the steady state error. The output of the voltage controller acts as reference to current controller. The closed loop control is illustrated in Figure 6.

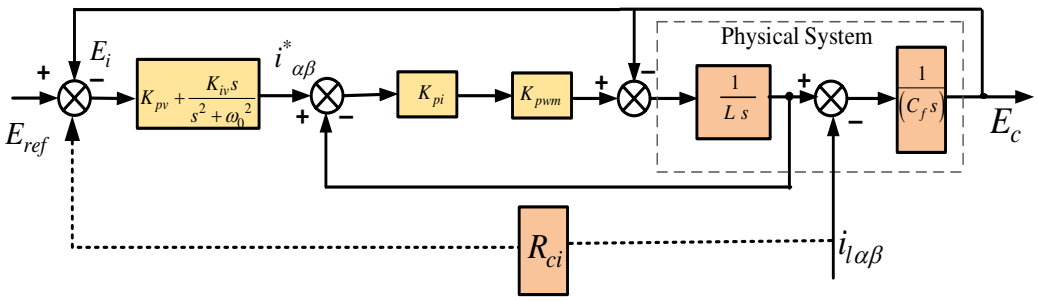


Figure 6. Closed loop control block diagram of 3-level inverter.

According to the literature, the virtual or compensating resistance if enabled, will be equivalent to the pervasive output resistance of the inverter at fundamental frequency. If the virtual impedance is crippled, the overall output impedance of the system is meant to be negligible at fundamental frequency. By analyzing the closed loop dynamics of the system, the control is reduced using Mason's reduction.

The control signal can be deduced as:

$$E_c(s) = \left[\frac{\left(K_{pv}+\frac{K_{iv}s}{s^2+\omega_0{}^2}\right)(K_{Pi})\left(\frac{1}{1+1.5T_s s}\right)}{L_f C_f s^2+\left(\left(C_f s+\left(K_{pv}+\frac{K_{iv}s}{s^2+\omega_0{}^2}\right)\right)(K_{Pi})\left(\frac{1}{1+1.5T_s s}\right)\right)+1}\right]E_{ref} - \left[\frac{L_f s+(K_{pi})\left(\frac{1}{1+1.5T_s s}\right)}{L_f C_f s^2+\left(\left(C_f s+\left(K_{pv}+\frac{K_{iv}s}{s^2+\omega_0{}^2}\right)\right)(K_{Pi})\left(\frac{1}{1+1.5T_s s}\right)\right)+1}\right]i_{l\alpha\beta} \quad (23)$$

Although the proposed droop control, restores the voltage, the influence of control parameters on the system at fundamental frequency need to be analyzed. The overall control diagram of the parallel NPC inverter is depicted in Figure 7. Estimating the real and reactive powers that can be delivered to load, proposed reinforced droop method generates the reference with supplementary droop loop. The Multi loop feedback controller utilizes the reference to generate the control signal for SPWM block.

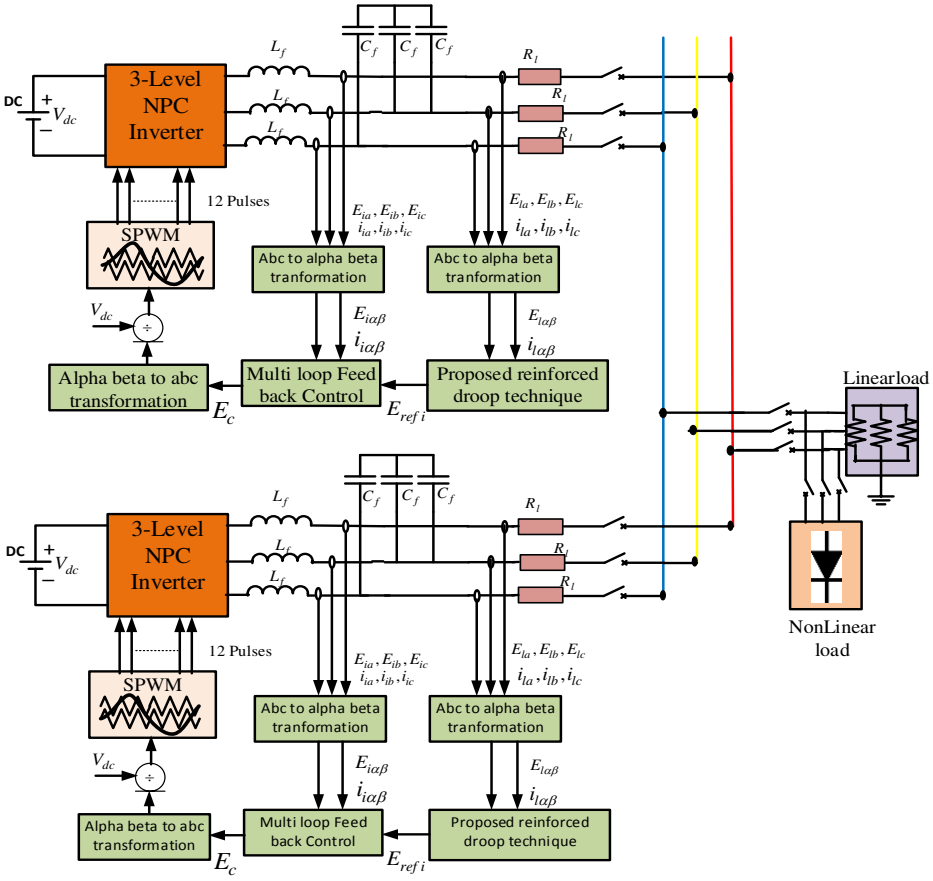


Figure 7. Overall control block diagram of the parallel 3-level NPC inverter for islanded microgrid.

4. Results and Discussion

4.1. Simulation Results

The Parallel 3-level NPC inverter for islanded microgrid application is simulated in the MATLAB Simulink environment to validate the proposed control strategy. The power stage parameters and the control parameters are tabulated in Table 1. The design parameters for the simulation is approximated to the experimental values to validate the accuracy of load sharing. The Simulation carried out, investigates the system performance in terms of current sharing when: (i) Both inverters operate in parallel under linear and nonlinear load conditions; (ii) Transient parallel operation of inverter with one of the inverters is switched on and off under linear and nonlinear load condition. Since the loads are balanced, simulation waveforms per phase is shown.

Table 1. System and control parameters.

Description	Parameter	Value
Nominal Voltage	$E_{0l\text{-}l}$	208 $V_{l\text{-}l}$(V)(rms)
Filter parameters	L_f, C_f	5 mH, 50 µF
Line resistance	R_{l1}, R_{l2}	1, 1.2 ohms
Switching frequency	f_s	5 kHz
Droop Coefficient	m_{p1}, m_{p2}	0.0012, 0.00168
Linear Load current	I_L	3 A(rms) Maximum
Nonlinear Load current	I_L	3 A(rms)
Cut off frequency	F_{cutoff}	2 kHz
DC Droop correction	K_{cr}	0.35
Voltage Compensation	K_p, K_i	0.02, 0.5
Multi loop- Voltage PR controller	K_{pv}, K_{iv}	0.68, 100
Multi loop current P control	K_p	1.36
The feedback resistance	R_{ci}	1 (Since the rating of inverters are identical)

4.1.1. Under Linear Load Conditions

The parallel system is made to operate under resistive load and the corresponding line voltage with and without filter is depicted in Figure 8. The inverter peak to peak (pk-pk) output voltage is 600 V (pk-pk) without filter and 592 V (pk-pk) with filter.

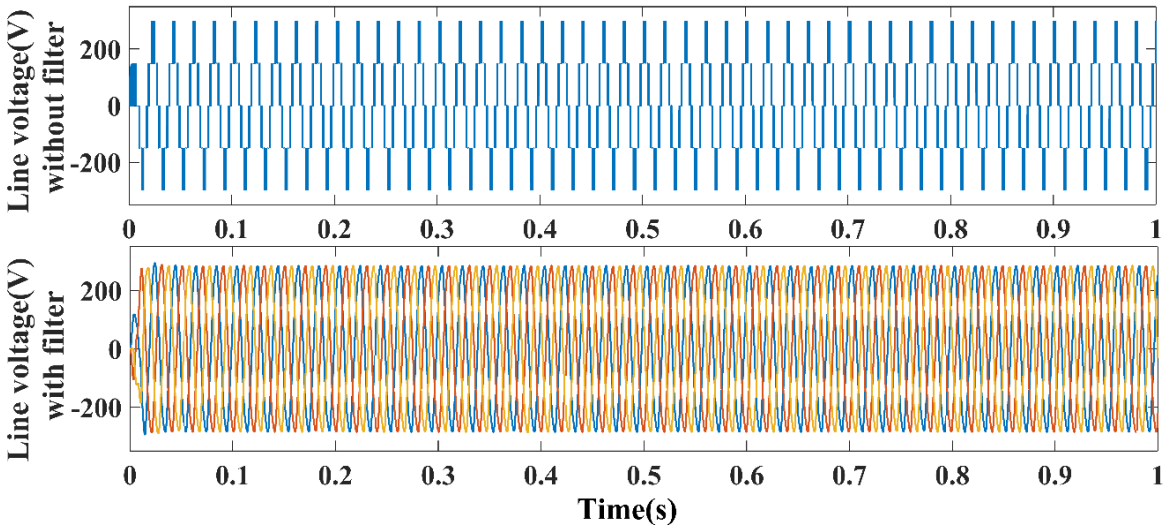


Figure 8. Line voltage of NPC inverter with and without filter.

Case (1): When both inverters operate in parallel

When both inverters operate in parallel, the current sharing through conventional droop strategy is investigated. The simulation result proves that, the currents of Inverter-1 and Inverter-2 are 2 A (pk-pk) and 1.6 A (pk-pk) whose sum equals the load current of 3.6 A (pk-pk). Although the currents are in phase, the conventional droop method poses a current sharing error of 11.1%. Figure 9 depicts the current sharing of inverters with conventional droop strategy. Figure 10 represents the current sharing with the proposed control strategy. With the proposed control, the current sharing accuracy is increased with Inverter-1 and Inverter-2 sharing a load current of 1.79 A (pk-pk) and 1.76 A (pk-pk) whose sum equals the total load current of 3.6 A (pk-pk).

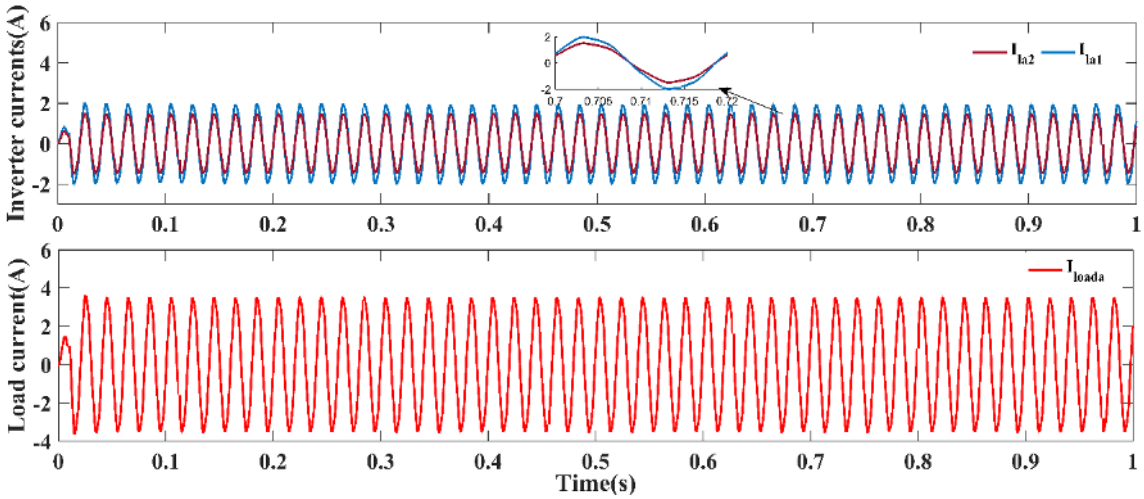


Figure 9. Current sharing during conventional droop control.

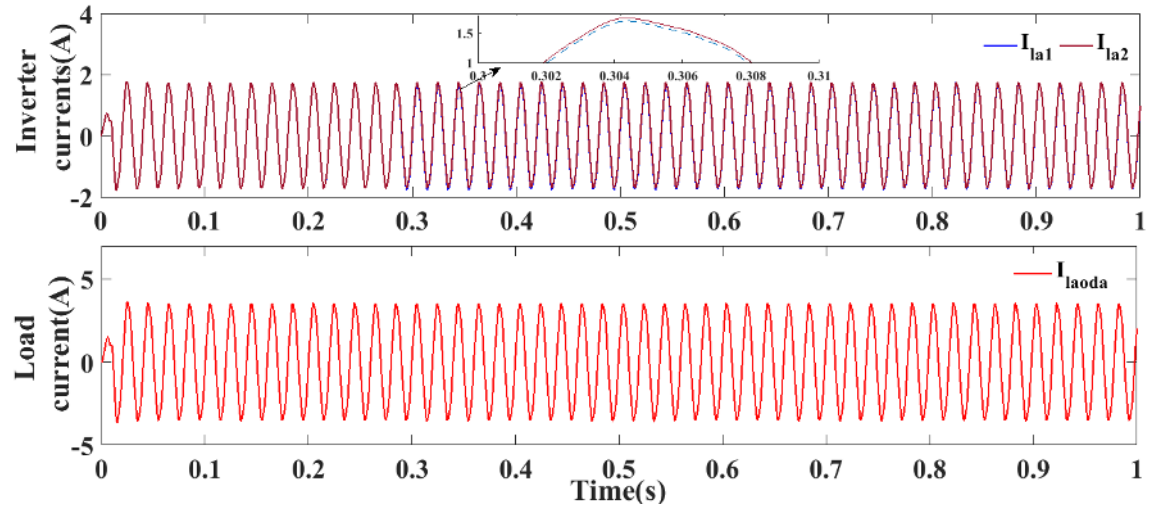


Figure 10. Current sharing with proposed reinforced droop control.

Case (2): Transient analysis of inverters during parallel operation

A. Transient operation of inverters

Transient operation is carried out with sudden switching on/off of the inverter and the respective results are depicted in Figure 11. At simulation time 0.2 s, Inverter-2 is switched, till then only Inverter-1 is feeding the load. From 0.2 s, both inverters share accurately the current of 1.8 A (pk-pk) of the total load current of 3.6 A (pk-pk).

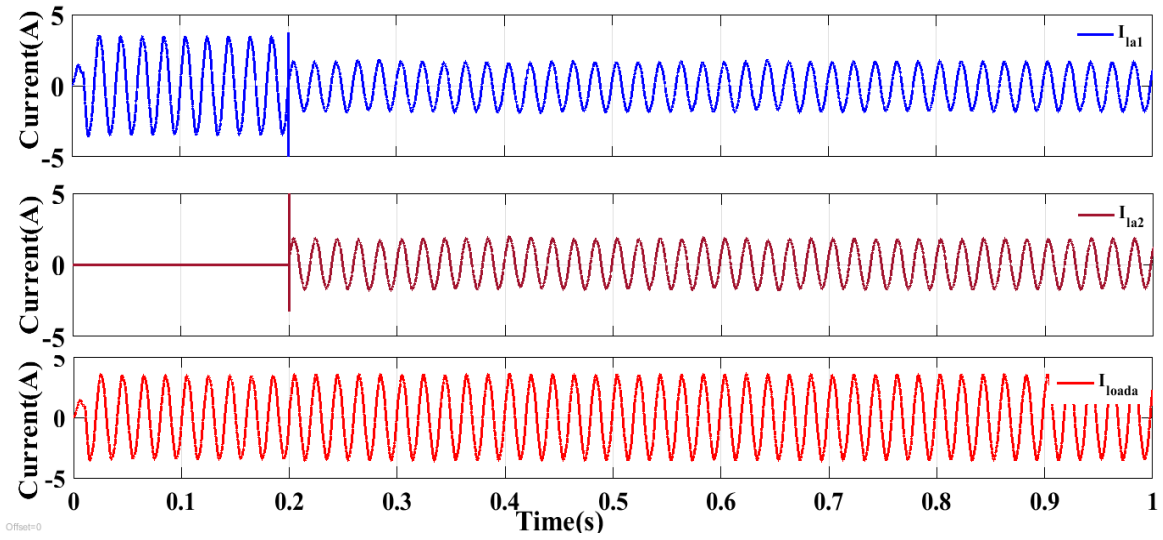


Figure 11. Current sharing during transient operation of parallel inverter.

B. Transient load current analysis

Figure 12 depicts the current sharing of parallel inverter during transient load condition. The load current of 3.8 A (pk-pk) is changed to 4.2 A (pk-pk) at 0.2 s and the same is changed to 4.2 A (pk-pk) at 0.6 s. The inverters share the load current accurately 1.8 A (pk-pk) each till 0.2 s and from 0.2 to 0.6 s the inverters share the currents of 2.1 A (pk-pk) respectively.

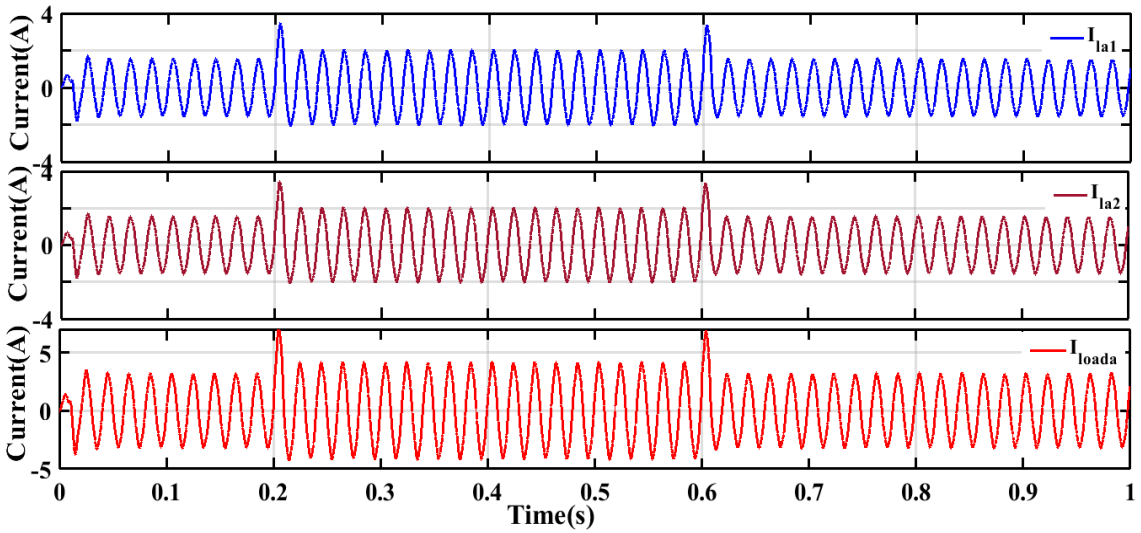


Figure 12. Parallel operation for transient load condition.

4.1.2. Under Non-Linear Load Conditions

Case (1): When inverters are in parallel

The parallel inverter when loaded with 3-phase diode rectifier, the output voltage of inverter with and without filter is depicted in Figure 13. The line voltage with and without filter are 600 V (pk-pk) and 592 V (pk-pk). Figure 14 illustrates the current sharing during transient operation of parallel inverters. The currents of 2.76 A (pk-pk) and 2.79 A (pk-pk) are shared accurately when loaded with total current of 5.6 A (pk-pk).

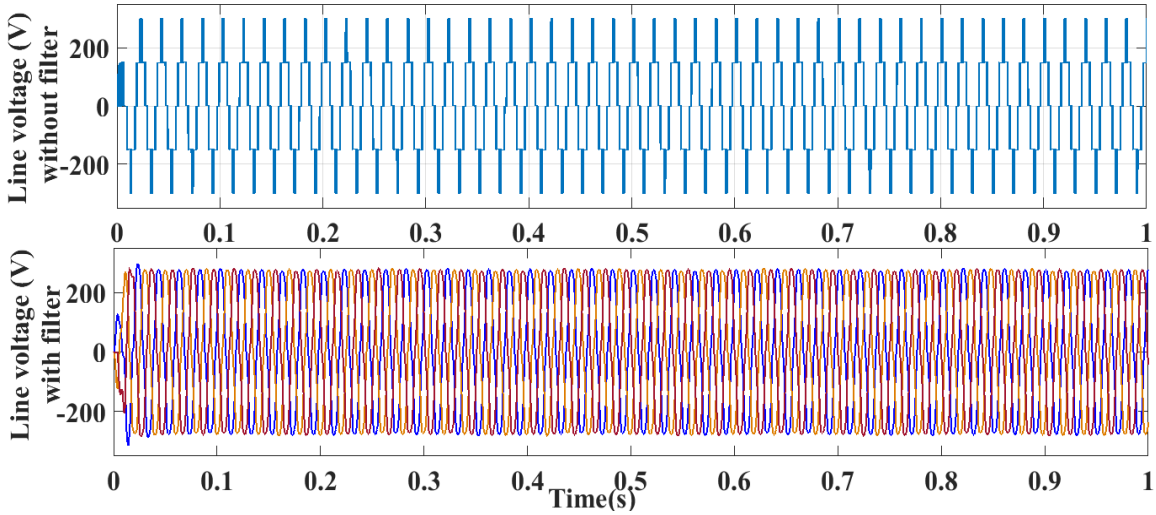


Figure 13. Line voltage of inverter with and without filter.

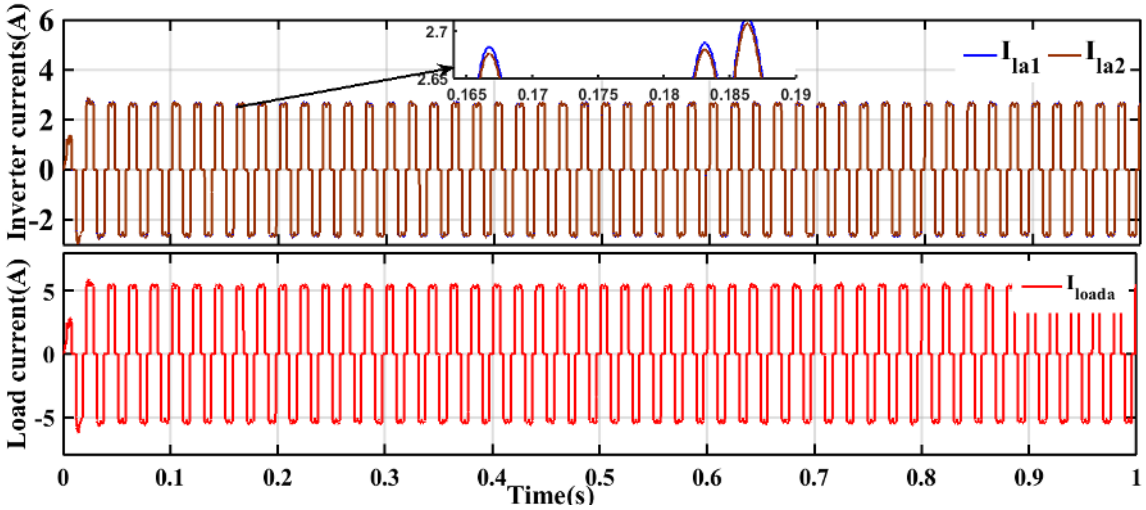


Figure 14. Current sharing with proposed method with nonlinear load.

Case (2): Transient analysis of parallel operated inverter with nonlinear load

A. Transient operation of parallel inverter

Even with nonlinear load, the current sharing takes place more accurately when one of the inverters is switched on/off. Inverter-2 is switched on at 0.2 s till then Inverter-1 share the full load. Figure 15 illustrates the transient operation of parallel inverter.

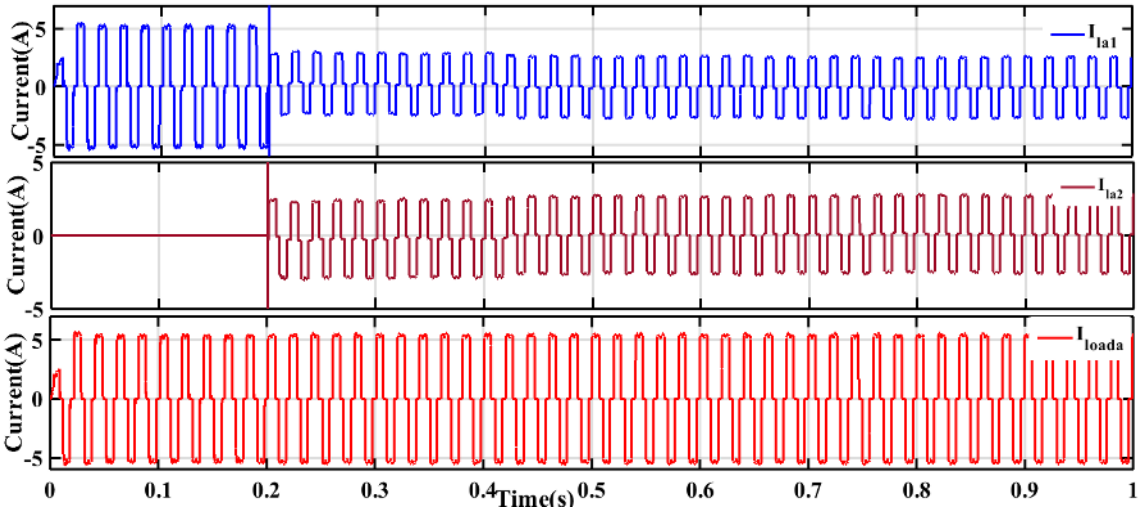


Figure 15. Transient operation of inverter with nonlinear load.

B. Transient load condition

To analyze the current sharing during the variable load conditions, the resistance connected to the rectifier load is changed at 0.2 s and again restored to the initial value at 0.6 s. Figure 16 exemplifies the accurate current sharing during the change in load.

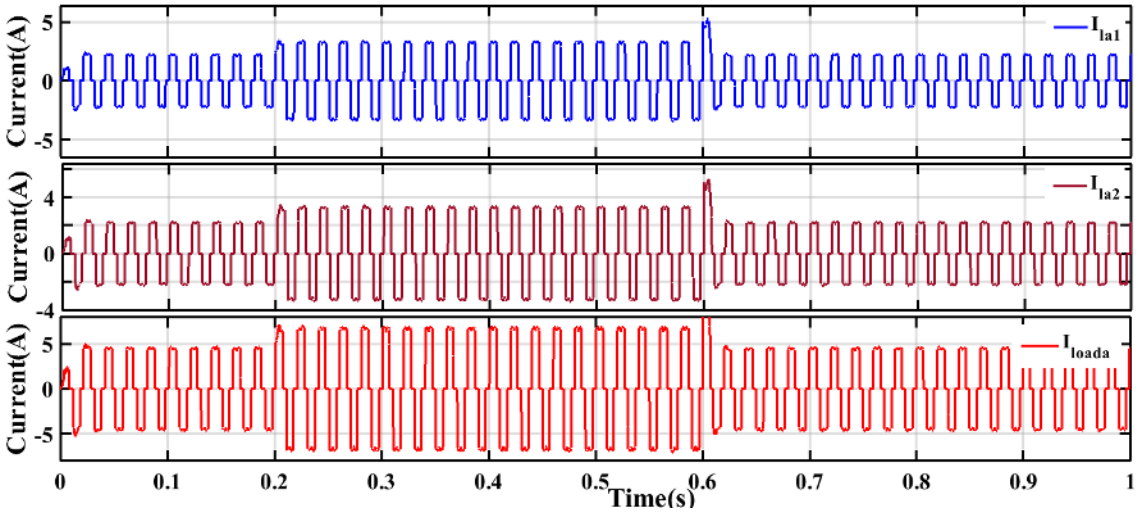


Figure 16. Current sharing during transient load condition.

4.2. Experimental Validation

4.2.1. Experimental Setup

The experimental validation is carried out with laboratory prototype model of two identical NPC inverters as shown in Figure 17. According to available supply voltage in the laboratory the NPC inverters operated at dc voltage of maximum 240 V. The DC voltage to the inverters are fed from the autotransformer connected to rectifier module. The voltage and current transducers, LEM LA 25-N and LV 50-P senses the output voltages and currents of the inverter. Since identical inverters are being used, the filter parameters like filter inductance L_f =5 mH, and capacitance C_f = 50 µF are used with each of the inverters. The control strategy implemented in the MATLAB Simulink is experimentally validated using Spartan-6 XC6SLX9 FPGA device as control target. The Simulink model implemented in MATLAB is converted to VHDL code and using Xilinx ISE 14.2 as software interface to dump the program in to FPGA board. The master and slave operating modes can be utilized due to the embedded function involved. The analog to digital converter in FPGA system converters the signals in digitized form to process the same. The JTAG link acts as interface between the analog to digital converter and the user at the hardware circuitry. Current sharing controller based on the proposed droop control is implemented in the functional block ADALINE of FPGA. The proposed reinforced droop generated reference is used to process the voltage and current error in feedback control. It uses proportional and proportional–resonant controller based on ADALINE function block. The control parameters are tuned by classic Ziegler-Nichols method. The droop control parameters are designed based on the IEC 60038 standard [45].

To demonstrate the effectiveness of proposed control strategy, the system is tested with both linear and non-linear loads, connected to the common bus/point of common coupling separately. The controller performance is evaluated based on the equal current sharing phenomenon. The output voltage of the inverter is demonstrated in Figures 18 and 19.

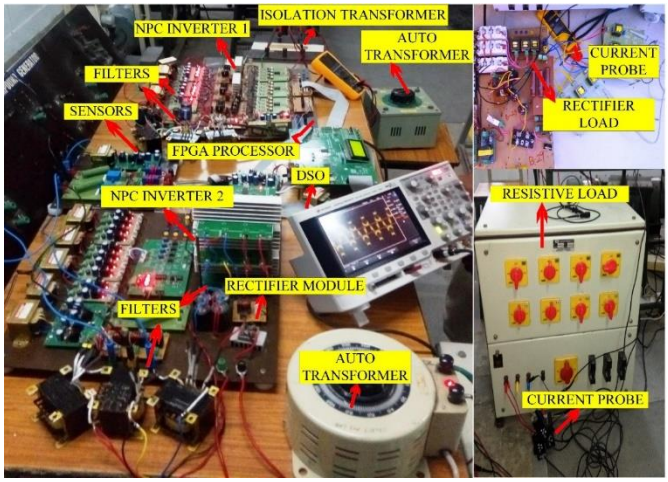


Figure 17. Hardware prototype for the experimental validation.

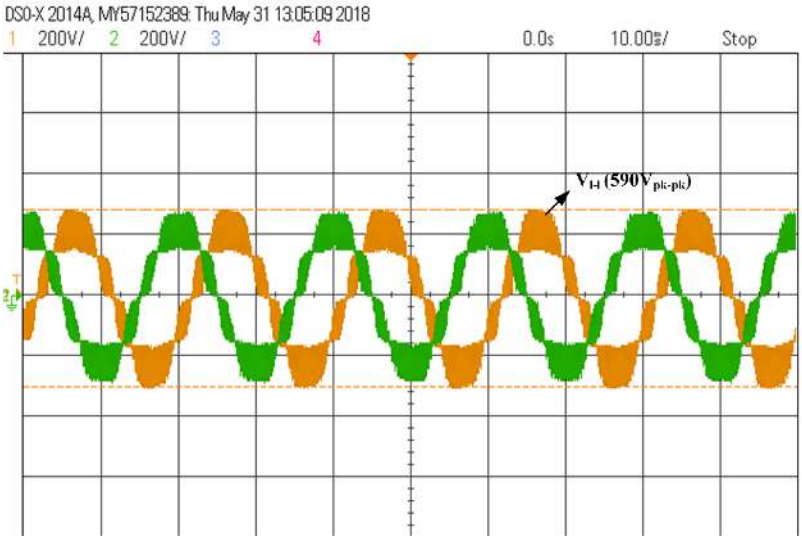


Figure 18. Output line voltage of NPC inverter.

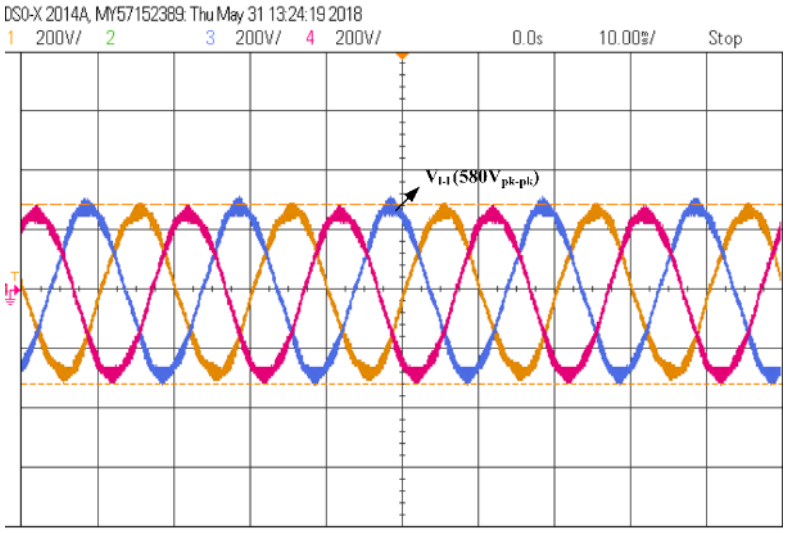


Figure 19. Output voltage of NPC inverter with filter.

4.2.2. Under Linear Load Conditions

Case (1): When both inverters operate in parallel

The Parallel NPC inverter is loaded with three phase resistive load at the common bus with maximum rms current of 1.5 Amps. Since balanced load is applied, per phase current of Inverter-1, Inverter-2 and load is analyzed. Figure 20 illustrates the current sharing with conventional droop control when loaded with total load current of 3.5 A (pk-pk). The conventional droop control does not constitute for accurate current sharing posing a current error of 0.35 A (pk-pk).

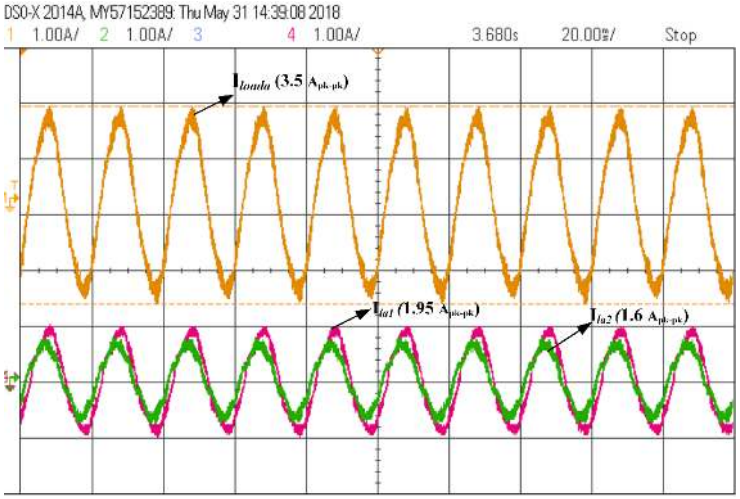


Figure 20. Output current of Inverter-1, Inverter-2 and load.

With the proposed control strategy, the effectiveness of current sharing is illustrated in Figure 21. The total load current of 3.5 A (pk-pk) is being shared by the inverters as 1.75 A and 1.70 A (pk-pk) more accurately.

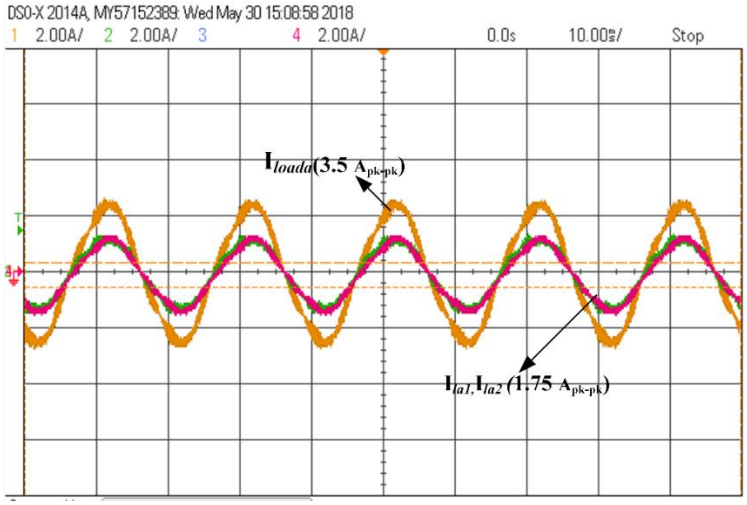


Figure 21. Output current of Inverter-1, Inverter-2 and load.

Case (2): Transient operation process and transient load analysis of inverter parallel operation

Transient analysis of inverters is carried out by transient operation of inverters and analysis of parallel operation inverters with transient load.

A. Transient Operation

The transient operation process of inverters constitutes sudden on and off of one of the inverters. The current sharing is analyzed with one of the inverters in off state. During initial condition, Inverter-2 is in off state and at 500 ms Inverter-2 switched on to operate both inverters in parallel. Figure 22 illustrates the performance of proposed control strategy with current sharing during the transient operation of inverters.

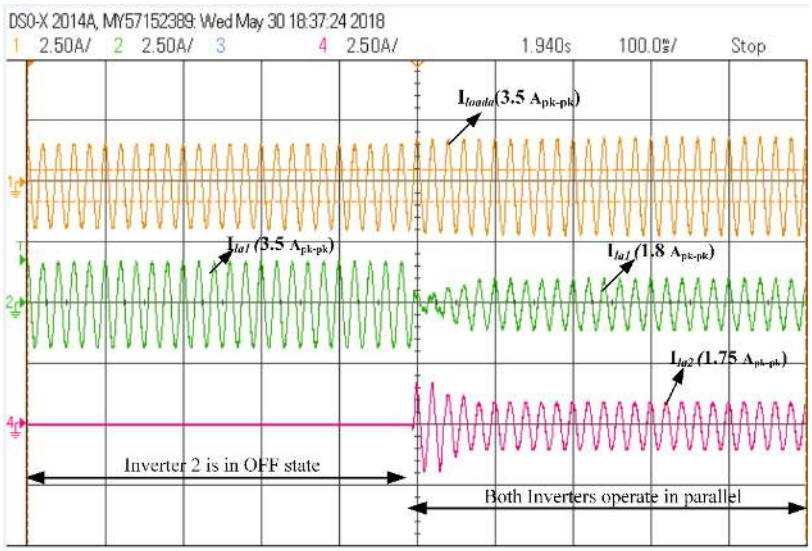


Figure 22. Current sharing during transient operation of parallel inverter.

B. Analysis of parallel operation under transient load conditions

Under transient load conditions, the load applied to the inverters is being varied to investigate the current sharing phenomenon. Figure 23 represents the change in load during parallel operation of inverter. During the parallel operation, the load current applied at the common bus is reduced from 4.2 A (pk-pk) to 3.2 A (pk-pk) and the again loaded from 3.2 A (pk-pk) to 4.2 A (pk-pk). Figures 24 and 25 illustrate the current sharing phenomenon where the accurate current sharing takes place between inverters irrespective of change in load. As illustrated in the Figures 24 and 25, both the inverters share 1oad accurately for step increase and decrease of total load.

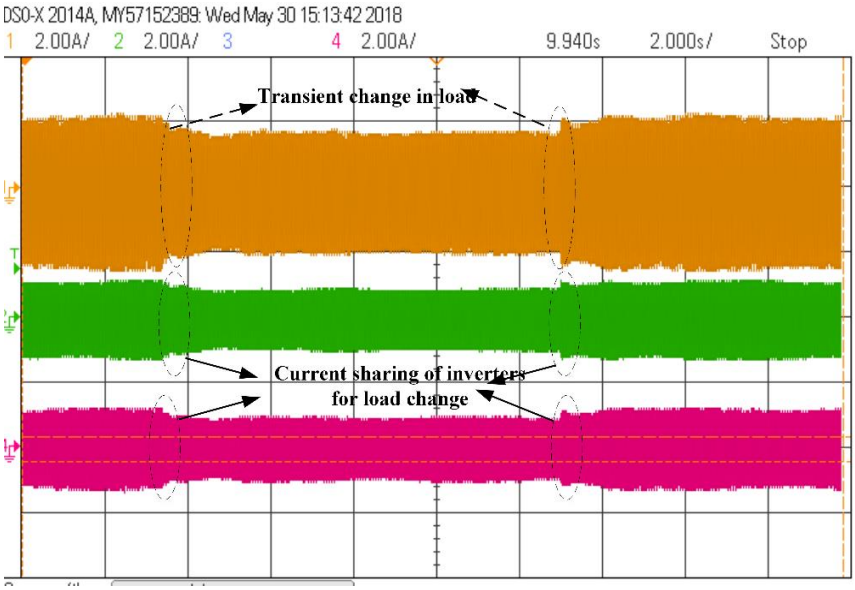


Figure 23. Load variation during parallel operation.

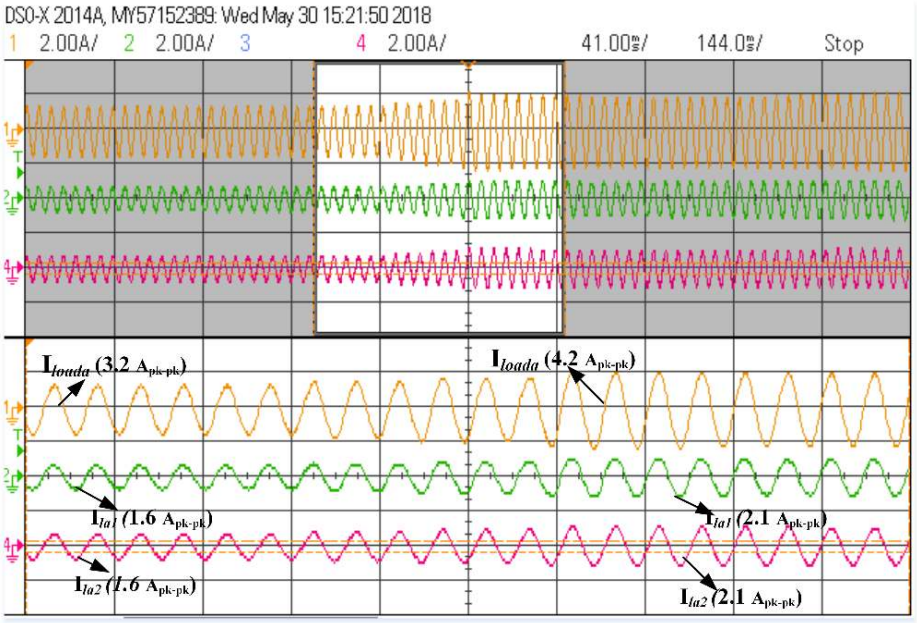


Figure 24. Parallel operation for increase in load.

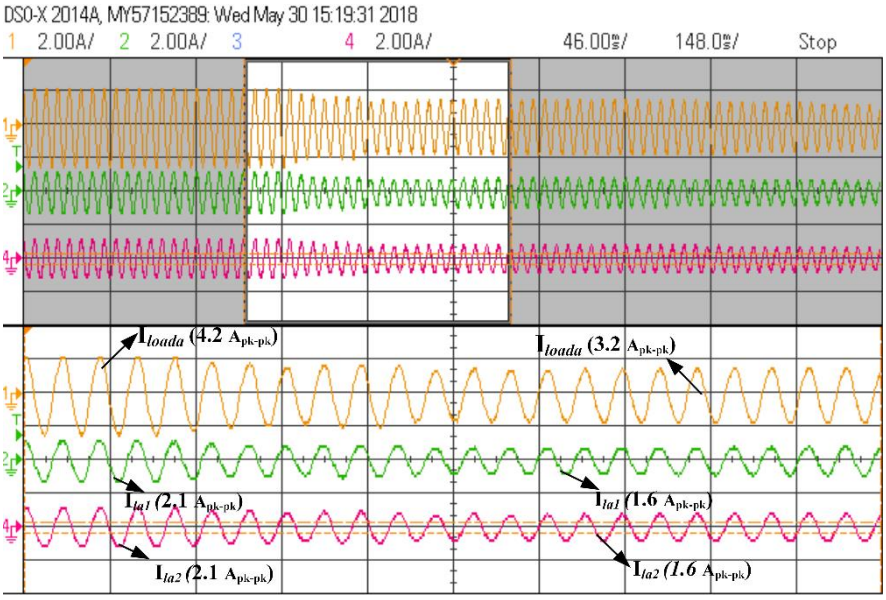


Figure 25. Parallel operation for decrease in load.

4.2.3. Under Non-Linear Load Conditions

Case (1): When both inverters operate in parallel

The research work also analyses the system behavior, when loaded with nonlinear load like a three-phase rectifier with resistive inductive load. Since the loads are balanced, voltage and current regarding one phase is displayed. Figure 26 shows the output voltage and current of an inverter with the rectifier load. During the parallel operation of inverters with rectifier load, the current sharing phenomenon is analyzed with line currents of inverters and load. Figure 27 represents the current sharing during the parallel operation of inverters with nonlinear load. With the ohmic resistance and inductance of 100 ohms and1.2 mH loaded to the rectifier load, the output currents of the inverters and load is distorted due to harmonics.

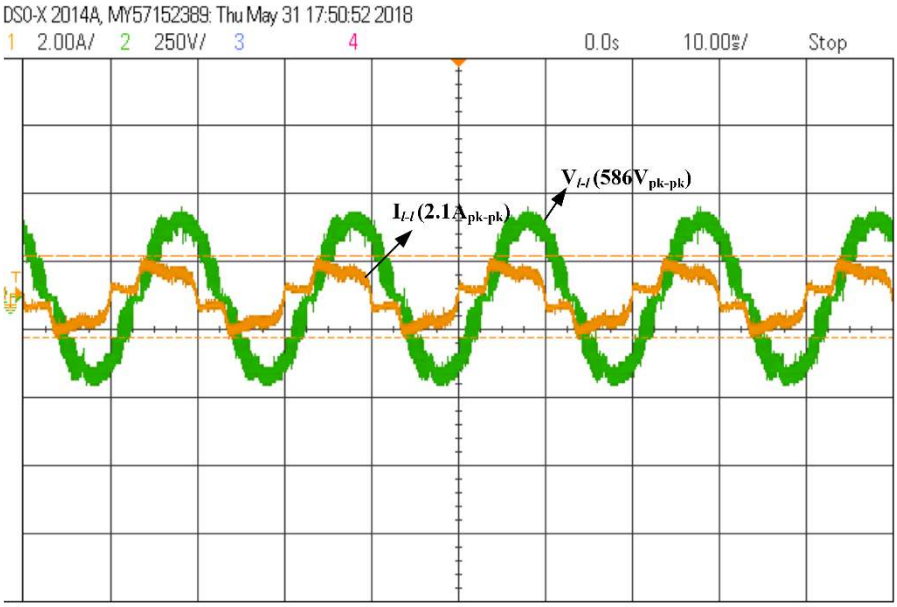


Figure 26. Output voltage and current of parallel inverter.

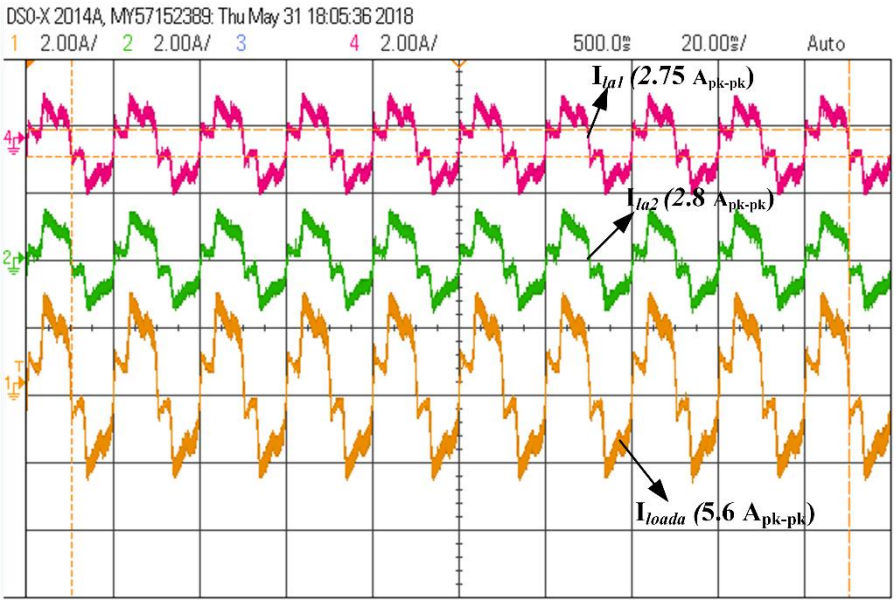


Figure 27. Output currents of Inverter-1, Inverter-2 and Load.

Case (2): Transient operation process and load analysis of inverter parallel operation

When one of the inverters is in off state and suddenly switched on with the rectifier load as nonlinear load. Figure 28 illustrates the current sharing during transient operation of the system. Although the sudden momentary switching on of one of the inverters creates an instability at that instant, the system gains stability and tends to share current accurately. Figures 29 and 30 explain the transient operation of the inverter under nonlinear load condition. Finally, Table 2 exemplifies the experimental results citing the pictorial result.

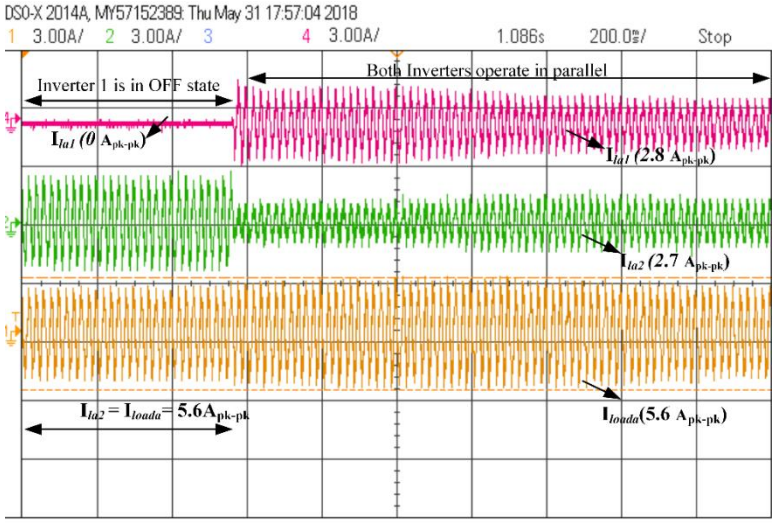


Figure 28. Transient operation of parallel inverters.

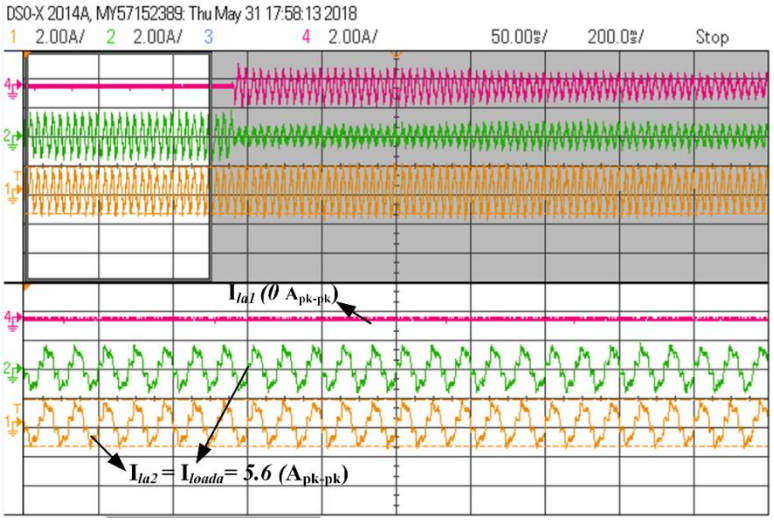


Figure 29. Current sharing when one of the inverters is in off state.

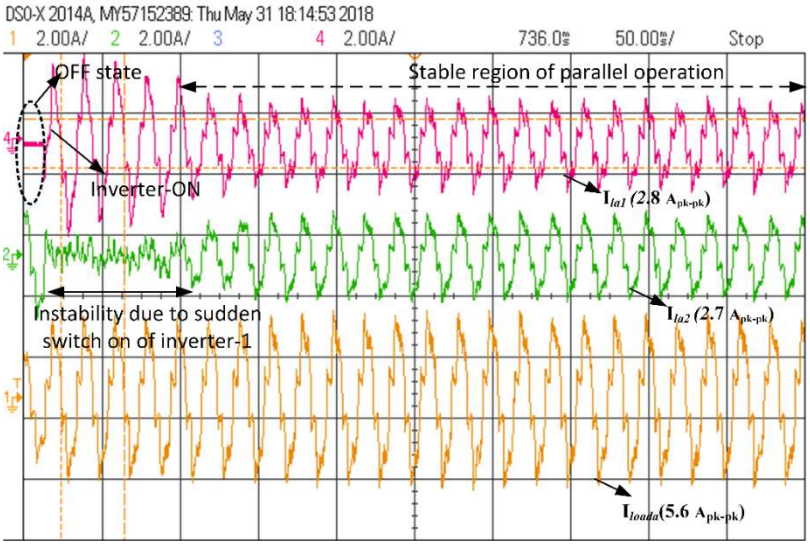


Figure 30. Current sharing during sudden switch on of the inverter.

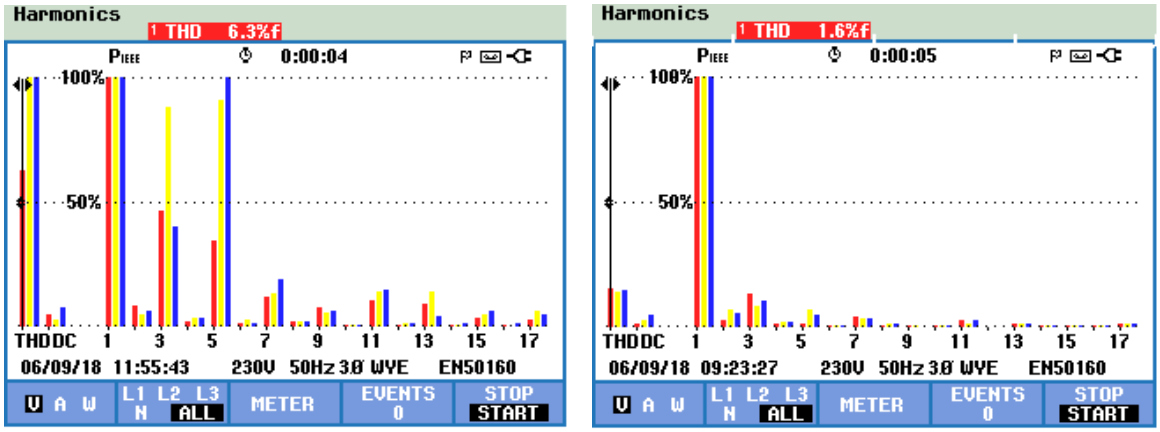
Table 2. Experimental result with figure citation.

Load Type		I_{La1}—Output Current of Inverter-1 in A (pk-pk)	I_{La2}—Output Current of Inverter-2 in A (pk-pk)	I_{Loada}—Total Load Current at the Common Bus in A (pk-pk)	Pictorial Depiction	Inference
Linear Load	Steady state operation with constant load	1.75	1.75	3.5	Figure 21	Accurate current sharing is achieved
	Transient operation with constant load	1.8	1.75	3.5	Figure 22	When inverter -2 is switched on at 500 ms, the current sharing is achieved much accurately in less than 50 ms
	Parallel operation for step change in load	2.1	2.1	4.2	Figure 24,	For increment of load current from 3.2 to 4.2 A, the rapid and accurate current sharing is achieved
		1.6	1.6	3.2	Figure 25	For a decrement of load current, rapid sharing is achieved
Nonlinear Load	Steady state operation with constant load	2.75	2.8	5.56	Figure 27	Accurate current sharing is achieved with 6.3% of total harmonic distortion
	Transient operation with constant load	2.8	2.75	5.56	Figures 28–30	For Sudden momentary switching of inverter, accurate current sharing is achieved and the system retains its stability in less than 50 ms.

$V_{l\text{-}l}$—line voltage at the common bus is 586 V (pk-pk) for nonlinear linear load, 580 V (pk-pk) for linear load.

4.3. Performance Analysis of NPC Inverter

The Parallel operation of NPC inverter performance is assessed by measure of power quality parameters like total harmonic distortion (THD) at the common load. The THD analysis is carried out with Fluke meter, measured at the common bus, which shows 1.6% when operating at linear load and 6.3% at nonlinear load in Figure 31a,b.



(**a**) (**b**)

Figure 31. (**a**) THD for non-linear load. (**b**) THD for linear load.

The crest factor of voltage and current at the common bus is as shown in Figure 32. The results suggest that the voltage and current meet the IEEE 519 standard [46]. From the results, it can be adjudged that the power quality is good enough during the parallel operation of inverters.

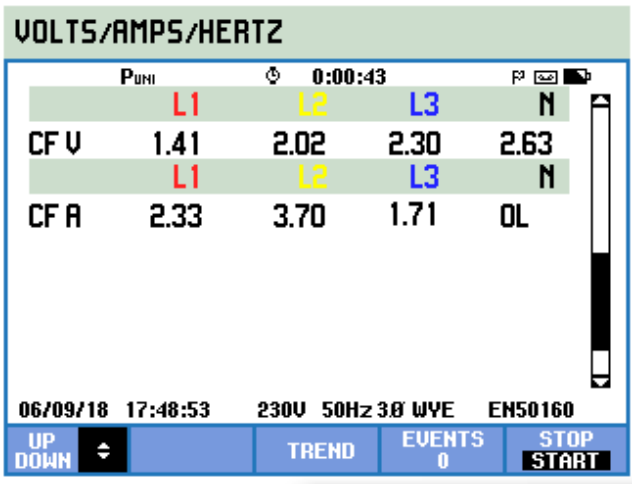


Figure 32. Crest factor at the point of common coupling.

In general, the current sharing accuracy is determined by the percentage of sharing error.

$$\%\text{ of current sharing error} = \frac{\text{Difference of the output current of inverter}}{\text{Total load current}}$$

Table 3 summarizes the current sharing pattern and the corresponding sharing error when implemented with conventional and proposed reinforced droop method. It suggests that percentage of accurate current sharing error is high in conventional droop method comparative to proposed reinforced droop, illustrated in Figure 33.

Table 3. Analysis of the conventional and proposed droop method for current sharing during parallel operation.

Validation Type	Control Strategy	Output Current in the System			Percentage of Current Sharing Error (%)
		I_{La1}—Output Current of Inverter-1 in A (pk-pk)	I_{La2}—Output Current of Inverter-2 in A (pk-pk)	I_{Loada}—Total Load Current at the Common Bus in A (pk-pk)	
Simulation by MATLAB	Conventional droop method	2.0	1.6	3.6	11
	Proposed reinforced droop method	1.8	1.76	3.6	1.2
Real time Validation	Conventional droop method	1.95	1.6	3.55	11.2
	Proposed reinforced droop	1.8	1.75	3.55	1.4

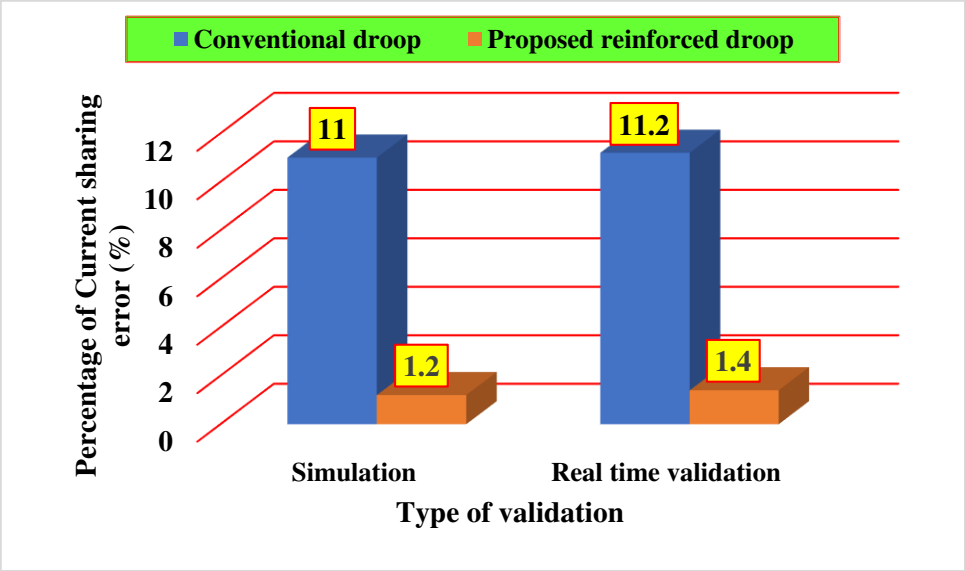


Figure 33. Comparison of conventional and proposed reinforced droop control.

5. Conclusions

The parallel operated 3-level NPC inverter, is investigated for AC microgrid in islanded application for both transient and static operation under linear and nonlinear load condition. The reinforced droop proposed in the research work accumulates the advantage of capacitor balancing with droop control mechanism due to which the major disadvantage of dc link imbalance is avoided. The proposed strategy overcomes the inherent practical limitation that both inverters should have identical output resistance to share the load accurately. The experimental and simulation results depict accurate current sharing during changing load and operating conditions. The voltage THD at the common bus is 1.8% with linear load and 6.4% with nonlinear load. The comparative analysis summarized in Table 3 infers that the proposed method efficiently improves current sharing by reducing the current sharing error to 1.4%, while the current sharing error of the conventional droop method is 11.2%. The authors explored the merits of 3-level NPC inverter and instigated the implementation of the same to operate in parallel, for AC Microgrid applications. The research gap concerning the utilization of NPC inverter in the area of low voltage microgrids is addressed. This also provides an insight of utilization of NPC inverter for microgrid to the researchers in future direction. The scope of the research work limit to the

analysis current sharing with resistive and rectifier load, where it could further be extended to study of dynamics and stability of system with Induction motor loads.

Author Contributions: Conceptualization, M.P. and K.M.; methodology, M.P.; software, M.P.; validation, M.P., formal analysis, M.P.; investigation, M.P.; writing—original draft preparation, M.P.; writing—review and editing, M.P. and K.M.; supervision, K.M. Both the authors have contributed to the research work, editing and proof reading of the research paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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