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RESEARCH ARTICLE

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Resilient cyber physical infrastructure for single-phase dual inverter with sliding mode control

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Summary

As the need in cyber infrastructure for electrical systems to realize the industry 4.0 revolution, this paper presents a configuration of two-switch dual-output voltage source inverter with integral sliding mode control (ISMC) and cyber twin approach to realize the performance of the system. The inverter has the capability of supplying two independent loads of equal voltage at the load end. The virtual model (cyber twin) is developed to realize the operation of the inverter (physical device) with a host system. The cyber-physical test bench is developed to evaluate the performance of the physical model (inverter prototype) with cyber-physical capabilities. The coupled computation of the virtual model and prototype model is executed to analyze the performance of the inverter.

KEYWORDS

cyber-physical systems, dual-output inverter, rapid control prototype, sliding mode control

1 | INTRODUCTION

The growth of information and communication technology (ICT)[1-3] results in the cyber-physical systems (CPS)[4,5] and internet of things (IoT),[6] which leads to development of smart grids. IoT only has the perception of sense, but CPS has the ability to robust control to the target. The CPS is stated as 3C's (computations, communications, and control). CPS empowers the programmed information gathering, data exchanging, monitoring, and controlling of physical devices, which prompt rising patterns in the field of smart grid[7,8] and virtual labs.[9,10] CPS provides a correspondence between the physical devices and users. The incorporation of CPS with the physical layer provides a solution for remote observing and control with programmed information trade over the web with remote sensor systems.[11,12] CPS frameworks empower the man to machine control through the web.

Nowadays, CPS assumes an essential part in the improvement of smart grids, remote lab and virtual labs in R&D area in the field of electrical designing. The number of researchers has been attempted to actualize CPS in a proficient way. An IoT-based surveillance system with low-complexity data repetition system to make efficient resilience and storage is proposed by Gonizzi et al.[13] Environmental monitoring based on two image sensor by using low power sensors was explained by Koedrith et al.[14] To monitor the environmental conditions by IoT, Zhou et al[15] developed a test bench

LIST OF SYMBOLS AND ABBREVIATIONS: $x(t)$, State vector; V_{DC}, DC Voltage; V_{C1},V_{C2},V_{C3}, Capacitor voltages; V_s, AC side voltage; R, Resistance in inductor; v_o, Output voltage; C, Filter capacitor; $\bar{i}$, DC component; P_s, Output power; V_{oU}, Upper side voltage; I_{oU}, Upper side current; S, Sliding Surface; i_{DC}, DC link Current; V_{ref}, Output reference voltage; f, line frequency; R_{idc}, Internal resistance of inductor; $u(t)$, Control vector; C_1,C_2,C_3, Capacitors; V_t, Terminal voltage; L, Inductor; R_L, Load Resistance; i_o, Output Current; P_{DC}, DC Power; $\tilde{i}$, Periodic Component; P_{loss}, Power loss; V_{oL}, Lower side voltage; I_{oL}, Lower side current; α_1,α_2,α_3, Sliding Coefficient; i_{DCref}, Reference DC current; u_{eq}, equivalent continuous control variable; f_{sw}, Switching frequency

for monitoring large-scale indoor climatic conditions using wireless sensor network. By using wireless sensor network, Aslan et al[16] developed a framework for detecting and monitoring the forest fire. Feng et al[9] proposed a system for the continuous online monitoring system for steel casting. The monitoring system is achieved through a wireless sensor network and team center platform. Mohammed et al[10] developed a cyber-physical system for wind energy monitoring systems, which tends to the internet of energy (IoE). Guobin et al[17] proposed a model for integrating the distributed energy resources and storage devices in the smart grid. [18]

The cyber twin (digital twin)[19] approach has the greatest advantage in implementing CPS. Cyber twin (digital twin) is termed as the realization of the physical system (real system) with a virtual model to enhance the performance of the physical system. In the digital twin (cyber twin) methodology, the virtual model understands the conduct of the physical system to foresee the dynamic changes and react to the framework for better activity. Digital twin (cyber twin) methodology has been proposed by different specialists: vehicle driving assistance for CPS based on fuzzy logic proposed by Kazi et al.[20] Hao Zhang et al[21] proposed cyber twin–based furniture production line. Qinglin et al[22] analyze the big data and cyber twin approach for the possibilities of implementation of Industry 4.0. The comparison of CPS implementation is given in Table 1.

The dual-output inverters make the system more reliable to supply two independent loads. The widely used dual-output inverters for renewable applications are dual-phase single DC bus inverter with a split capacitor, three-wire single-phase inverter, dual-phase dual DC bus inverter, and dual phase with transformer.[24-26] The development of inverter with reduced switches and dual-output inverters with six switches and three switches for single-phase applications are given in previous studies.[27-30] The reduction in the number of semiconductor switches resulted in low semiconductor losses and simple controlling. Generally, the control of inverter is achieved by PI, PID, and direct power control. The sliding mode control (SMC)[22,31-38] provides the dynamic response to the nonlinear systems with the property of hysteresis. The steady-state error of the system is low compared with other controllers. To reduce the steady-state error of the system, integral sliding mode control (ISMC) is utilized. [39-45] The advancements in the field of renewable energy and electrical systems result in smart grids.

As the need in cyber infrastructure for electrical systems to realize the industry 4.0 revolution, this paper presents a configuration of two-switch dual-output voltage source inverter with integral sliding mode control (ISMC) and cyber twin approach to realize the performance of the system. The inverter has capability of supplying two independent loads of equal voltage at load end. The virtual model (cyber twin) is developed to realize the operation of inverter (physical device) with host system. The cyber-physical test bench is developed to evaluate the performance of the physical model (inverter prototype) with cyber-physical capabilities. The coupled computation of virtual model and prototype model is executed to analyze performance of the inverter. In this paper, the design of dual-output inverter for single-phase applications with the reduced number of switches for single-phase applications is designed and integrated with CPS. In two switch half bridge inverter, the split capacitors act as one leg, which results in a

TABLE 1 CPS comparison

Reference	Sensors Type	Mode	Network/Monitoring	Programming Platform
		Zigbee,		
Zhang et al[9]	RFID tag	CAN,	XML	Multidomain
		RFID		
Moness and Moustafa Ahmed[10]	RTU	WSN	CC studio,	Multidomain
			SCADA/HMI	
Gonizzi et al[13]	SenseLab	WSN	Cooja network	Multidomain
	Sensor		simulator	
Zhou et al[15]	Sensor nodes	WSN,	Green orbs	Multi domain
	Green orbs	Zigbee	host computer	
Gonzalez et al[23]	Sensors	WIFI	LabVIEW	Multidomain
	PLC		JIL server	
Proposed	NI sensors	WIFI	LabVIEW	Single domain
	MyRIO		VI Server	

reduction of semiconductor switches. The proposed inverter topology is more reliable in induction motor drive systems, renewable energy systems, and low and medium power applications. The control strategy is based on integral sliding mode control (ISMC) that has the advantages of robustness to the varying parameter and dynamic response to the system. The rapid control prototype (RCP) is implemented for rapid testing of the prototype. The RCP is integrated with CPS for control and performance monitor of the proposed inverter prototype. The highlights of the research work are as follows:

- In two switch half bridge inverter, the split capacitors act as one leg, which results in a reduction of semiconductor switches.
- To control the inverter sliding mode control (SMC), strategies is introduced. The sliding mode control and integral sliding mode control (ISMC) is designed and comparative performance analysis is executed. ISMC has better controlling performance than the SMC with reduced errors.
- The integration of cyber-physical systems (CPS) with power electronics devices is performed to analyze the possibilities of cyber infrastructure to enhance the facilities in electrical system/smart grids.
- The cyber twin–based test bench is developed. The digital model of the inverter with control is modeled in LabVIEW and Multisim packages.
- The single domain programming is utilized to avoid the error in data exchange for each stages.

2 | A CYBER TWIN PERSPECTIVE MODEL

The cyber twin–based RCP test system is developed for performance evaluation of two-switch dual-output inverter. The cyber twin–based cyber physical system includes three sections: physical layer, cyber-physical integration layer, and cyber layer. The target (physical) device with sensors and actuators comprises in physical layer. In Cyber twin model, the software modules with host computer are integrated for the data collection from the physical device through sensors for the generation of control signals.

The development of cyber twin–based cyber infrastructure is introduced for electrical systems. This leads to the improvements in smart grids design and developments. To analyze the real behaviour of the system, a virtual model for the physical device is created and integrated with the system. The block diagram of the cyber infrastructure with cyber twin model is shown in Figure 1. The cyber twin (digital twin) model is developed with LabVIEW-Multisim packages. The data collected from the physical device is processed in cyber integration layer with cyber twin capabilities that is monitored through the web interface present in cyber layer. The system configuration of the inverter with cyber infrastructure is shown in Figure 2.

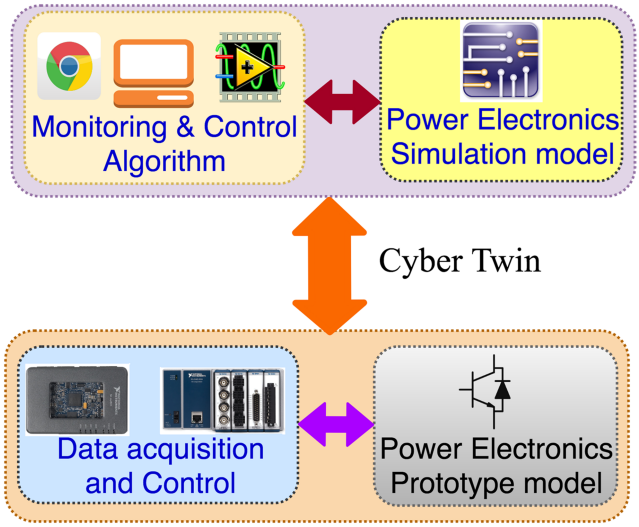

FIGURE 1 Block diagram of cyber twin

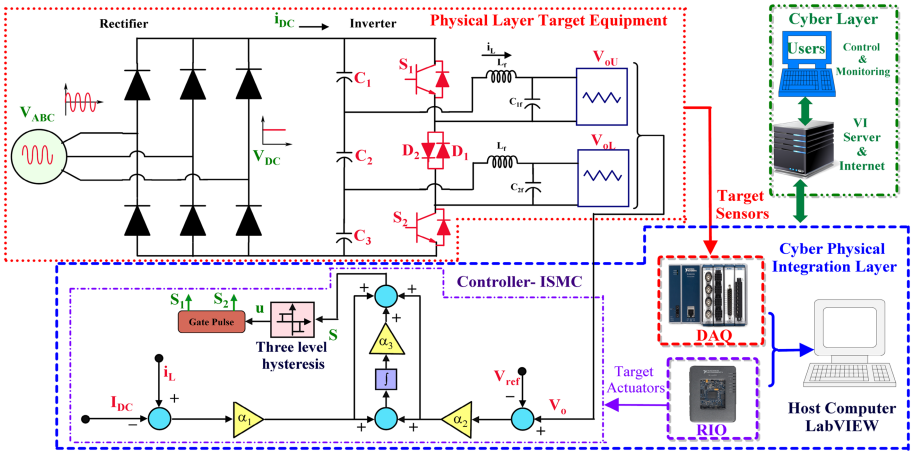

FIGURE 2 System configuration

2.1 | Generalized CPS model

The cyber-physical infrastructure developed for system is shown in Figure 2. The system has the physical components of inverter, sensors, actuators, and controllers representing the physical parameters like current, voltage, frequency, and communications equipments present in physical device. The generalized physical model is represented by multi-input-multi-output (MIMO) based on the assumptions and models along with control, and switching is represented in the generalized models.

$$\dot{x}(t) = Ax(t) + Bu(t), \tag{1}$$

$$Y(t) = Cx(t), \tag{2}$$

where A is the system matrix, B is the input matrix, C is the output matrix, $x(t)$ is the state vector, $u(t)$ is the control vector, and $Y(t)$ is the observation vector. For control of physical device, the integration of the physical layer with the cyber layer is executed. The data collected through sensors (n_s) from physical device are exchanged to controller (n_c) in the host system for computations that are connected to the communication network. The control structure is given by

$$u(t) = Kx(t), \tag{3}$$

where sensor and controller connection are given by $K \in R^{n_c x n_s}$ and $K_{n_c n_s}$ is non-zero term and implies the connection of controller (n_c) and sensor (n_s). The closed-loop control system is represented as

$$\dot{x}(t) = \tilde{A}x(t), \tag{4}$$

$$\text{Closed -loop matrix} \quad (\tilde{A}) = A - BK. \tag{5}$$

The dynamics of the system with delay between sensor and controller is represented by

$$\dot{x}(t) \simeq \tilde{A}x(t) \tag{6}$$

$$\text{Matrix with delay} \quad (\tilde{A}) = (I - BD_{n_c n_s}K)(A + BK) \tag{7}$$

$$\text{Delay matrix} \quad D_{n_c n_s} = \begin{cases} 1 \text{ if } n_s \ \& \ n_c \text{ are connected} \\ 0 \text{ if } n_s \ \& \ n_c \text{ are not connected} \end{cases} \tag{8}$$

The operation of the system is based on switching function of the given by

$$\dot{x} = A_n x + B_n u; \quad t_{n-1} \leq t < t_n. \tag{9}$$

The control reference is computed based on the sensor data, and the communication between the sensor and controller is continuous to provide proper switching function to operate the physical device.

3 | DUAL-OUtPUT SINGLE-PHASE INVERTER

The design of systems with ICT facilitates the development of smart grid systems. This enhances the facility of control and monitoring of the inverter from the remote location with adaptive control. The CPS system design consists of three layers: physical layer, cyber-physical integration layer, and cyber layer. Figure 2 shows the architecture layer proposed for CPS-based RCP evaluation of inverter.

The general dual-output inverters used for renewable energy applications are dual-phase single DC bus inverter with a split capacitor, three-wire single-phase inverter, dual-phase dual DC bus inverter, and dual phase with a transformer. The comparison of existing inverter models and proposed is given in Table 2. The existing models have a higher number of switches that leads to increase in size, control circuitry, and losses. The proposed inverter has two legs with one leg connected with split capacitors (C_1,C_2,and C_3). The split capacitors in this configuration act as one leg for the inverter. Similarly, the second leg consists of two switches ($S_1$and S_2). The anti-parallel diodes ($D_1$and D_2) will act as a common for both upper and lower loads. The inverter will act as a parallel inverter connected to two independent loads. The configuration of the inverter is to supply dual single-phase output for two independent loads with single DC input. Due to the reduced number of switches, the implementation cost, gate driver circuit, will be reduced and reduction in semiconductor losses.

3.1 | Switching states

- In switching state A, the switch S_1 in ON state and S_2 in OFF state. The output is in positive cycle. The voltage of the upper load is V_{C1} and lower load is $V_{C1}+V_{C2}$.
- In switching state B, the switch S_2 in ON state and S_1 in OFF state. The output is in negative cycle. The voltage of the upper load is $-V_{C2}-V_{C3}$ and lower load is $-V_{C3}$.

3.2 | Half bridge average model analysis

The average model of the half bridge inverter is shown in Figure 3. The AC side current (i) is expressed as (10)

$$L\frac{di_{DC}}{dt} + R_{idc} = V_t - V_S \tag{10}$$

$$C\frac{dv_o}{dt} = i_o - \frac{v_o}{R_L}. \tag{11}$$

TABLE 2 Comparison of inverters

Inverter Type	Switches	Capacitor	Transformer
Dual phase with single DC bus with split capacitor	4	2	-
Dual phase with three wires	6	-	-
Dual-phase dual DC bus	4	4	-
Dual phase with transformer	4	2	1
Proposed	2	3	-

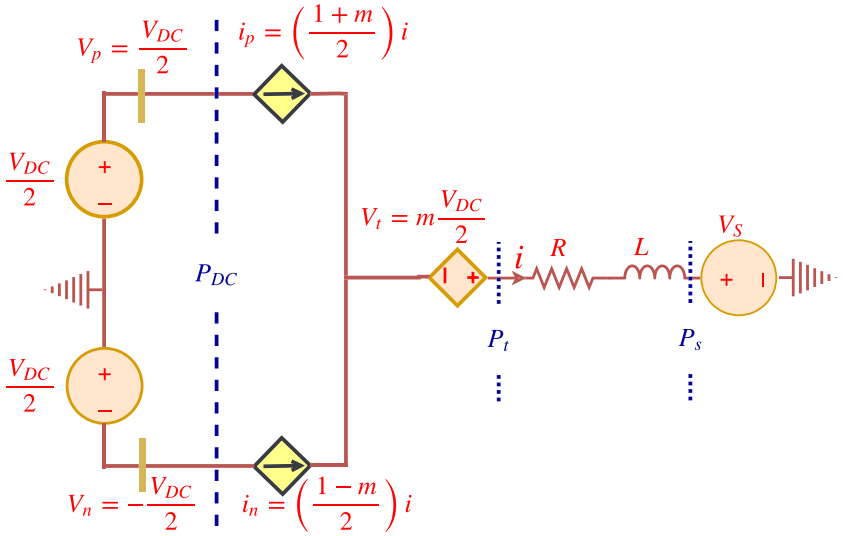

FIGURE 3 Converter average model

The periodic function with conduction period (T_s) with fourier series is expressed by

$$V_t(t) = \frac{1}{T_s}\int_0^{T_s} V_t(\tau)dt + \sum_{h=1}^{h=+\infty}[a_h cos(h\omega_s t) + b_h sin(h\omega_s t)]. \tag{12}$$

Substituting $V_t(t)$ from (12) in (10),

$$L\frac{di(t)}{dt} + Ri(t) = \text{DC comp.} + \text{Periodic comp.} \tag{13}$$

$$\text{DC comp.} = \frac{1}{T_s}\int_0^{T_s} V_t(\tau)dt - V_s \tag{13a}$$

$$\text{Periodic comp.} = \sum_{h=1}^{h=+\infty}[a_h cos(h\omega_s t) + b_h sin(h\omega_s t)]. \tag{13b}$$

Equation (13) describes the output current (i) with low-pass filter with DC component (13a) and periodic component (13b). The response of the filter by superposition principle is considered as the summation of the response of filter to DC component ($\bar{\imath}$) and periodic component ($\tilde{\imath}$) is given by (14),

$$i(t) = \bar{\imath}(t) + \tilde{\imath}(t). \tag{14}$$

The average operator for nonlinear system is expressed in

$$\tilde{x} = \frac{1}{T_s}\int_{t-T_s}^{t} x(\tau)d\tau. \tag{15}$$

By applying the average operator (15) to switches S_1 and S_2, the switching timing obtained is

$$S_1(t) = d, \tag{16}$$

$$S_2(t) = 1 - d. \tag{17}$$

The system operation is expressed in state space matrix as (18)

$$\begin{bmatrix} \dot{v}_o \\ \dot{i}_o \end{bmatrix} = \begin{bmatrix} -R_{idc}/L & -1/L \\ -1/C & -1/R_L C \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix}. \tag{18}$$

The transfer function of the system is given by (19)

$$G(s) = \frac{\dfrac{1}{LC}}{S^2 - S\left(\dfrac{-L + R_L C(-R_{idc})}{R_L CL}\right) + \left(\dfrac{(-R_{idc} R_L C - L)LC + R_L CL}{R_L C^2 L^2}\right)}. \tag{19}$$

3.3 | Converter average model

The average model of the half bridge inverter is obtained and displayed in Figure 3.

For steady-state condition, current (i) and DC voltage (V_{DC}) is assumed to be constant. The terminal voltage (V_t) is given by

$$V_t = \frac{V_{DC}}{2}(2d - 1) = m\frac{V_{DC}}{2}, \tag{20}$$

where m=2d−1 is the relation between modulating signal and duty ratio (d). The DC power (P_{DC}) and terminal power P_t of the converter is expressed as (21):

$$P_{DC} = P_t = \frac{V_{DC}}{2}(2d - 1)i = m\frac{V_{DC}}{2}i. \tag{21}$$

The output power (P_s) of the converter with respect to output voltage (V_s) is given by (22):

$$P_s = V_s i. \tag{22}$$

The power loss (P_{loss}) of the converter model is given by

$$P_{loss} = P_{DC} - P_t. \tag{23}$$

3.4 | Capacitor voltage and current balancing

The capacitors (C_1,C_2,and C_3) connected is parallel to the source, and the voltage balancing of the capacitors are expressed as

$$\left.\begin{aligned} V_{C1} &= \frac{V_{DC}}{2}(1 - T_{ON}) \\ V_{C2} &= \frac{V_{DC}}{2}(T_{ON} - T_{OFF}) \\ V_{C3} &= \frac{V_{DC}}{2}(1 - T_{OFF}) \end{aligned}\right\} \tag{24}$$

where, V_{C1},V_{C2}, and V_{C3} are voltage across the capacitors. V_{S1}, V_{S2}, and V_{S3} are the voltages in the switches S_1 and S_2. V_{D1} is the voltage across the diode D_2. The DC ripple (ΔV_C) is given by

$$\Delta V_{DC} = \frac{I_{max}}{2C\omega}. \tag{25}$$

The ripple voltage for the capacitors are expressed

$$\left.\begin{aligned}\Delta V_{C1} &= \frac{I_{oU}}{2C_1\omega_U} + \frac{I_{oL}}{2C_1\omega_L}(1 - T_{ON}) \\ \Delta V_{C2} &= \frac{I_{oU}}{2C_2\omega_U} + \frac{I_{oL}}{2C_2\omega_L}(T_{ON} - T_{OFF}) \\ \Delta V_{C3} &= \frac{I_{oU}}{2C_3\omega_U} + \frac{I_{oL}}{2C_3\omega_L}(1 - T_{OFF})\end{aligned}\right\}. \tag{26}$$

The capacitor voltage balanced, and the voltage that appears on the lower and upper load is expressed as

$$\left.\begin{aligned}v_{oU} &= \frac{V_{DC}}{2}sin\omega t \\ v_{oL} &= \frac{V_{DC}}{2}sin\omega t\end{aligned}\right\}. \tag{27}$$

The currents flowing through the capacitors are

$$\left.\begin{aligned}I_{C1} &= I_{DC} + I_{leg} = (1 - T_{ON})I_{oU} + (1 - T_{ON})I_{oL} \\ I_{C2} &= I_{C1} + I_{oU} = (1 - T_{ON})I_{oU} + (1 + T_{ON})I_{oL} \\ I_{C3} &= I_{C2} - I_{oL} = -(1 + T_{ON})I_{oU} - (1 + T_{ON})I_{oL}\end{aligned}\right\}, \tag{28}$$

where I_{C1},I_{C2} and I_{C3} are currents through the capacitors. I_{leg} is the current flowing through the inverter leg.

3.5 | Sizing of capacitors

The split capacitors are common for both DC link and one leg for inverter. In the inverter first leg, there are three capacitors (C_1,C_2,and C_3), which are connected in the ratio of 1:0.5:1. The apparent power (S) of the inverter is given by

$$S = V_{rms} * I_{rms}(VA). \tag{29}$$

Capacitor equations for (C_1,C_2,and C_3) are expressed as

$$C_1 = C_3 = \frac{S}{2\omega * V_{DC} * \Delta V_{DC}}, \tag{30}$$

$$C_2 = \frac{1}{2}\left(\frac{S}{2\omega * V_{DC} * \Delta V_{DC}}\right). \tag{31}$$

4 | INVERTER CONTROL BASED ON INTEGRAL SLIDING MODE CONTROL (ISMC)

The sliding mode control (SMC) is the viable controller with switching nature of inverter inferred from the system model. The benefits of SMC is that it has a superior unique reaction, steadiness against the variations of the load, and easy implementation. The control is based on two loops inner current control and outer voltage control loops. The state variables considered from the system are input inductor current (x_1), and output capacitor voltage (x_2) is considered as the state variables for controlling. The error variables are represented as

$$\text{Error variables} = \begin{cases} x_1 = i_{DC} - i_{DCref} \\ x_2 = v_o - V_{ref} \end{cases} \tag{32}$$

where i_{DC} is the DC link current, i_{DCref} is the DC link reference, v_o is the output voltage, and V_{ref} is the output reference voltage. The existence of steady-state error in the SMC is identified, and in order to minimize the steady-state error, an

additional integral controlled state variable (x_3) is incorporated in sliding surface and termed as integral sliding mode control (ISMC). The additional error variable is defined by (33):

$$\text{Error variable} = x_3 = \int (x_1 + x_2)dt. \tag{33}$$

The sliding surface (S) is represented as (34):

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3, \tag{34}$$

where α_1, α_2, and α_3 are the sliding coefficients. The extra factor x_3 gathers straightforwardly to steady-state errors of x_1 and x_2. The time derivative of (34) is

$$\dot{S} = \alpha_1 \dot{x}_1 + \alpha_2 \dot{x}_2 + \alpha_3 \dot{x}_3 \tag{35}$$

$$\dot{x}_3 = x_1 + x_2. \tag{36}$$

The state variables are computed by Equations (10) and (11). The $\dot{x}_1$, $\dot{x}_2$, and $\dot{x}_3$ are the derivatives of error variables and given by (37), (38), and (39):

$$\dot{x}_1 = \frac{1}{L}(V_t - Ri_{DC} - uv_o) - \frac{di_{DCref}}{dt}, \tag{37}$$

$$\dot{x}_2 = \frac{1}{C}\left(ui_{DC} - \frac{v_o}{R_L}\right) - \frac{dV_{ref}}{dt}, \tag{38}$$

$$\dot{x}_3 = \left(i_{DC} - i_{DCref}\right) + \left(v_o - V_{ref}\right). \tag{39}$$

where V_s is the source voltage, C is the output filter capacitor, R is the load, and u is the switching function. The derivatives of sliding function ($\dot{S}$) obtained by incorporating (37), (38), and (39) is expressed as (40):

$$\dot{S} = \left(\frac{-u\alpha_1}{L} - \frac{\alpha_2}{R_L C} + \alpha_3\right)v_o + \left(-\alpha_1 R_L + \frac{\alpha_2 u}{C} + \alpha_3\right)i_{DC} + B, \tag{40}$$

where B is expressed as (41),

$$B = \left(\alpha_1 \frac{V_t}{L} - \frac{di_{DCref}\alpha_1}{dt} - \alpha_2 \frac{dV_{ref}}{dt} - \alpha_3 I_{DC} - \alpha_3 V_{ref}\right). \tag{41}$$

To satisfy the stability condition $S\dot{S} < 0$, u=1 and u=−1 are incorporated to the equation (41).
If $S < 0 = \dot{S} > 0 \Rightarrow u = 1$,

$$\dot{S} = \left[\left(\frac{-\alpha_1}{L} - \frac{\alpha_2}{R_L C} + \alpha_3\right)v_o + \left(\frac{-\alpha_1 R_L}{L} + \frac{\alpha_2}{C} + \alpha_3\right)i_{DC} + B\right] > 0. \tag{42}$$

If $S > 0 = \dot{S} < 0 \Rightarrow u = -1$,

$$\dot{S} = \left[\left(\frac{\alpha_1}{L} - \frac{\alpha_2}{R_L C} + \alpha_3\right)v_o + \left(\frac{-\alpha_1 R_L}{L} - \frac{\alpha_2}{C} + \alpha_3\right)i_{DC} + B\right] < 0. \tag{43}$$

The simplified condition for stability from Equations (42) and (43) is given by (44):

$$0 < \left(-\alpha_1 C + \alpha_2 \frac{L}{R_L} - \alpha_3 LC\right)v_o + (-\alpha_3 LC + \alpha_2 L + \alpha_1 R_L C)i_{DC} - LCB < 2(\alpha_2 L i_{DC} - \alpha_1 C v_o). \tag{44}$$

The equivalent continuous control (u_{eq}) is represented as (45):

$$u_{eq} = \frac{LC}{v_o C\alpha_1 - \alpha_2 L}\left(-\frac{\alpha_2 v_o}{R_L C} + v_o\alpha_3 - \frac{i_{DC}\alpha_1 R_L}{L} + i_{DC}\alpha_3 + B\right). \tag{45}$$

The condition for stability is tested with numerical computations of sliding coefficients (α_1,α_1, and α_3) along with i_{DC} and v_o. From (44), the equation (46) is obtained based on the numerical computations with minimum and maximum values.

$$2(\alpha_2 L i_{DC} - \alpha_1 C v_o) > 0. \tag{46}$$

To maintain the stability, the sliding coefficients (α_1,α_2, and α_3) must be in positive. i_{DC}=I_{DC} at steady-state condition, the condition for v_o is given by

$$\frac{\alpha_2}{\alpha_1} > \frac{C v_o}{i_{DC}}. \tag{47}$$

The sliding coefficient (α_3) will be resolved regardless of ($\alpha_1$and α_2) by adjusting to acquire the coveted reaction. The block diagram for ISMC is shown in Figure 2. The hysteresis band (h) is fixed between 5% and 10% of the reference voltage. Based on the frequency (f), the hysteresis band is calculated and expressed as (48):

$$\text{Hysteresis band} \quad = \frac{1}{8fL}\left(V_{DC} - \frac{4v_o^2}{V_{DC}}\right). \tag{48}$$

In three-level hysteresis, for $+_{ve}$, cycle voltage is $+V_{DC}$ when error achieves the lower hysteresis band (h_{lower},$-h$) and "0" when the error bring down than "$-h$." For $-_{ve}$ cycle, the voltage is $-V_{DC}$ when upper hysteresis band (h_{upper},$+h$) and "0" when higher than "$+h$." The hysteresis band (h) brings about a dead band (t_d) for semiconductor switches. In three-level hysteresis, the "0" level presence will bring about the dead time for semiconductor switches and has less distortion. The switching frequency (f_{sw}) for three-level hysteresis is ascertained in on the basis of (49):

$$f_{sw} = \frac{\omega_o^2 V_{DC}}{h + t_d\omega_o^2 V_{DC}}\left(\frac{2}{\pi}m - \frac{1}{2}m^2\right) \tag{49}$$

where ω_o=$2\pi f$, f is the frequency, and m is the disturbance amplitude. The momentary switching frequency (f_{in}) depends on the progression between h_{upper} and h_{lower}. The dead band of 3 microseconds with switching frequency of 2.9 kHz and the line frequency is 50 Hz is considered for the generation of control signals

The switching function is defined by the hysteresis (h) block in the controller design. The hysteresis switching function has three levels (−1,0,+1). The switching function for the inverter is given by (50):

$$u_1 = \begin{cases} +1 \; if \; S < -h \\ 0 \quad if \quad S > 0 \end{cases} \quad u_2 = \begin{cases} -1 \; if \; S < \; +h \\ 0 \quad if \quad S > 0 \end{cases}. \tag{50}$$

The sliding surface (S) is the contribution to the Schmitt triggers (hysteresis switching). The Schmitt triggers are intended to work according to the switching conditions (50) for creating control signals. The ISMC reacts superior to SMC and limited the steady-state errors. The correlation of SMC and ISMC is examined by considering the system parameters, L=10 mH, C=20μF, R=50Ω, α_1=0.0002, α_2=0.2, and α_1=50. The performance of SMC is observed from Figure 4A; the inductor current has the steady-state error of 5%, and steady-state error of the voltage is 10% inferred from Figure 4B.

The host PC with LabVIEW, C-DAQ, and MyRIO includes a cyber-physical reconciliation layer as appeared in Figure 2. The LabVIEW is a graphical programming instrument with consistent combination of equipment for information procurement and controlling of physical devices. The source voltage (V_{DC}), source current (i_{DC}), output voltage (V_o), and output current (i_o) are detected from the physical equipment by utilizing the NI C-DAQ 9174 with voltage (NI-9225) and current (NI-9227) sensor. The reconfigurable input/output controller (NI-1900 MyRIO)with onboard WIFI is utilized to implement the control algorithm for the generation of control pulse and to trigger the semiconductor device using gate driver TI SM72295. The experimental setup is shown in Figure 6.

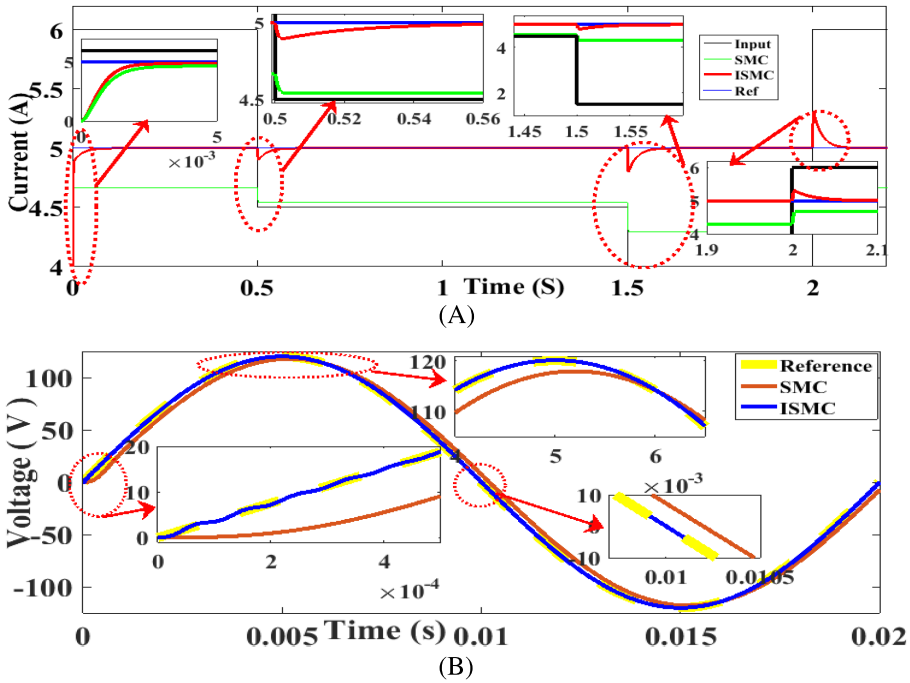

FIGURE 4 Performance comparison of SMC and ISMC: A, input current; B, output voltage

5 | CYBER LAYER

The data from the physical device and cyber-physical integration layer are monitored and controlled through the network by cyber layer. The host computer has the data of sensors, control parameters, data storage, and supervisory control of the physical device. The cyber layer is linked to the Internet to the host computer. Widely used protocol for connection is local area network (LAN), and wireless local area network (WLAN) is utilized for CPS implementation. The cyber layer architecture is designed such a way to monitor real-time data and controlling of the physical device. The system enables the CPS for providing the features like

1. internet-based cross-field communications.
2. interaction of cross-domain and intelligent knowledge sharing, and
3. task and mode based sensing and controlling of physical device.

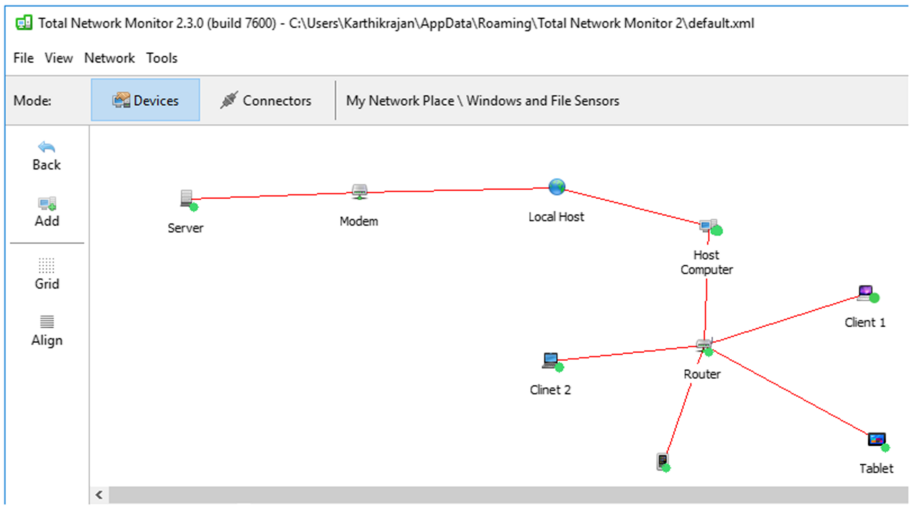

FIGURE 5 Network monitoring

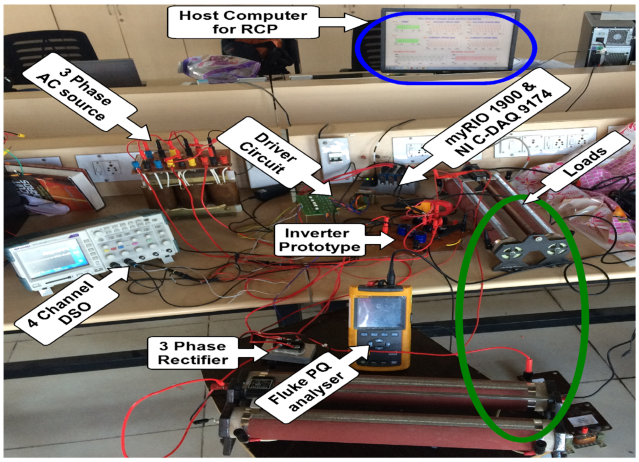

FIGURE 6 Experimental setup

The implementation of LabVIEW-based CPS is done by using VI server method with the web service management tool. This method has good live data support and good interaction between the client and user. The cybersecurity is good compared with all other methods. The security layer SSL x.509 with TCP protocol to ensure the security of the system. The URL mapping is represented as https://localhost:portaddress/webservice.html. The network connected to the system is monitored through the total network monitoring software to track the active devices. The network map is shown on Figure 5.

6 | RESULTS AND DISCUSSIONS

The performance of dual-output single-phase inverter with ISMC and cyber infrastructure is evaluated. The experimental setup is shown in Figure 6. The specifications of cyber infrastructure with inverter are given in Table 3. The three-phase supply is fed to the rectifier, and the rectified dc voltage V_{DC} is fed to inverter. Figure 7 shows the source voltage, DC voltage, and current. The source voltage of 50 V is fed, and Figure 7A shows the source voltage and current. Figure 7 B shows the source voltage with V_{DC} and I_{DC}. Figure 7C,D shows the THD for source voltage and current. The dual-output inverter is tested under PWM condition with frequency of 50Hz.

6.1 | Steady-state performance

The dual-output single-phase inverter is analyzed with cyber-physical infrastructure with ISMC-based control strategy. The controller performance is discussed in Section 4. Figure 4A,B shows the performance of SMC and ISMC. The 3∅ AC source at front-end RMS voltage v_{rms}= 50V is feed to uncontrolled rectifier. Figure 8 depicts the output of dual-output inverter with ISMC.

TABLE 3 System parameters

Parameters	Values (Units)
Maximum rated power	960 W
DC link voltage (V_{DC})	115 V
C_1 and C_3	440 μF
C_2	220 μF
IGBT	IRG4BC30S
Diodes	MUR860
Controller	NI myRIO 1900
Data acquisition systems	NI C-DAQ 9174
Driver circuit	TI SM72295
Four channel DSO	Textronix TPS 2024B
Network monitoring	Total network monitor

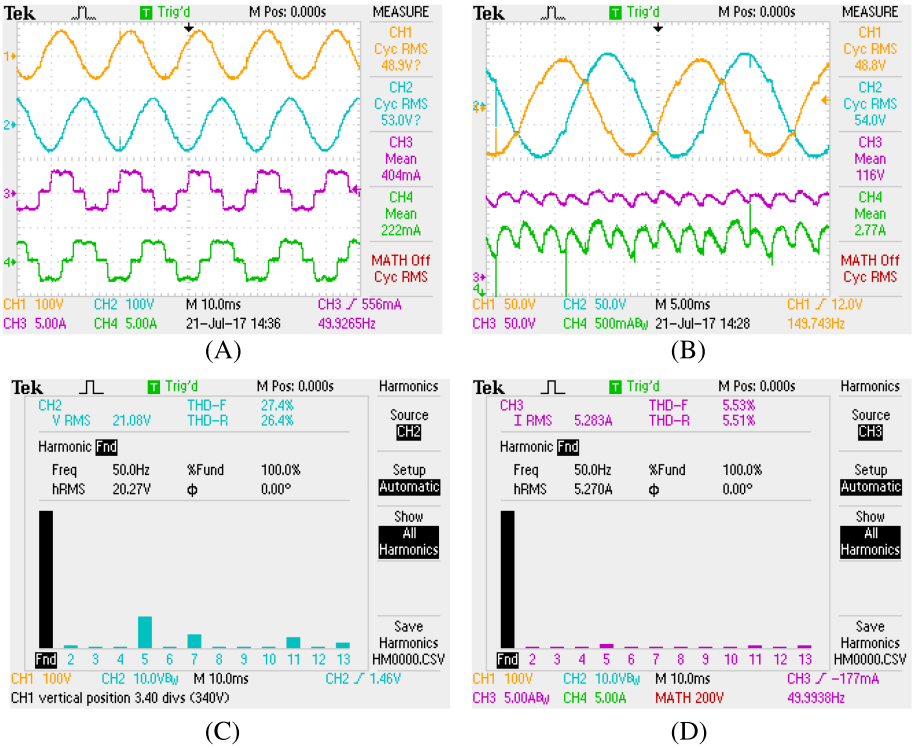

FIGURE 7 Hardware prototype results for source voltage and current: A, source voltage and current, B, source voltage, DC voltage, and current, C, THD for source voltage, and D, THD for source current

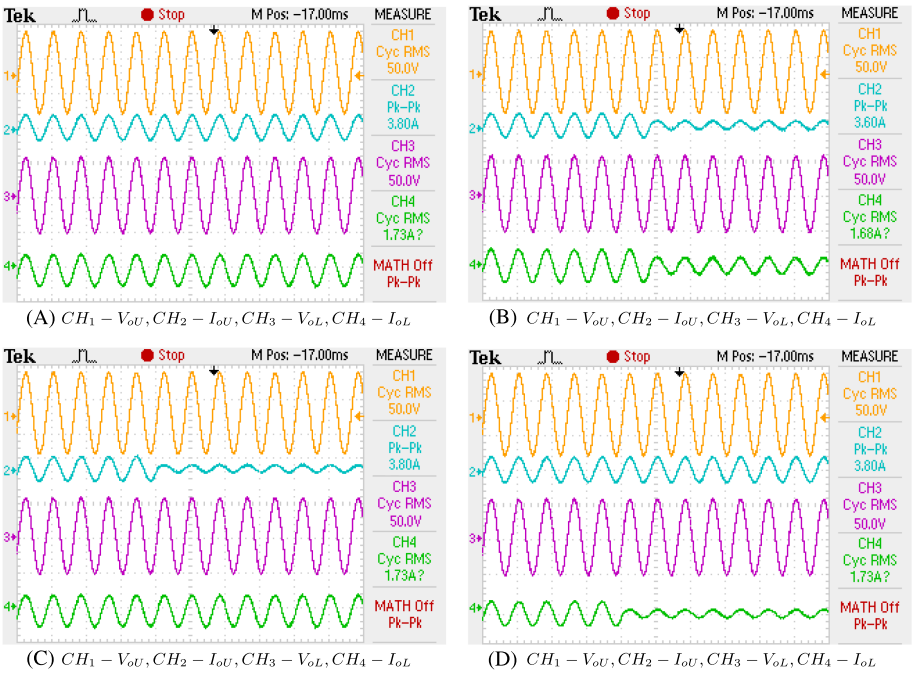

FIGURE 8 Prototype results: A, Output voltage and current of dual-output inverter, B, THD of output voltage, C, THD of output current, D, output voltage and load current with step change in both upper and lower load, E, output voltage and load current with step change in upper load, and F, output voltage and load current with step change in lower load

Figure 8A depicts the performance of dual-output inverter in steady-state analysis. The upper output voltage (V_{oU}) and lower output voltage (V_{oL}) are 50 V. The upper load current (I_{oU}) inferred from Figure 8A is 3.80 A, and lower load current (I_{oL}) inferred from Figure 8A is 1.73 A. The THD observed from Figure 9A is 5% for upper output voltage (V_{oU}),

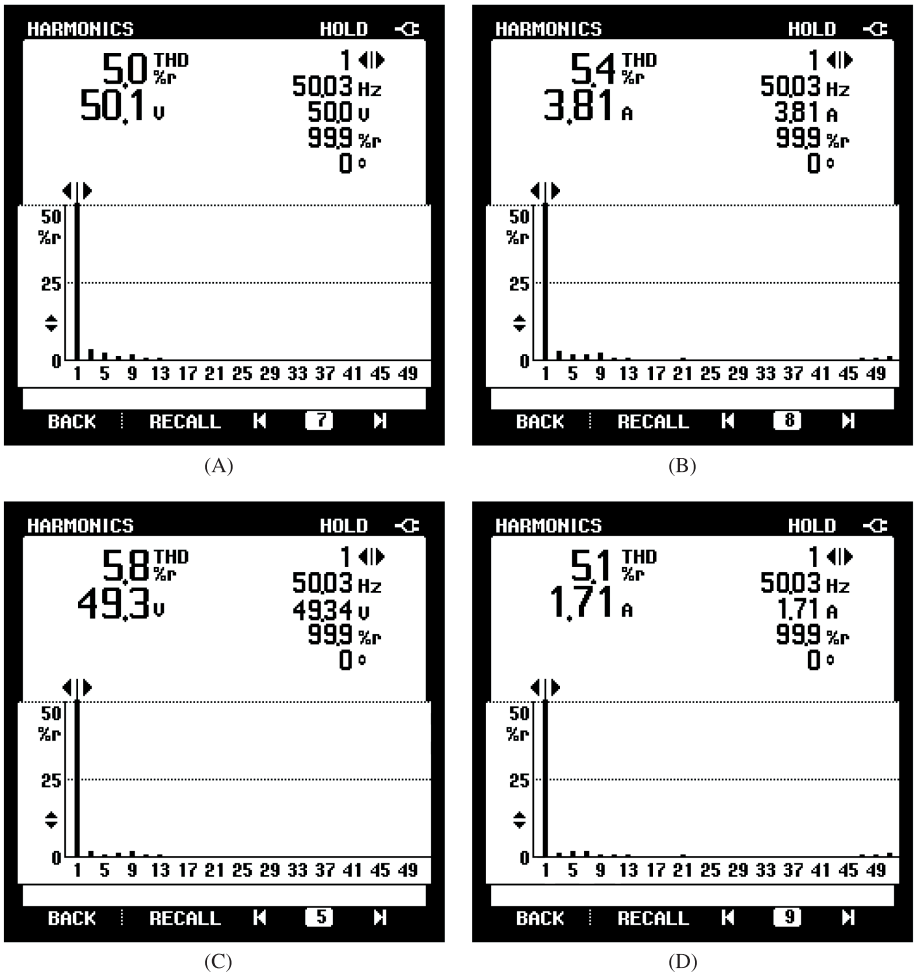

FIGURE 9 Hardware prototype results with fluke analyzer: A, THD of upper voltage (V_{oU}), B, THD of upper current (I_{oU}), C, THD of lower voltage (V_{oL}), and D, THD of lower current (I_{oL})

and THD for upper output current (I_{oU}) is 5.4% as inferred from Figure 9B. Figure 9C depicts that the THD for lower output voltage (V_{oL}) is 5.8%, and the corresponding current (I_{oU}) is 5.1%, which is observed from Figure 9D. The THD for both voltage and current is in under acceptable limits as per IEEE:519-2014 standards.

6.2 | Response to load variations

At initial condition, the load is kept at constant, and to evaluate the controller performance, the load is varied. It is observed from Figure 8B that the output voltage is not affected when there is a step change in the load. It is inferred from Figure 8B that the load current (I_{oU}) and (I_{oL}) has step change. Figure 8C depicts the step change in upper load current (I_{oU}), and lower load remains same. It is inferred from Figure 8D that the performance of inverter with step change in lower load is analyzed. Figure 8C,D depicts the performance of inverter with step change in lower load, and the output voltage is not affected in both V_{oU} and V_{oL}.

6.3 | Cyber-physical systems results and discussions

The LabVIEW-CPS–based rapid control prototype evaluation of two switch dual-output inverter is modeled and tested, and the cyber infrastructure results are shown in Figure 10. The implementation of the experimental setup consists of two sections of LabVIEW-based CPS test bench and inverter prototype. The experimental setup is shown in Figure 6. The pictorial representation of CPS integration is shown in Figure 2. The control of the physical device can be achieved by CPS using LabVIEW server with request- and response-based model.

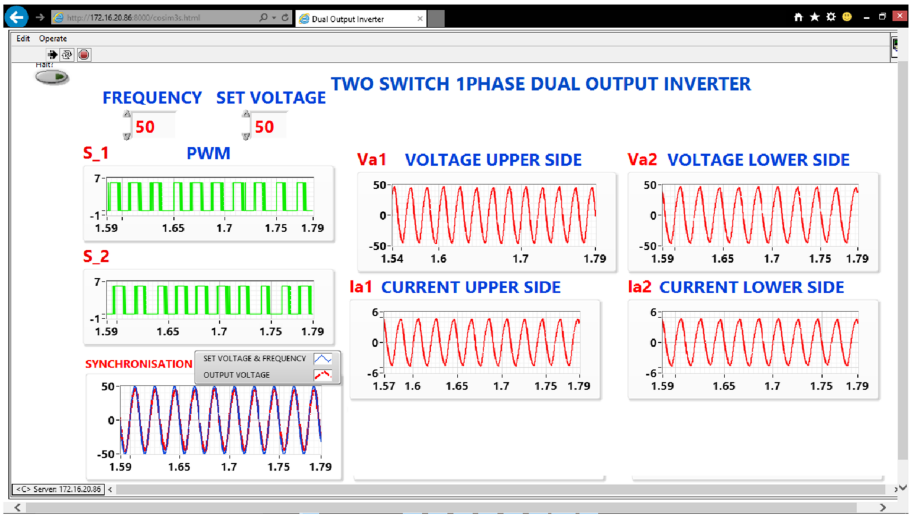

FIGURE 10 Cyber infrastructure observations

The CPS should behave as (a) intelligent (to anticipate and comprehend the behavior of the system, LabVIEW-based environment is used), (b) real time (to gather the continuous information from physical device, C-DAQ with LabVIEW is utilized), and (c) adaptive and predictive control (to respond and anticipate the changes in the physical systems, the ISMC-based control strategy is implemented in MyRIO-1900).

The combination of physical layer and the cyber-physical layer is integrated into the cyber layer. The cyber layer has host computer with monitoring station and server. The collected data from the cyber-physical layer is monitored and controlled through LabVIEW. The VI server-based web service management system is implemented to perform the testing of the proposed model. The control pulse is generated using NI MyRIO. The control strategy is based on ISMC. The monitoring screen (Figure 10) of the system has the frequency, set voltage, the voltage of upper and lower side, current of lower and upper side, source voltage, rectified voltage, PWM for two switches, set voltage, and output voltage synchronization waveforms. The inverter is tested under 50 V, 50 Hz, as set voltage and frequency, respectively. The performance is monitored in the Internet Explorer, and results shown in Figure 10. The network monitoring of the cyber infrastructure is analyzed using Total Network Monitor package.

6.4 | Voltage stress

The inverter model has two switches: S_1 and S_2. The voltage stress of the switches is calculated by the peak voltage across the collector and emitter V_{CE1} and V_{CE2} terminals. The voltage stress is given by

$$V_{CE1} = V_{CE2} = \frac{V_{DC}}{2}. \tag{51}$$

6.5 | Loss analysis

The total power loss (P_{loss}) of the configuration includes rectifier loss, IGBT loss, and inverter diode loss.

$$P_{loss} = P_{Rec} + P_C + P_{SW} + P_{Diode}. \tag{52}$$

6.5.1 | Bridge rectifier

The three-phase bridge rectifier has six diodes, and the loss is expressed as

$$P_{Rec} = 6(V_D I_{Rec}). \tag{53}$$

6.5.2 | Diode in inverter

The loss in diode D_1 and D_2 in the inverter is given by

$$P_{Diode} = 2(V_D I_o). \tag{54}$$

6.5.3 | IGBT conduction loss

The conduction loss occurs when the IGBT or free wheeling diode is in ON state. The conduction loss on high side P_{ON-H} of the inverter is given by

$$P_{ON-H} = I_o^2 * R_{ON-H} * \frac{V_o}{V_{DC}}. \tag{55}$$

The conduction loss on low side P_{ON-H} is given by

$$P_{ON-L} = I_o^2 * R_{ON-L} * \left(1 - \frac{V_o}{V_{DC}}\right), \tag{56}$$

where the R_{ON-H} and R_{ON-L} are the resistances of IGBT for high and low side, respectively.

6.5.4 | IGBT switching loss

The power loss occurred during the transition and based on switching frequency. The switching loss P_{SW} is calculated by

$$P_{SW} = \frac{1}{2} * V_{DC} * I_o * (t_r + t_f) * f_{sw}, \tag{57}$$

where t_r and t_f are the high time and fall time of IGBT, respectively. f_{sw} is the switching frequency.

The loss analysis of the switches S_1, S_2, and S_2 based on the internal parameters are calculated. The conduction loss and switching loss are analyzed for a different range of input voltages and power. The loss for various operating conditions such as PWM, modified sine wave, and SWPM is calculated. The comparison is graphed, is plotted for one switch, and is shown in Figure 11. While comparing the utilization of semiconductor devices compared with existing models as given in Table 4, the proposed model has low losses.

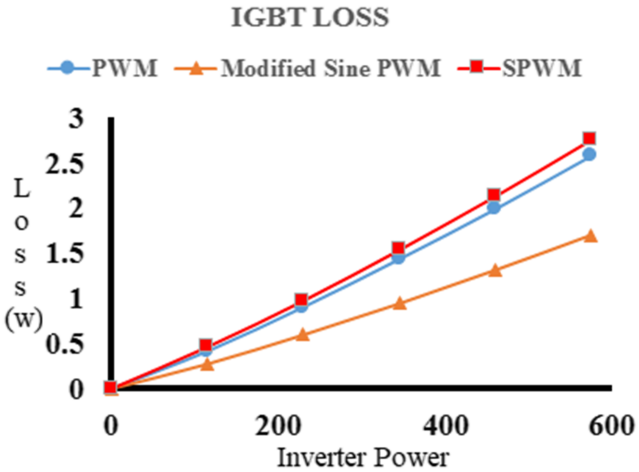

FIGURE 11 IGBT loss comparison for single switch

TABLE 4 IGBT loss comparison

Inverter Type	Switches	Capacitor	Total Loss, W
Dual phase with single DC	4	2	11.032
bus with split capacitor			
Dual phase with three wires	6	-	16.548
Dual-phase dual DC bus	4	4	11.032
Dual phase with transformer	4	2	11.032
Proposed	2	3	5.516

7 | CONCLUSION

The dual-output back-end converter is designed with two semiconductor switches with significant advantage of supplying two independent loads. The sliding mode control is designed, and it results in 10% steady-state error for voltage and 5% for current, and to alleviate the error, integral sliding mode (ISMC) is introduced. The integration of cyber infrastructure with cyber twin approach is implemented. The proposed system is evaluated with the cyber infrastructure, and performance is analyzed. The inverter is analyzed under steady-state and variable-operating conditions. The ISMC-based control strategy results in robust performance even under the load variations. The output voltage is not distorted under step change in the loads.

The cyber twin approach realizes the physical system with the virtual model to enhance the performance of the control and monitoring of the system. Cyber twin approach has the wide range of applications in electrical systems. In smart grids, Industry 4.0 evaluations implementing of cyber infrastructure with cyber twin makes the system reliable and man to machine interactions.

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