Stability performance of optimized symmetric DG-MOSFET

Stability performance of optimized symmetric DG-MOSFET

K Sivasankaran and P S Mallick†

School of Electrical Engineering, VIT University, Vellore, Tamilnadu, India

Abstract: This article presents the bias and geometry optimization procedure for the radio frequency (RF) stability performance of nanoscale symmetric double-gate metal-oxide semiconductor field-effect transistors (DG-MOSFETs). The stability model can provide hints for optimizing the DG-MOSFET under an RF range. The device parameters are extracted for different bias and geometry conditions through numerical simulation, and the RF figures of merit such as cut-off frequency (f_t) and maximum oscillation frequency (f_{max}), along with stability factor, are calculated for an optimized structure. The proposed structure exhibits good RF stability performance.

Key words: DG-MOSFET; radio frequency; stability factor; numerical simulation

DOI: 10.1088/1674-4926/34/10/104001 **EEACC:** 2570

1. Introduction

The scaling of conventional planar MOSFETs down to the sub-50 nm regime leads to an increase in leakage currents and short channel effects (SCEs), which causes severe problems in the switching operations. In order to obtain an improved performance, double-gate MOSFETs were proposed for better SCE suppression capability, higher current drive capability, lower leakage current and better scaling capability[1, 2]. In recent years, DG-MOSFETs have become popular for analog and RF applications due to the volume inversion effect at low gate bias. The impact of structural parameter fluctuation on the RF performance of DG-MOSFETs was studied and the optimized structure reported[3]. The impact of gate and channel engineering on the RF performance of DG-MOSFETs was also studied[4] and shows that a dual material (DM) work function for the gate has better RF performance as compared to halo-doped channel DG-MOSFETs. Recently, graded channel (GC) technology, gate stack engineering (GS), the DM work function gate and combinations of these technologies, i.e., GCGSDG and GSDMDG, were studied for analog and RF performance[5]. The optimized DG-MOSFET design using DM and GC requires additional effort in processing steps such as the metal wet etch process, metal inter diffusion process, and selective implantation to maintain the dual work function in DM devices. Selective tilted ion implantation is required for GC devices. However, studies on the stability performance of DG-MOSFETs have not received attention, and this is one of the most important parameters for radio frequency integrated circuit (RFIC) design.

In our previous work, we studied the RF stability of silicon nanowire transistors[6] and this article presents the stability performance of optimized DG-MOSFETs in the RF range. We have discussed the bias and geometry optimization procedure of DG-MOSFET in detail.

2. Device structure and simulation

Figure 1(a) shows the cross sectional view and Figure 1(b) shows the 3D schematic structure of a symmetric DG-MOSFET with a physical channel length (L_{ch}) of 22 nm and gate oxide thickness (t_{ox}) of 1.6 nm, as per ITRS[7]. The DG-MOSFET has an n^+ source and drain with a doping concentration of 2×10^{20} cm^{-3} and channel doping of 10^{15} cm^{-3}. Si_3N_4 is used as the gate spacer material to provide mechanical strength to the gate. HfO_2 is used as the gate dielectric, which reduces gate tunneling leakage current, and the gate electrode work function is considered as 4.15 eV. Electric field dependent carrier mobility with velocity saturation, band gap narrowing, a Lombardi constant voltage and temperature (CVT), along with a concentration-dependent mobility model, were activated for simulation. Fermi-Dirac statistics, Shockley Read Hall and auger recombination for minority carrier recombination have been used, along with a density gradient quantum correction model, for inversion layer quantum effects for simulation[8]. The AC characteristics were performed to extract two port Y and Z parameters. The extracted parasitic resistances and capacitances from device simulation are used to calculate the RF FoM of the DG-MOSFET. The device simulations were performed using a Silvaco ATLAS device simulator.

3. Stability factor and modeling

The stability factor, K, gives an indication as to whether a device is conditionally or unconditionally stable. The DG-MOSFET is unconditionally stable at any operating frequency above a critical frequency (f_k). Unconditionally stable means that the transistor will not begin to oscillate independently from the value of the signal source and load impedances from any additional passive termination networks at the transistor's input and output[9]. At an operating frequency below f_k, however, the transistor is conditionally stable and certain termination conditions can cause oscillation. Hence, the device must satisfy the condition $K > 1$ to be unconditionally stable[10]. The stability factor is calculated using Y-parameters at different frequencies of operation for the DG-MOSFET. The stability factor in terms of Y-parameter can be expressed as[11]

† Corresponding author. Email: psmallick@vit.ac.in

Received 14 March 2013, revised manuscript received 22 April 2013

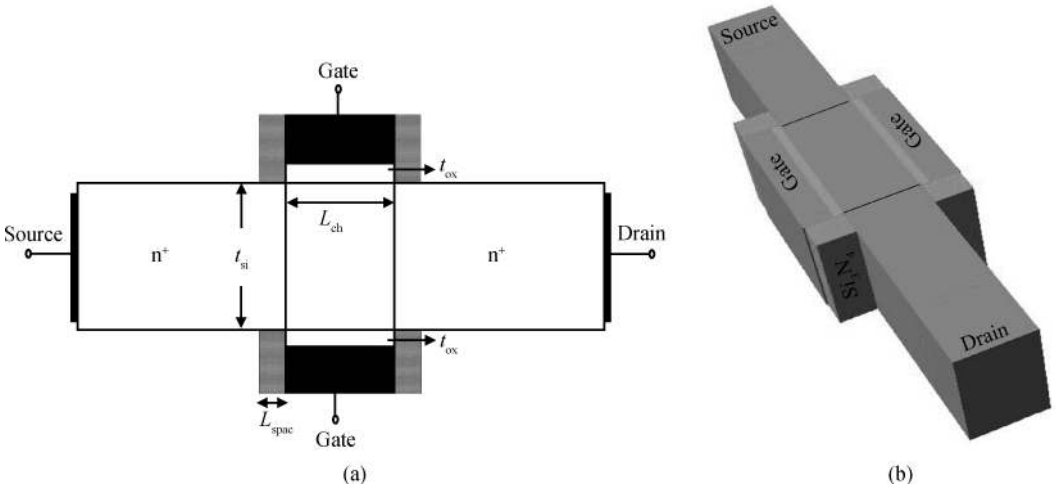

Fig. 1. (a) Cross-section view and (b) 3-D schematic view of a symmetric DG-MOSFET.

$$K = \frac{2\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}. \quad (1)$$

This article focuses on a symmetric DG-MOSFET which has three terminals. Both the gates are tied to form a single gate terminal, and there are source and drain terminals. The Y-parameters are considered with intrinsic small signal parameters of symmetric DG-MOSFETs as[12]

$$Y_{11} \approx \omega^2 R_{gd} C_{gd}^2 + \mathrm{j}\omega \left(C_{gs} + C_{gd}\right), \quad (2)$$

$$Y_{12} \approx -\omega^2 R_{gd} C_{gd}^2 + \mathrm{j}\omega C_{gd}, \quad (3)$$

$$Y_{21} \approx -\omega^2 R_{gd} C_{gd}^2 - \mathrm{j}\omega \left(C_{gd} + \tau g_m\right), \quad (4)$$

$$Y_{22} \approx g_{ds} + \omega^2 R_{gd} C_{gd}^2 + \mathrm{j}\omega C_{gd}. \quad (5)$$

These Y parameters can be used in Eq. (1) to simplify further as

$$K \cong \frac{\omega \left(R_{gs} g_{ds} C_{gg}^2 + 2R_{gd} g_m C_{gg} C_{gd} + C_{gg}^2\right)}{C_{gd}\sqrt{2\omega^2 g_m C_{gg}^2 + g_m^2}}, \quad (6)$$

where C_{gs} is the total gate-to-source, C_{gd} is the total gate-to-drain and C_{gg} is the total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$), g_m is the transconductance, g_{ds} is the drain to source conductance, R_{gs} is the gate-to-source resistance and R_{gd} is the gate-to-drain resistance.

Equation (6) is extended to obtain f_k by substituting $K = 1$ and by making approximation $\omega^4 R_{gd}^2 C_{gd}^4 \ll 1$, $\omega^4 R_{gs}^2 C_{gs}^4 \ll 1$, and $\omega^2 \tau_m^2 \ll 1$.

$$f_k \cong \frac{f_t N}{\sqrt{g_{ds} g_m R_{gs} M^2 + NM\left(g_m R_{gd} + 1\right)}}, \quad (7)$$

where $M = \frac{C_{gs}}{C_{gg}}$, $N = \frac{C_{gd}}{C_{gg}}$, and $f_t = \frac{g_m}{2\pi C_{gg}}$.

The total C_{gs} and C_{gd} without considering overlap capacitance and external fringing capacitance can be calculated as[13]

$$C_{gs} = C_{gsi} + C_{fint}, \quad (8)$$

$$C_{gd} = C_{gdi} + C_{fint}, \quad (9)$$

$$C_{fint} = \frac{W\varepsilon_{Si}}{3\pi} \ln\left[1 + \frac{t_{Si}}{2t_{ox}} \sin\left(\frac{\pi}{2}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\right)\right] \times \exp\{-[(V_{gs} - V_{FB} - 2\phi_f - V_{ds})/(3/2)\phi_f]^2\}, \quad (10)$$

where ε_{Si} and ε_{ox} are the dielectric constants of silicon and oxide; W, t_{si}, and t_{ox} are the width and thickness of the silicon body and the gate oxide thickness, respectively. V_{FB} and ϕ_f are the flat band voltage and Fermi potential, respectively. Equation (7) describes the relation between f_k, the intrinsic small signal parameters and f_t, which also provides a hint for the optimization. It is clear from Eq. (7) that the M and N values can be adjusted to reduce f_k without f_t degradation. But N is almost an independent parameter on the stability model with respect to f_t. The optimization begins with the study of factors related to M and N, especially C_{gs}, C_{gd} and C_{gg}. Equations (8)–(10) show the bias and geometry dependence on C_{gs} and C_{gd} of the DG-MOSFET. By adjusting the applied gate and drain bias, and the geometrical parameters such as t_{si} and spacer length (L_{spac}), the DG-MOSFET can be optimized for better stability performance.

4. Results and discussion

The stability factor is calculated from the extracted Y-parameters for various applied gate (V_{gs}) biases with a drain (V_{ds}) bias of 0.8 V, and is shown in Fig. 2. It is evident from Fig. 2 that the DG-MOSFET attains an unconditionally stable condition at higher V_{gs} since C_{gs} dominates C_{gd} at higher gate bias.

Figure 3 shows the extracted stability factor for various V_{ds} at $V_{gs} = 1.2$ V. As V_{ds} increases, the stability performance degrades due to degradation in C_{gd}, and drain induced barrier lowering (DIBL) also affects device performance at higher V_{ds}.

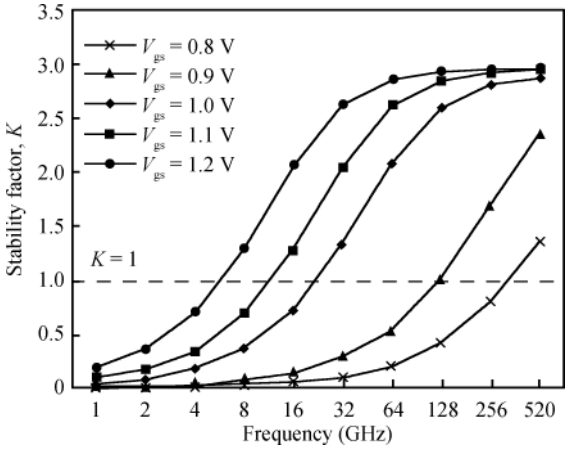

Fig. 2. The extracted stability factor for different V_{gs} at $V_{ds} = 0.8$ V.

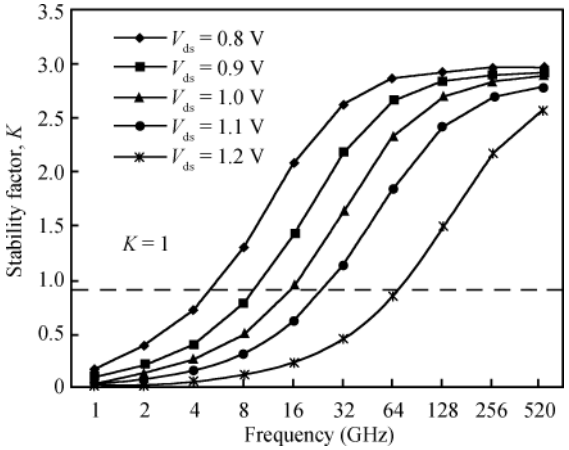

Fig. 3. The extracted stability factor for different V_{ds} at $V_{gs} = 1.2$ V.

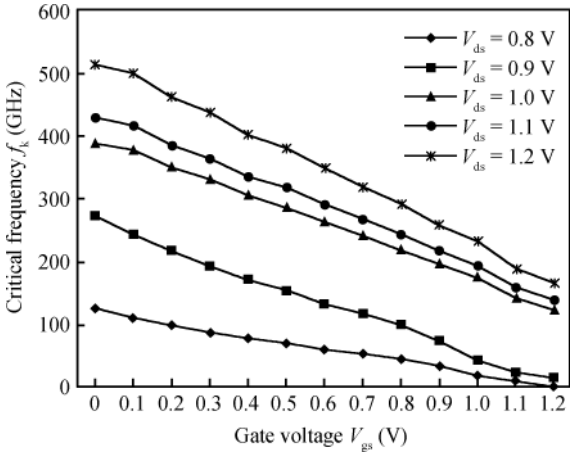

Fig. 4. Critical frequency as a function of gate voltage.

Hence, a smaller drain bias is preferred to operate the DG-MOSFET in the RF range.

Figure 4 shows the critical frequency (f_k) as a function of gate voltage (V_{gs}). The f_k reduces with the increase in gate bias and further reduces with a smaller applied V_{ds}. This shows that at smaller drain biases and higher gate biases, the DG-MOSFET exhibits better RF stability performance.

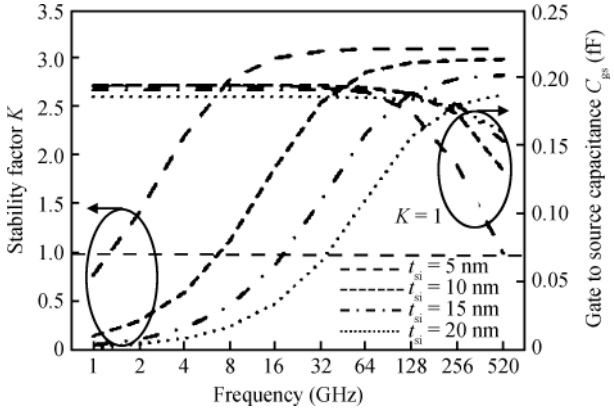

Fig. 5. The extracted stability factor and C_{gd} for different silicon body thicknesses.

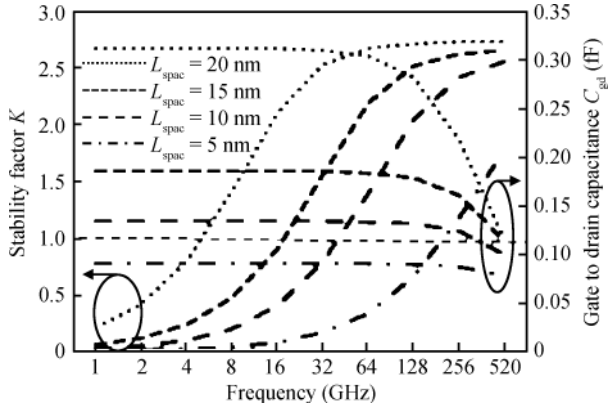

Fig. 6. The extracted stability factor and C_{gd} for different spacer lengths.

Figure 5 shows the extracted stability factor and C_{gd} for various silicon body thicknesses (t_{si}). It is evident that for thinner t_{si}, stability is reached at an earlier frequency compared to thicker t_{si}, since C_{gd} decreases with thinner t_{si}. However, t_{si} cannot be reduced further as it leads to an increase in device oscillation at higher frequency. The parasitic source and drain resistance increases with thinner t_{si}, which also increases the SCEs. The optimized t_{si} for better RF stability is 10 nm, comparable to the ITRS requirement[6] for ultra-thin silicon body thickness.

Figure 6 shows the extracted stability factor and C_{gd} for different spacer lengths (L_{spac}). L_{spac} has an impact on the RF stability performance of DG-MOSFETs. The fringing capacitance increases with thinner L_{spac}, thereby causing oscillation at higher frequency. The DG-MOSFET becomes stable at $f_k = 4$ GHz for an L_{spac} of 20 nm as C_{gd} decreases with L_{spac}. A further increase in L_{spac} will not have any impact on stability because C_{gd} is saturated for larger L_{spac}.

The DG-MOSFET exhibits better stability performance at $t_{si} = 10$ nm, $t_{ox} = 1.6$ nm and $L_{spac} = 20$ nm. Figure 7 shows the extracted stability factor for the optimized structure. It is evident that K reaches 1 at 7.5 GHz which shows that the device can be operated as unconditionally stable from 7.5 GHz onwards. This indicates that the DG-MOSFET does not require an additional circuit when operated from 7.5 GHz onwards in

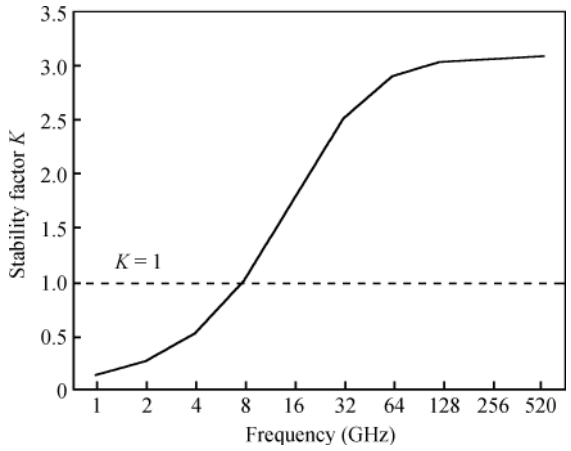

Fig. 7. The extracted stability factor for the optimized DG-MOSFET at $V_{gs} = 1.2$ V and $V_{ds} = 0.8$ V.

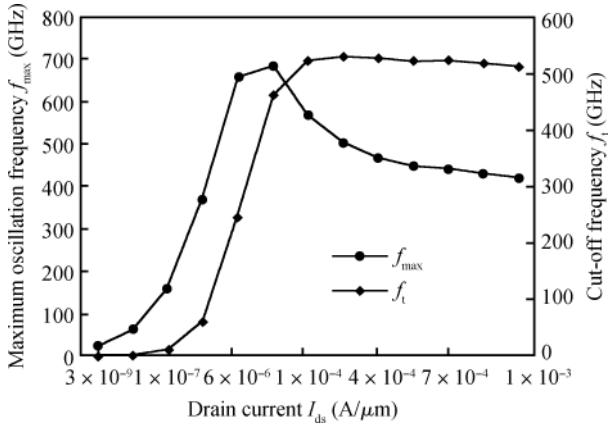

Fig. 8. The variation of f_t and f_{max} with drain current for the optimized DG-MOSFET at $V_{gs} = 1.2$ V and $V_{ds} = 0.8$ V.

RFICs.

It is necessary to observe f_t and f_{max} to understand the capability of the DG-MOSFET under the RF range. The cut-off frequency f_t is evaluated as the frequency for which the magnitude of the short circuit gain drops to unity, which can be expressed as $f_t = g_m/2\pi C_{gg}$. The f_{max} is related to the capability of the device to provide power gain at large frequencies, and is defined as the frequency at which the magnitude of the maximum available power gain drops to unity. It is given by $f_{max} = f_t/\sqrt{4(R_s + R_g + R_i)(R_{ds} + 2\pi f_t C_{gd})}$, where g_{ds} is the drain to source conductance and R_g, R_s and R_i are the gate, source and channel resistances, respectively. The gate resistance is obtained from the extrinsic parasitic model, which can be expressed as $\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_g$.

Figure 8 shows the variation in f_t and f_{max} with drain current for the optimized DG-MOSFET. The bias and geometry optimized structure has an f_t of 650 GHz due to the improved g_m and f_{max} of 700 GHz, which shows that the proposed DG-MOSFET structure is suitable for high-speed switching and high-frequency applications.

5. Conclusion

The RF stability model is developed for a DG-MOSFET, and its stability characteristics are performed through TCAD simulation. The stability of the device is studied for various bias and geometry conditions, and it is observed that C_{gd} and C_{gs} are responsible for the degradation in f_k. The proposed optimized geometry and bias conditions show excellent stability performance. No additional circuit is required as the device is unconditionally stable from 7.5 GHz onwards.

References

[1] Wong H S P. Beyond the conventional transistor. IBM Journal of Research and Development, 2002, 6(2.3): 133
[2] Sorin C, Géard G, Thierry O, et al. Ultimately thin double-gate SOI MOSFETs. IEEE Trans Electron Devices, 2003, 50(3): 830
[3] Liang J, Xiao H, Huang R, et al. Design optimization of structural parameters in double gate MOSFETs for RF application. Semicond Sci Technol, 2008, 23(5): 1
[4] Mohankumar N, Syamal B, Sarkar C K. Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs. IEEE Trans Electron Devices, 2010, 57(4): 820
[5] Sharma R K, Gupta M, Gupta R S. TCAD assessment of device design technologies for enhanced performance of nanoscale DG MOSFET. IEEE Trans Electron Devices, 2011, 58(9): 2936
[6] Sivasankaran K, Kannadassan D, Seetaram K, et al. Bias and geometry optimization of silicon nanowire transistor: radio frequency stability perspective. Microw Opt Technol Lett, 2012, 54(9): 2114
[7] International Technology Roadmaps for Semiconductor (ITRS), 2005
[8] Device simulator ATLAS user manual. Silvaco Int., Santa Clara, CA, May 2006 [Online Available]: http://silvaco.com
[9] Schwierz F, Liou J J. Semiconductor devices for RF applications: evolution and current status. Microelectron Reliab, 2001, 41: 145
[10] Gonzales G. Microwave transistor amplifiers—analysis and design. 2nd ed. Prentice-Hall, 1997
[11] Rollet J M. Stability and power gain invariants of linear two ports. IRE Trans Circuit Theory, 1962, 9: 29
[12] Cho S, Kim K R, Park B G, et al. RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. IEEE Trans Electron Devices, 2011, 58(5): 1388
[13] Sarkar A, Das A K, De S, et al. Effect of gate engineering in double-gate MOSFETs for analog/RF applications. Microelectron J, 2012, 43(11): 873