

# Survey on Energy - Efficient Methodologies and Architectures of Network-on-Chip

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## Abstract

The emerging technology requires a large number of core to be integrated into a single chip. This had led to the development of System on Chip. SoC's have paved way for large scale integration of electronics mounted on a single chip. SoC's are nowadays highly preferred for designing portable and compact devices with low power. The complex and complete integration of SoC has paved way for the concept of Network on Chip (NoC). NoC is a key challenge for power optimization as they are battery operated. In this paper survey provides a design of energy aware NoC with reduced power consumption and enhanced performance. A broad view of power optimization using voltage/frequency Island is provided. The paper also provides a detailed survey of the different data encoding techniques and their efficiency. The objective of this survey is to provide information regarding improved design for reducing power in NoCs. The survey also helps to arrive at a conclusion of the various power optimization techniques.

**Keywords:** Data Encoding Techniques, Network on Chip, System on Chip, Voltage/Frequency Island

## 1. Introduction

The components integrated should be provided interconnections and these links play important role in SoC. Now a day's demand for large number of portable and smart devices has converted the entire system such as Central Processing Unit (CPU), graphics, Routers, etc. into a Single System on Chip (SoC). SoC is now used in many fields such as critical military applications, processors and controllers, medical instrumentation with low power, etc... As these devices are power aware biggest challenge for performance measurement is the power consumption (i.e.,) battery power. Designing a low power device with improved performance parameters and less power consumption is the challenging for design engineers and researchers. Performance of the system should not be affected with reduced power.

Integration of large number of electronics components into a single SoC has increased the complexity of

implementing shared bus into the digital design. Shared Bus architecture will reduce the power overhead due to the inter link in the circuits. NoC is proposed mainly for enhancing the speed of the communication among various components mounted on a single chip. In NoC implementation shared bus architecture is used to increase the speed of the SoC architecture. Network interfaces are used in the NoC for the communication over the chip. This facilitates the NoC to work at a high speed, higher bandwidth and decreased latency. Concurrent programming and execution is supported in NoC based architecture based design. In architecture of NoC it includes all the components such as network interface, switches, schedulers and Virtual Channels (VC), etc.

Design of NoC should also be cost efficient with respect to energy utilization. System level power utilization is also considered for implementing NoC into the communication system. As the number of switches

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increases will gradually increase power consumption. Leakage power is one of the major drawbacks in the digital system. NoC will consume 35% of power in a SoC. Routing algorithms decides the power consumption in the digital systems. These algorithms will decide the path for data packet transmission.

This survey will elaborate the power optimization techniques in Network on Chip (NoC). Section 2 gives the power optimization survey with voltage and Frequency Island and Section 3 explains the data encoding techniques for power reduction, Section 4 concludes the survey on power optimization.

## 2. Voltage Island

Power dissipation in NoCs is one of major problem in digital designing. The power dissipated can be classified as static and dynamic power dissipation. Leakage current is the major cause of static power dissipation and switching leads to dynamic power wastage. Many techniques have been proposed for power optimization in NoCs and Voltage Island (VI) is one of technique for power optimization. VIs efficiently optimizes the power dissipation along with area optimization in the chip.

In<sup>1</sup> has introduced the concept of Voltage Island (VI) for designing a system architecture and implementation methodology for chip. This method can be utilized for power reduction in both static and dynamic System on Chip (SoC) design. Technology upgradation has lead to increased performance with power optimization and also to meet the market demand in time. Voltage Island will be integrated into the SoC to meet the performance requirement in this work. Industrial implementation of Voltage Island is implemented in this work.

In<sup>2</sup> has proposed concept of Voltage Island instead of implementing multiple supply voltage for different components in a System on Chip (SoC). Multiple supply voltage is used for the various components in the finer power supply and to provide improved power optimization. Power consumed by circuits is always proportional to the supply voltage. This approach in industrial implementation will provide power optimization upto ten folds when compared with the logic based industrial system.

In<sup>3</sup> have proposed a method combining both the voltage optimization along with a level shifter assignment problem. Design of low power is necessary due to the improvement of CMOS technology into nanometer. Many

approaches utilize multiple power supplies for power optimization by both dynamic and static dissipation. The proposed approach is implemented in both post and pre floor planning. In the post floor planning a low cost algorithm is implemented for handling the level shifter assignment along with a optimum algorithm for voltage management. In case of post planning a heuristic based approach is implemented for monitoring the area of chip. From the experimental result it is found that proposed technique reduces power by 17% and PNR ratio by 7.2%. This technique is efficient and significant with certain increased runtime for execution.

In<sup>4</sup> have proposed a framework for synthesis of Network on Chip (NoCs) with Voltage Islands (VI). This design will increase the performance according to the requirement with reduced power dissipation. Voltage island based NoCs is becoming tough due to evolution of power consuming chip processors with multiple interfaces. This framework will provide algorithms and approaches base on heuristics to reduce traffic by 62%. Experimental analysis of VI based synthesis is performed on a mesh connected NoC using frameworks named VISION, VISION-P, VISION-B. Communication power is optimized along with the computation power; here distributed control over the network is implemented instead of centralized approach. This will increase the power optimization of about 32%. Total power reduction of about 13% is achieved using this technique.

In<sup>5</sup> has proposed a method for power optimization by combining voltage segmentation along with forming islands in order to reduce power, chip area and runtime. There are many techniques forte power optimization in System on Chip (SoC) and among them voltage island is preferred in order to reduce power with more gain. Here one application driven Power State Machine (PSM) is employed and region with similar supply voltage are grouped for creating islands. After identification of core voltage a look up table is created with heuristic approach. Employing this technique will result in power reduction of about 8.7% and also improves runtime by 2.4 times.

In<sup>6</sup> have developed some algorithm as solution of power consumption due to voltage assignment problem and network flow issues. Two algorithms were developed; mini-cost flow algorithm is developed for voltage assignment problem under time constrained environment. Value oriented branch and bound is also developed for network level power optimization. MCF algorithm is employed to assign voltage to the certain

network under time constrained environment followed by a MCF solver. VOBB is a tree based algorithm works upon searching method and solves the voltage assignment problem. Multiple supply voltage is proposed as solution for voltage assignment problem now a day. In the case of MSV, it should be designed with certain time constraints and in this work MSV is apply along with floor planning layout. This proposed framework will provide power optimization in the floor planning of circuit layout itself. MCF algorithm followed by VOBB is applied at the ground level floor planning with a physical layout design. From the results, this approach has provided a improvement in power optimization.

In<sup>7</sup> have proposed voltage island technique instead of Multiple Supply Voltage (MSV) in 3D ICs. Introduction of 3D ICs are proposed to reduce the interconnection delay and delay to improve the overall performance of the chip. But 3D IC has increased the power consumption and power density of chip due dense fabrication. Applying MSV as a solution for reducing voltage increased the complexity along with path delay with multiple supplies. Voltage island technique is applied to resolve the MSV technique by grouping the modules with same voltage. In this work voltage island is implemented along with Mixed Integer Linear Programming (MILP) and this technique will reduce the power due to routing in network. From the experimental results it has been derived that power reduction of about 23% is obtained due to this technique.

In<sup>8</sup> proposed a technique based on Voltage Island for power reduction in CMOS circuits. CMOS active power is major power consumption in these circuits. In this work selective custom design is employed along with internal regulations based on voltage. By applying these techniques power reduction can be obtained upto 25%.

In<sup>9</sup> have introduced the concept of voltage and frequency island combined together to provide better power optimization in digital circuits. Multi core system on chip has become more complex due to integration of high level modules and this has correspondingly raised the power utilization. Clocking is important in digital system for triggering any operation and supplying single global clock over the network increase the time and energy utilization. In this work a global asynchronous and locally synchronous clock is generated for lower power utilization. NoC is partitioned into multiple VFIs and different supply and threshold is applied to each VFIs. This technique will reduce power consumption by about 40%.

In<sup>10</sup> presented a technique with combination of partitioning, mapping and interfacing. Voltage and Frequency Island (VFIs) performs a significant power reduction in Network on Chip (NoC). Here VFI is implemented in partitioning, routing and mapping of a digital design. VFI is uniformly implemented over entire network and thus this will reduce the overhead due to clock input or buffer output. Employing this technique will reduce power consumption by 10% and this will be more optimized then global energy optimization framework.

In<sup>11</sup> proposed a technique to solve the problem due to voltage and frequency assignment in various applications. Assigning voltage and frequency islands in a globally asynchronous and locally synchronous have some integration problem in the network. Applying static voltage assignment over the network will reduce the complexity in the network and also problem due to assigning different clock dynamically. Power consumption by dynamic assignment is more when compared to the static VFI. Incase of specific dynamic voltage assignment will provide energy saving upto 44%.

In<sup>12</sup> introduced a method combining reduction of power due to computation and communication over the network. A framework is developed to reduce power utilization using genetic algorithm. Voltage island technique is implemented in digital system to reduce the power by applying unique voltage supply to the group of identical core. The algorithm will automatically perform path estimation, allocation, and routing, mapping, speed assignment parallelly. The proposed algorithm is implemented in the network with different topologies. From the experimental results the proposed technique performs well and reduces energy consumption in digital systems.

In<sup>13</sup> have introduced a approach for customizing the shutdown of voltage island, which is not in use. Here a application specific NoC is designed for the selective shutdown of voltage islands in a system. Interconnection architecture is a major thread in shutting down the voltage and frequency islands in the NoCs. From the experimental results this approach has achieved a power saving of about 3% and area reduction on chip.

In<sup>14</sup> introduced a mapping of real time applications into many cores. MPSoCs design is challenging due to the increasing complexity and high integration density on a single chip. Low power utilization is achieved by assigning different task for on processors and V/F levels to various

Processing Elements (PEs). Global Asynchronous and Locally Synchronous (GALS) is a preferred approach for V/F partitioning. Network on Chip (NoC) will implement its Mixed Integer Linear Programming (MILP) in GALS based system. In this work reliability of the system is solved using fault analysis in MILP. Heterogeneous PEs is implemented to avoid the error due to threshold formulation. This approach creates NP-Hard problem, hence heuristics based sampling technique is executed. From the experimental results 70% of power reduction is achieved using this technique.

In<sup>15</sup> have proposed a technique for solving problem of distribution of single clock throughout the entire chip, which is major drawback in high performance VLSI system. In this work a reconfigurable FIFO is proposed for assigning clock in case of synchronous and asynchronous system. Network on chip (NoC) is divided into various voltage and frequency islands for achieving gain in power management. These synchronous system designs is not required, if the switched located adjacent have same clock and in addition to reconfigurable FIFO Reconfigurable Mesosynchronous FIFO is also designed. Various techniques for implementing these FIFO are described and which reduces the power utilization, latency and even area overhead in the NoCs. From the experimental results it is compared with non reconfigurable system. NoC based on reconfigurable FIFO for clock generation performs well. Power consumption is reduced by 17% in NoCs and this will result in overall improvement of about 29% in power and latency reduction.

In<sup>16</sup> have proposed a power optimization technique using voltage and frequency island based three dimensional SoCs with multicore architecture. SoCs with multiple cores are been the great solution for complicated applications utilizing less system power. VFI base on two dimensional techniques are used in the existing system where as in this work 3-D based VFI is proposed. The proposed system also handles deadline and thermal limitations. Energy aware scheduling of the task and power balancing is utilized in the thermal constraints. 2-D is implemented in core mapping and island partitioning with similar voltage. From the experimental results power reduction of about 15.8% is achieved.

In<sup>17</sup> have proposed energy aware power reduction technique to reduce the power consumption and cost of hardware in VFI based NoC implementations. Voltage and frequency based NoC implementation is a energy

aware architecture design for digital system. Usually in VFI based NoC system various clock frequencies and voltages are distributed to group of cores and here processing elements are partitioned to reduce the workload due to communication. In this work power optimization with respect to communication overhead is optimized by efficient routing and mapping algorithms in inter communication among VFI. From the experimental results power optimization of 32-15% is achieved.

In<sup>18</sup> have proposed the voltage island technique with power down mode for power optimization. Power down mode is applied to the entire core with floorplanning. The floor plan will provide better solution with optimal voltage assigning and partitioning. Multiple Supply Voltage (MSV) is used for providing various voltages to the island cores. Here power down is used along with the MSV to further reduce power consumption. Simulated annealing technique is used for searching. Applying this to the digital design reduces power by 50% for all data sets. In this work power is optimized using power down mode as well as by placing the island near corresponding pin.

In<sup>19</sup> introduced a technique for power optimization in NoC depending upon the workload and operational constraints. Voltage and frequency scaling in implemented to reduce power by grouping similar cores working on same frequency range. In this work a runtime optimization of the power is proposed by implementing dynamic voltage scaling in the network depending upon the current workload of the system. A real-time video is compressed and experimental test are conducted to estimate the power reduction. Here a state space feedback strategy is used in order to handle the dynamic voltage and frequency scaling. From the experimentation results, it performs well with a unique voltage and clock distributor. GALS based NoC architecture is used in power reduction and power estimation of proposed work.

In<sup>20</sup> have proposed hardware based technique for power optimization with dynamic voltage and frequency scaling depending upon the workload at particular time. Voltage and Frequency Island has the advantage of both speed and voltage control over the NoC. In the proposed method frequency is varied according to the speed and voltage of the synchronous islands. A FIFO based interface is used in multi clock distribution in the network on chip architecture. From the experimental results power gain of about 65% is obtained.



### 3. Data Encoding

Power consumption in NoC can be optimized by many techniques. One of the efficient methods to reduce the power due to transition of data in the network. Data Encoding is used here for power optimization by encoding the data using various data encoding techniques before transition. This is specially proposed for bus based system in NoC. Run time encoding is a significant technique for low power techniques and utilized for on chip as well as off chip. Dynamic encoding is implemented in the run time data encoding which proportional to the switching. Hence this switching will reduce the power for encoding. The data encoding techniques can be classified into two folds. First category is encoding to reduce power due to switching activity and another one is to reduce power due to coupled switching in NoCs.

In<sup>21</sup> has presented a data encoding technique to reduce power consumption in Network on Chip (NoC). Power consumption in NoC is mainly due to the interconnect in network data buses. On chip power reduction is required to achieve the low power consumption in digital system. In this paper the data packets are encoded before transmitting in the network. This will reduce both the switching and couples switching power in the NoC based system design. But overhead is created due to encoding and decoding in the network interface. From the experimental results power consumption of about 26% is obtained using this technique.

In<sup>22</sup> have proposed data encoding as a technique for power reduction in Network on Chip (NoC). The proposed technique does not employ any change in the routers and the link for data transition in the chip. Data encoding will reduce the amount of data by compressing them into some form and coding those data into transition buffer. This technique can be implemented in both the traffics synthetic and run time traffic. from the experimental results this technique has reduce power consumption of about 51% with less power as well area overhead in the network.

In<sup>23</sup> have employed a data encoding technique to reduce power consumption without any modification in its performance. Data packets are encoded before sensing them into transmission buffer and this technique will reduce the power consumption without affecting its performance. Data encoding based on memory controller is less effective when compared with FSM based memory controller. From the experimental results comparing both

the controllers has produced an area reduction of 43% and power optimization around 38%. The FSM based controller has resulted in a throughput of about 32% when compared with existing techniques. This technique is tested with different traffic parameters and more energy optimized then other techniques.

In<sup>24</sup> introduced a technique to reduce the power utilization and traffic due to crosstalk interference and power due to wire in NoC architecture. In this paper a power aware reliable encoding scheme for NoC which supports reconfiguration dynamically. Data encoding techniques and reasoning framework are combined for effective encoding strategy in NoC architecture. By implementing this power aware encoding 83% of power reduction is obtained due to interference and application level power reduction of 39%. Many data encoding algorithms are implemented and the performance in terms of power and performance are evaluated. Dynamic reconfigurations during run time will further reduce the power loss due to data transition.

In<sup>25</sup> have proposed a hardware based technique for data encoding in the Network on Chip (NoC). In this work Clock gating is employed along with the data encoding techniques. Clock gating will reduce the power to dynamical power dissipation. FPGA is used for testing the data integrity and data encoding. From the experimental results FPGA based system performance is less effective when compared to the performance of ASIC based system. Power consumption is also due to the encoder and decoder circuit in the system. This will increase additional power consumption where as encoder design should be power optimal. This system performs well in ASIC based system design.

In<sup>26</sup> has proposed a hardware improvement in area and the number of logic gates used in a 2-D LFSR which can be applied to test anSoC with multiple IP cores. This helps to reduce the hardware architecture and also the same configuration can be used to test the different IP cores.

In<sup>27</sup> has proposed the power reduction technique by implementing the data encoding technique in the NoC. The proposed data encoding technique is based on the priority. Data encoding implemented to reduce the data density in the network, but for data encoding it requires encoder and decoder. Encoder will itself require some power which increases the power consumption, hence priority based coding is implemented. Data transmitted to next neighbor node should not be encoded while the transmission cost is less compare to encoder. Hence

effective power reduction can be achieved using distance based data encoding.

In<sup>28</sup> introduced the concept of bus inverting encoding technique to reduce the power consumption due to the power, crosstalk noise, etc... Network on Chip (NoC) is used to provide better performance with reduced latency ensuring low power and area overhead. In the case of circuit with high end chip design, crosstalk noise will reduce performance and power dissipation will increase enormously. In this work a detector is designed to reduce the error before transmission and this will in turn reduce the power consumed for error correction in the network. Storing the data and routing them for error correction consumes lot of power. From the experimental results crosstalk errors with various multimedia patterns are evaluated and results show that it provide better performance in terms of cost.

In<sup>29</sup> have introduced the data encoding technique with wormhole switching between the end to end task to reduce the power consumption in the circuit. In this work a network interface is added between the encoder and decoder. This interface will encode the data before transmission and decode before reception of data. Network interface will be transparent to the underlying entire network. This technique does not employ any change in routers and tested with all traffic criteria. From the experimental results power reduction of about 37% is achieved in switching activity and 18% of coupled switching without any degradation in performance and area.

## 4. Conclusion

This paper reviews various power optimizations techniques in NoC based system design. Power is the major drawback in designing any digital circuit especially in communication systems. Voltage/Frequency Islands and data encoding techniques are described for power optimization in NoC. From the above survey various power optimization techniques using VFI is elaborated. Low power digital design is implemented along with these digital techniques to achieve low power.

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