Universal Verification Methodology Based Verification of UART Protocol

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Bidisha Kashyap[1], Ravi V[1*]
[1]School of Electronics Engineering, Vellore Institute of Technology, Chennai, India
[*]ravi.v@vit.ac.in

Abstract. Verification today acts as a constriction of any complex VLSI design. Bringing out improved verification efficiency is a must. Most of the computers and microcontrollers contain a number of serial data ports. These data ports are used to connect with devices such as keyboards and printers which are basically serial input and output devices. Transmission and reception of serial data from an isolated location can be done with the help of a modem connected to the serial port. UART- Universal Asynchronous Receiver and transmitter is a hardware device which facilitates serial transmission and reception of data. In this work presented here, the UART has been designed with the use of the industry standard Verilog HDL code and the verification of the protocol has been done using system Verilog code in UVM environment. The UVM based verification methodology can significantly reduce the time needed for verification.

1. Introduction

Most UART is a computer hardware device that is used for serial communication. The device is used for data exchange between a computer and outer devices as it provides high reliability and capability of data transmitting to a long distance. It is used to control the process of converting parallel data into serial data. It consists of one transmitter and one receiver.

The basic structure of the UART illustrating the process of both transmission and reception is shown in Figure1.

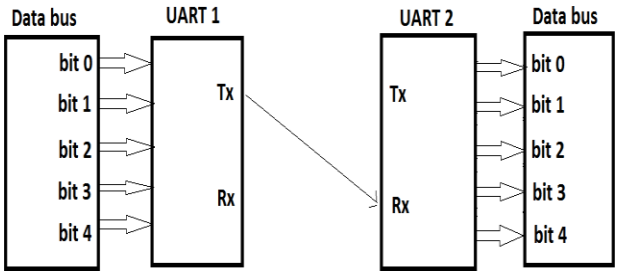

Figure 1 Illustration of transmission and reception of UART

The conventional verification techniques do not provide verification environments which can be reused over again. The time to market of these conventional techniques is also very slow [1]. The Universal Verification Methodology (UVM) library contains reclaimable components as well as

environments for test with the help of System Verilog. The UVM is a standard methodology used for the verification of integrated circuit designs. Reusability, scalability, interoperability and all these things can be achieved through methodology only like UVM which serves as a great advantage of using UVM [2].

The Section 2 in this paper presents a discussion on UART protocol and it's working. Section 3 discusses about the Universal Verification Methodology and the following section i.e. section 4 presents the registers used in the UART protocol. Section 5 discusses about results and the Conclusions are presented in section V6.

2. UART Protocol Overview

In this UART stands for Universal Asynchronous Receiver and Transmitter. The objective of a UART device is transmitting and receiving serial data. In UART communication, there are two UART devices, namely transmitter and receiver. The role of the transmitting UART is to convert parallel data to serial data [3]. The receiving UART again converts the serial data to parallel form. One big advantage is that only two wires are needed for transmission and reception of data between two UARTs [4].

UART is an asynchronous device i.e. it does not have a clock signal to synchronize data. Instead of a clock signal, the data frame consists of start bits and stop bits. On receiving the start bit the UART knows that it has to start reading the bits. The frame structure of UART protocol is shown in Figure 2.

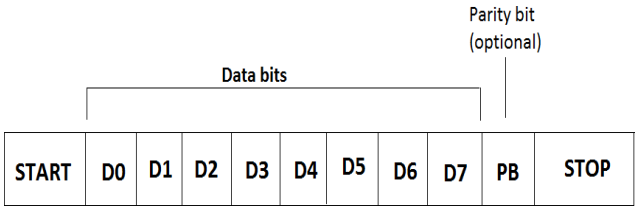

Figure 2. Frame structure of UART protocol

After detecting the start bit, at some frequency UART reads the bits is known as Baud Rate. The unit of Baud rate is bits per second .The Transmitter UART and Receiver UART should work on same baud rate. In UART data bus is used to transmit and receive the data. Data is transferred in parallel form the transmitter to receiver. After that, the data frame is created by adding start, stop and parity bit. This data frame is sent serially on Transmit pin. The receiver starts reading the data frame bit by bit at its receiving end. And it is again converted into parallel form by removing star, stop bits [5]. The data which is to be transmitted is arranged into frames. Each Frame carry one start bit, five to nine data bits, parity bit, and one or two stop bits. The actual data length can be five to eight bits.
Two modes to do the communication between UARTs:

- Half Duplex Mode:- In Half duplex mode the communication is done only from transmitter to receiver which means only in one direction.
- Full Duplex Mode:- In full duplex mode two UARTs can transfer data with each other concurrently.

There are several advantages of the UART protocol such as:

- It is two wired protocol.
- Clock signal is not required.
- Error detection is possible.

3. Universal Verification Methodology

The UVM as mentioned earlier is a standard method for verification. The Universal Verification Methodology (UVM) has many class libraries which help to reuse environment, also in UVM methods are defined in base classes [6]. By using these base classes an environment can be created.

UVM environment consist of many blocks such as sequencer, scoreboard, stimulus, monitor and driver. The data is generated by sequencer and is send to DUT by driver. Then it is compared in Scoreboard. The monitor monitors the response which is received.

A brief description on all the testbench elements is given here:

The test is the topmost class. At first the testbench is configured .Second is to construct a test bench . Third is the sequence which starts the stimulus.

- The UVM Env: in UVM environment more than one scoreboard and agents are grouped together.
- The UVM Agent: consist of the components which are related to interface .
- UVM DRIVER :drives or send the data between sequence_item and DUT .
- UVM SEQUENCE: the sequencing of data items generation and reception towards or from the driver is done.
- The UVM Monitor: it notice the activity of the signals which are there on interface and scoreboard receives those packets from monitor.
- The UVM Scoreboard: predicted values and the data received from monitor is being compared.

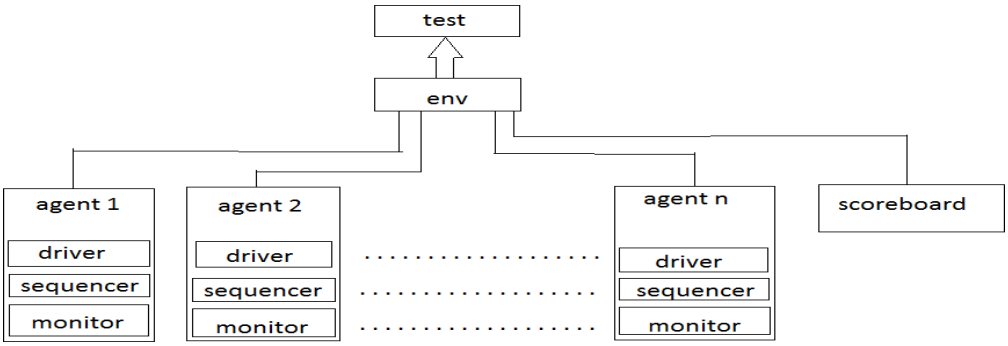

Figure 3. UVM test bench hierarchy

4. Registers used in UART

There are several registers that are being used in the UART which are mentioned as follows:

- Interrupt Enable Register: This is an 8-bit register and has both Read/Write access. There are several interrupt requests generated by the UART. Enabling and disabling of each type of these requests is done by the register. Only the requests that are enabled in the register are forwarded to the CPU.
- Interrupt Identification Register: A UART generates a processor interrupt when there is a state change on the communication device. An additional information is needed prior to the necessary actions that are to be taken in response to an interrupt. The IIR interrupt identification register plays a role here. The bits of the register show the current state and which state change is causing the occurrence of interrupt.
- FIFO Control Register: This is an 8-bit register and a write-only register. The FCR, as the name suggests controls the activities of FIFOs.
- Line Control Register: This register is used for controlling the format of the asynchronous data communication. This is an 8-bit register.

- Line Status Register: The Line Status Register (LSR) gives information regarding the status of data transfer to the CPU. It also gives information about the current state of communication.
- Divisor latches (DLL and DLM): The DLL and DLM are two eight bit registers also called divisor latch registers. There are latches in the two registers. For the generation of the baud clock in the baud generator, these latches are employed in storing the 16-bit divisor. The MSB of the divisor are stored by the DLM register and the LSB are stored by the DLL.

5. Results

In the work presented here, the data bus width of both the transmitting and receiving UART is 8. The interface being used here is the Wishbone Interface. The interface is a powerful mechanism which is used for connecting the Design under test (DUT) and Test Bench.

The Design is done using Verilog HDL and SystemVerilog. The verification is done by using UVM Test Bench. There are several test cases that are being verified in the work presented here. The test cases are namely Full Duplex test case, Half Duplex Test case, Parity Error test case and over run test case.

The Simulated waveforms are shown in the Figure 4-6:

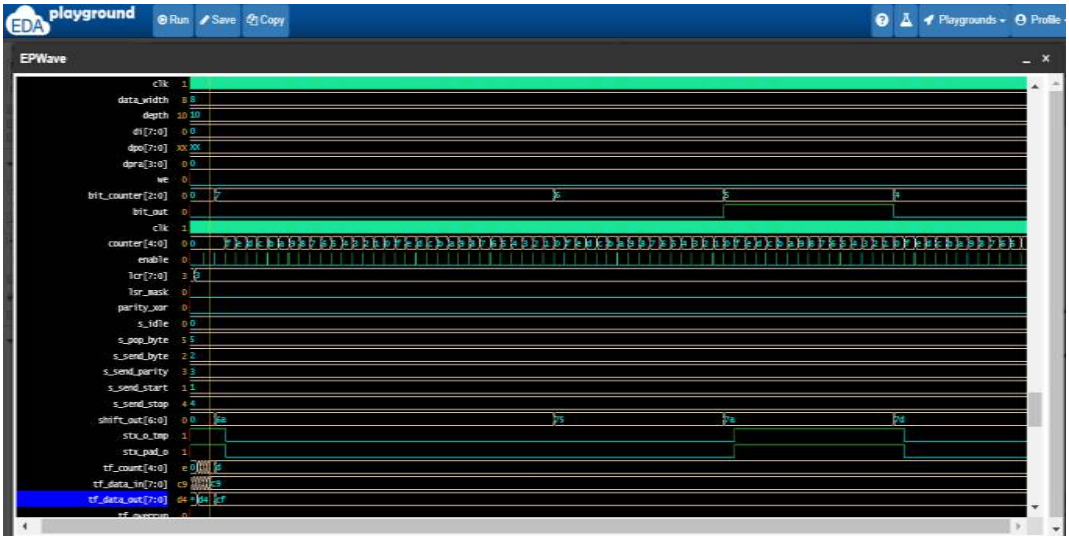

Figure 4. Functional simulation response of UART-Wishbone communication

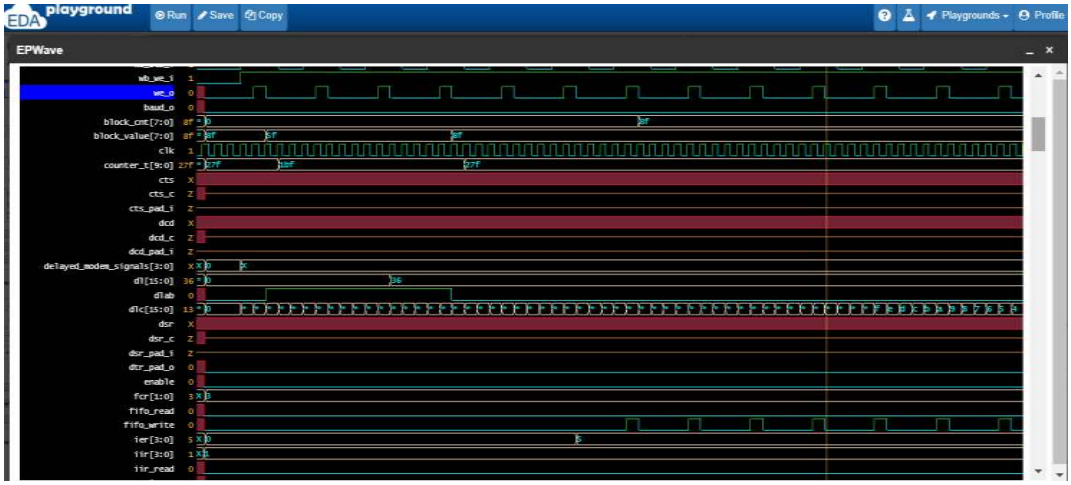

Figure 5. Functional simulation response of UART communication

```
# KERNEL: --- UVM Report Summary ---
# KERNEL:
# KERNEL: ** Report counts by severity
# KERNEL: UVM_INFO :   131
# KERNEL: UVM_WARNING :     0
# KERNEL: UVM_ERROR :     0
# KERNEL: UVM_FATAL :     0
# KERNEL: ** Report counts by id
# KERNEL: [DRV]     41
# KERNEL: [MON]     41
# KERNEL: [RNTST]      1
# KERNEL: [SB]     40
# KERNEL: [TEST_DONE]      1
# KERNEL: [UVM/RELNOTES]      1
# KERNEL: [UVMTOP]      1
# KERNEL: [uart_driver]      2
# KERNEL: [uart_monitor]      2
# KERNEL: [uart_scoreboard]      1
```

EPWave

Figure 6. UVM Report Summary

6. Conclusion

The UART is successfully designed using Verilog HDL and System Verilog. The verification is successfully done using UVM methodology. The UART Protocol functionality has been verified successfully. The different test cases are also implemented. This communications between the two UART devices are seen to be working as per requirement. The UART Receiver is also capable of converting Serial data into parallel data.

References

[1] Agrawal, Ritesh Kumar, and Vivek Ranjan Mishra. 2013 The design of high speed UART 2013 IEEE Conference on Information & Communication Technologies.

[2] Mahat, Nennie Farina. "Design of a 9-bit UART module based on Verilog HDL 2012 10th IEEE International Conference on Semiconductor Electronics (ICSE). IEEE

[3] Nanda, Umakanta, and Sushant Kumar Pattnaik 2016 Universal asynchronous receiver and transmitter (UART) 2016 3rd International Conference on Advanced Computing and Communication Systems (ICACCS). Vol. 1. IEEE

[4] Ashok, A. and Ravi, V., 2017, March. ASIC design of MIPS based RISC processor for high performance. In 2017 International Conference on Nextgen Electronic Technologies: Silicon to Software (ICNETS2) (pp. 263-269). IEEE.

[5] Gallo, Raffaele, et al. "Revision and verification of an enhanced UART 2004 IEEE International Workshop on Factory Communication Systems, Proceedings. IEEE.

[6] Ni, Wei, and Xiaotian Wang 2015 "Functional coverage- driven UVM-based UART IP verification." 2015 IEEE 11th International Conference on ASIC (ASICON). IEEE.